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Benchmarking of Phase Locked Loop based Synchronization Techniques for Grid-Connected Inverter Systems

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***Abstract*—Grid-connected renewables are increasingly developed in recent years, e.g. wind turbine systems and photovoltaic systems. Synchronization of the injected current with the grid is mandatory. However, grid disturbances like voltage sags, harmonics, and frequency deviations may occur during operation, becoming inevitable challenges to the synchronization of the grid-connected renewable energy systems. In order to ensure the quality of the power generation from the renewables, robust and reliable synchronization methods are in demand. Among the prior-art solutions, Phase Locked Loop (PLL) based synchronization methods have gained much popularity in grid-connected applications. However, an appropriate selection and thus a proper design of the selected PLL synchronization remain of interest in practice, especially for single-phase systems. Therefore, in this paper, a benchmarking of the main PLL synchronization methods for single-phase grid-connected inverter systems in terms of accuracy, dynamic response, harmonic immunity, etc., has been conducted. Experiments on a 1-kW single-phase grid-connected system, suffering from different grid disturbances, are performed for the benchmarking. The experimental results have verified the discussions.**

***Index Terms*—Phase locked loop (PLL), synchronization, T/4 delay PLL, inverse park transform PLL, enhanced PLL (EPLL), second order generalized integrator PLL (SOGI-PLL), multi-harmonic decoupling cell PLL.**

I. Introduction

Power electronics technology has enabled an increasing integration of renewable energy into the grid [1]–[3], e.g. wind turbine and photovoltaic systems. However, due to the intermittency of renewable energy, it has also brought harmonic challenges to the grid [4]–[6], as a fluctuating power is continuously injected to the grid. Since the inner current controller of a typical two-cascaded control system [1], [4] is responsible for shaping the current (e.g., power quality issues) in such applications, efforts have to be devoted to the control of the feed-in grid current, which has to be synchronized with the grid voltage using a synchronization system. Fig. 1 demonstrates the significance of synchronization in the entire control of a single-phase system. As it can be seen in Fig. 1, the information provided by a synchronization is of ultimate importance, and it is used at different levels of the entire control system, e.g. for a reference frame transformation (the $\alpha\beta$-stationary frame $\rightarrow$ the dq-rotating frame).

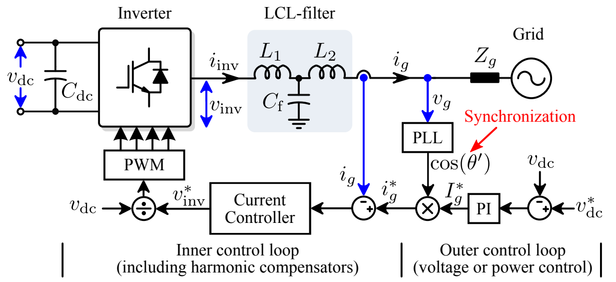

Fig. 1. Overall control structure (dual-loop) of a single-phase grid-connected inverter system with an LCL-filter.

In the literature, a vast of synchronization methods have been reported [4], [7]–[17], [29]. These prior-art synchronization methods can be categorized into a) mathematical analysis methods (e.g., grid synchronization based on the Discrete Fourier Transform - DFT) [16], [18]–[20] and b) Phase Locked Loop (PLL) based synchronization techniques. The first category are based on signal processing techniques, e.g. the DFT and Hilbert transform analysis, which are commonly implemented in a digital controller, and thus has a strict requirement of the sampling rate [4], [8], [21]. In contrast, a PLL synchronization method is a closed-loop system, which is widely used in the grid-connected systems [4], [12]. However, for single-phase applications, where only the grid voltage v_g is measured, it requires more dedications to the synchronization.

Advanced control strategies can thus be applied to an inverter system, while its performance significantly relies on the dynamics of the synchronization, as shown in Fig. 1. Both the mathematical analysis and the PLL based synchronization are able to provide accurate and fast information for the control in the case of a normal grid condition [8], [14], [18]. However, the grid voltage cannot always be maintained as "constant" in terms of amplitude, frequency, and phase, due to multiple eventualities like continuous connection and disconnection of loads and fault to ground [22], [23]. Together with the harmonics in the grid voltage (e.g., due to non-linear loads), a big

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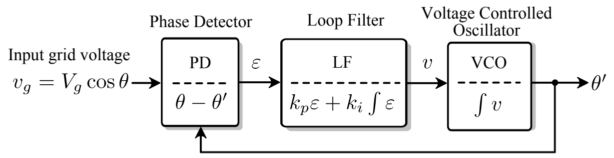

Fig. 2. Basic block diagram of a phase locked loop system for grid-connected inverter systems, where V_g is the grid voltage amplitude.

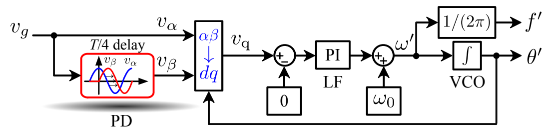

Fig. 3. Detailed structure of a phase locked loop system by introducing a quarter phase delay ($T/4$ Delay PLL), where $\omega_0 = 2\pi f_0$ with f_0 being the nominal grid frequency.

obstacle for synchronization, especially for the Fourier based method [16], [24], has been imposed on. Thus, it calls for an advancement of these synchronization techniques in order to enhance the entire system performance, requiring a clear identification of the pros and cons of the synchronization methods. Alternatively, a benchmarking of the most commonly-employed PLL techniques could contribute to not only an enhancement of the PLLs but also a development of new PLLs. As a result, an advanced synchronization system will ensure a more reliable control of the injected current and thus a more reliable and stable operation of the entire grid-connected inverter system.

In light of the above issues, a benchmarking of several selected PLL based synchronization methods is conducted in this paper. Firstly, the basics of the single-phase PLL system are presented in § II, including the small signal modelling and basic design considerations. Then, § III gives a description of the selected PLL synchronization methods, including the $T/4$ Delay PLL, the Inverse Park Transform PLL (IPT-PLL), the Enhanced PLL (EPLL), the Second Order Generalized Integrator based PLL (SOGI-PLL), and the Multi-Harmonic Decoupling Cell based PLL (MHDC-PLL). Followingly, those synchronization techniques are benchmarked in terms of accuracy, dynamic response, harmonic immunity, and etc. by experimental tests in § IV, where the grid suffers from various disturbances. A conclusion is then drawn.

II. Basics of Single-Phase PLL Systems

As it can be seen in Fig. 1, the PLL system plays a key role in the entire control loop of grid-connected inverter systems. Typically, a PLL system consists of a Phase Detector (PD), a Loop Filter (LF) which is performed by a Proportional Integrator (PI) controller, and a Voltage Controlled Oscillator (VCO). Fig. 2 represents the basic block diagrams of a PLL system that is widely utilized in grid-connected applications. Accordingly, the transfer function of the PLL system $G_{\text{PLL}}(s)$ can be described as,

$$G_{\text{PLL}}(s) = \frac{\theta'(s)}{\theta(s)} = \frac{k_p s + k_i}{s^2 + k_p s + k_i} \tag{1}$$

where θ is the grid voltage phase, θ' is the locked grid voltage phase, k_p and k_i are the proportional and integral gains of the PI controller (i.e., the LF).

It can be seen from (1) that the PLL system is a typical second order system [4]. Therefore, the damping ratio ξ and the undamped natural frequency ω_n of (1) can be calculated by,

$$\xi = \frac{k_p}{2\omega_n}, \text{ and } \omega_n = \sqrt{k_i}.$$

Subsequently, the settling time of the PLL system can be approximated as,

$$t_s = \frac{4.6}{\xi\omega_n} = \frac{9.2}{k_p} \tag{2}$$

which can be used to benchmark the transient performance of different PLL systems, and also can be taken as guidelines for tuning the LF parameters:

$$k_p = \frac{9.2}{t_s}, \text{ and } k_i = \left(\frac{k_p}{2\xi}\right)^2 \tag{3}$$

where $\xi = \sqrt{2}/2$ is typically chosen for a satisfactory and optimal damping.

In the case that the control parameters of the LF (i.e., k_p and k_i) are set to be identical in different PLLs, the performance of the PLL synchronization methods will strongly rely on the configurations of the PD system. A sinusoidal multiplier is the most intuitive way to the implementation of a PD system, but it introduces double-frequency harmonics in the closed-loop system [13], which cannot be fully eliminated by the LF (i.e., the PI controller). Therefore, the task of advancing a PLL system is shifted to improve the detection of the phase error (i.e., $\varepsilon = \theta' - \theta$) using the input grid voltage v_g and feedback signals (e.g., the estimated phase θ'). The following demonstrates how the PD systems are constructed in the most commonly employed single-phase PLL techniques.

III. Selected PLL Synchronization Methods

As previously discussed, a number of single-phase PLL based synchronization methods have been developed in the literature. In this section, the most popular PLL systems are presented, including their basic design guidelines.

A. $T/4$ Delay PLL

An alternative phase detection can be achieved with the aid of the Park transform ($\alpha\beta \rightarrow dq$), where a virtual system (β variable) that is in-quadrature with the grid voltage v_g (α variable) is required in single-phase applications. Simply, a quarter delay of the input grid voltage is a possibility, being the $T/4$ Delay PLL, as it is shown in Fig. 3, where T is the known fundamental period of the input grid voltage v_g.

Specifically, on an assumption that the grid voltage is purely sinusoidal, i.e., $v_g(t) = V_g\cos(\theta) = V_g\cos(\omega t + \varphi_0)$ with ω being the grid angular frequency and φ_0 being the initial phase angle, applying the Park transform yields,

$$\mathbf{v}_{\text{dq}} = \overbrace{\begin{bmatrix} \cos(\theta') & \sin(\theta') \\ -\sin(\theta') & \cos(\theta') \end{bmatrix}}^{\boldsymbol{T}_p} \mathbf{v}_{\alpha\beta} \approx V_g \begin{bmatrix} 1 \\ \varepsilon \end{bmatrix} \tag{4}$$

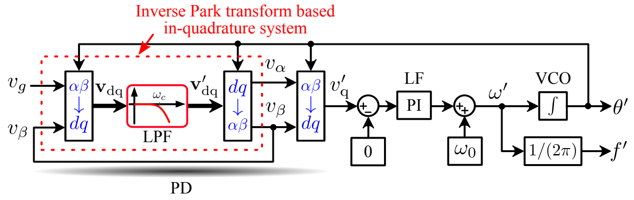

Fig. 4. Block diagram of the inverse park transform based phase locked loop (IPT-PLL).

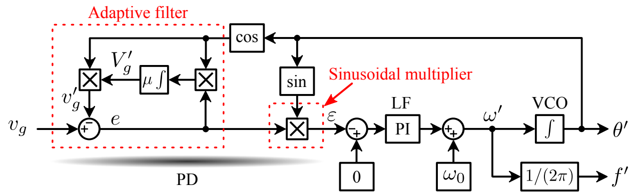

Fig. 5. Enhanced phase locked loop (EPLL) system based on an adaptive filtering technique [9].

where $\boldsymbol{T}_p$ is the Park transform matrix. Eq. (4) shows that the detected phase error ε (i.e., v_q/V_g) can be regulated by a PI controller so that the grid voltage phase θ is locked as θ' in the steady-state. In addition, the grid voltage amplitude $V_g = v_{\text{d}}$ and frequency $f' = \omega'/(2\pi)$ can also be obtained according to (4) and Fig. 3, respectively.

In regards to the implementation of the $T/4$ Delay PLL, a fixed delay of a quarter period (i.e., $T/4 = 1/(4f_0)$ with f_0 being the nominal grid frequency) is normally adopted for simplicity. As a result, the dependence of the grid voltage frequency f_0 to create the virtual in-quadrature system makes the $T/4$ Delay PLL not very suitable for the single-phase applications, where the grid voltage is subjected to frequency variations [25]. Moreover, the background distortions will directly propagate to the LF when the input voltage is delayed for a quarter period. This becomes another big challenge to the $T/4$ Delay PLL.

B. Inverse Park Transform PLL (IPT-PLL)

Another possibility to detect the phase error seems to be a good one for single-phase systems, and it is based on the Inverse Park Transform (IPT, $dq \rightarrow \alpha\beta$) [4]. Fig. 4 shows the block diagram of an IPT based PLL system (IPT-PLL). When compared to the $T/4$ Delay PLL, the IPT-PLL requires two additional Low Pass Filters (LPF), and thus certain harmonics in the grid voltage will not propagate to the LF, contributing to a good harmonic rejection. Thus, from the harmonic immunity point of view, the IPT-PLL is better than the $T/4$ Delay PLL.

According to Fig. 4, the PD structure of the IPT-PLL system can be described by the following:

$$\mathbf{v}_{\text{dq}}(s) = \boldsymbol{T}_p(s)\begin{bmatrix} v_g(s) \\ v_\beta(s) \end{bmatrix}, \ \mathbf{v}'_{\text{dq}}(s) = \boldsymbol{T}_p(s)\begin{bmatrix} v_\alpha(s) \\ v_\beta(s) \end{bmatrix} \tag{5}$$

and

$$\mathbf{v}'_{\text{dq}}(s) = G_{\text{LPF}}(s)\mathbf{v}_{\text{dq}}(s) = \frac{\omega_c}{s+\omega_c}\mathbf{v}_{\text{dq}}(s) \tag{6}$$

where $\boldsymbol{T}_p(s)$ is the *Laplace* form of T_p shown in (4), and $G_{\text{LPF}}(s)$ is the transfer function of the first-order LPF with ω_c being the corresponding cut-off angular frequency. Then, exploiting the Euler formula and the *Laplace* property for the frequency shifting yields [4],

$$\mathbf{v}_{\alpha\beta}(s) = \begin{bmatrix} v_\alpha(s) \\ v_\beta(s) \end{bmatrix} = \begin{bmatrix} \dfrac{\omega_c s}{s^2+\omega_c s+\omega'^2} \\ \dfrac{\omega_c \omega'}{s^2+\omega_c s+\omega'^2} \end{bmatrix} v_g(s) \tag{7}$$

which indicates that the performance of the IPT-PLL system is highly dependent on the LPF, $G_{\text{LPF}}(s)$.

A design parameter of the IPT-PLL system can then be defined as $k_{\text{ipt}} = \omega_c/\omega'$. In accordance to (7), $v_g(s)$-to-$v_\alpha(s)$ and $v_g(s)$-to-$v_\beta(s)$ represent a second-order band- and low-pass filter, respectively. Consequently, the design parameter k_{ipt} should be equal to $\sqrt{2}$ in order to ensure an optimal damping of the second-order filters in terms of good settling time and overshooting in the dynamics, and accordingly the cut-off frequency ω_c of the LPF can be set. However, the design parameter k_{ipt} , may need to be tuned slightly in practice when considering the entire control system (e.g., computation delay effects). Nevertheless, the IPT PD system can ensure not only a proper deriving of the in-quadrature system ($\mathbf{v}_{\alpha\beta}$) but also a filtering of the high-order harmonics of the grid voltage (i.e., since $v_g(s)$-to-$v_\beta(s)$ behaves as a second-order LPF), resulting in a good harmonic immunity, which is in coincidence with the previous discussion.

C. Enhanced PLL (EPLL)

The basic ideas of the above two PLLs fall into the establishment of in-quadrature systems, thus enabling the Park transform to detect the phase error. Using adaptive filtering techniques is another way to the phase detection, as an adaptive filter is able to adjust the parameters automatically according to the error signal and a reference (e.g., $\cos(\theta')$) [4], [9]–[11]. The Enhanced PLL (EPLL), which was introduced in [9], is a typical representative of adaptive filtering based PLL systems. Similar principle has also been implemented in the control of the instantaneous power of a single-phase system [10].

Actually, the EPLL phase detection is achieved using an Adaptive Filter (AF) and a simple sinusoidal multiplier, as it is shown in Fig. 5, so that the EPLL can enhance the performance in contrast to a sinusoidal multiplier based PLL [8]. More specifically, the AF is used to estimate the input voltage v_g according to the detected phase error ε and the locked phase θ' (in order to generate the filter reference $\cos(\theta')$) by minimizing an objective function, e.g., $(v_g - v'_g)^2/2$. After a period, the frequency and phase of the EPLL will be free of oscillations [4].

As it can be observed in Fig. 5, the most important feature of an EPLL is that both the grid voltage amplitude V'_g and the phase θ' of the input voltage v_g can be locked. According to Fig. 5, the estimated grid voltage amplitude V'_g can be expressed as,

$$\dot{V}'_g = \mu e \cos(\theta') \tag{8}$$

in which μ is the control parameter and $e = (v_g - v'_g)$. It is also implied in (8) that the dynamic response of the EPLL

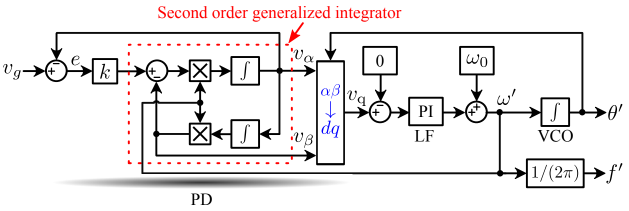

Fig. 6. Second order generalized integrator based phase locked loop system (SOGI-PLL) [7].

system depends on the speed of the estimation process (i.e., the dynamics of the adaptive filtering mechanism are controlled by μ). Simply linearizing (8) results in,

$$\frac{V_g'(s)}{V_g(s)} = \frac{1}{\tau s + 1} \tag{9}$$

which represents a simple LPF with $\tau = 2/\mu$ being its time constant. The settling time of the AF can then be approximated as $4\tau = 8/\mu$ [8], [10]. Considering the delay induced by the LF, the EPLL will present slow dynamics, and thus it is not a good solution for the applications requiring fast responses.

D. Second Order Generalized Integrator PLL (SOGI-PLL)

Actually, the AF of an EPLL system is only using one adaptive weight [4], and it will take a transient period for the error signal e to come into the zero steady-state, as it has been discussed in the last paragraph. This happens only when both the frequency and the phase of the input grid voltage v_g and the estimated grid voltage v_g' are matched. That is to say, a zero steady-state tracking of the reference signal $\cos(\theta')$ shown in Fig. 5 is achieved by the one-weight adaptive filter.

In order to further improve the performance, a second order adaptive notch filter with two adaptive weights can be a replacement of the AF in the EPLL system, and actually in that case the second order AF will act like a "generalized sinusoidal integrator". Fig. 6 shows the block diagrams of a Second Order Generalized Integrator based PLL (SOGI-PLL) system, which inherently incorporates both the sine and cosine blocks with the feedback of the detected angular frequency ω' as the AF reference [4], [7]. Then, according to Fig. 6, the in-quadrature system of the SOGI-PLL can be described by,

$$\mathbf{v}_{\alpha\beta}(s) = \begin{bmatrix} v_\alpha(s) \\ v_\beta(s) \end{bmatrix} = \begin{bmatrix} \dfrac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \\ \dfrac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \end{bmatrix} v_g(s) \tag{10}$$

which are second-order systems with k being the control parameter of the SOGI based PD system.

For the second-order systems presented in (10), the control parameter k should be equal to $\sqrt{2}$ so as to roughly achieve a good relationship between the settling time and the overshooting. Additionally, according to (10), the PD system of the SOGI-PLL exhibits like a band-pass filter (i.e., $v_g(s)$-to-$v_\alpha(s)$) and a low-pass filter (i.e., $v_g(s)$-to-$v_\beta(s)$), respectively, which is similar to that of the IPT-PLL shown in (7). Consequently, when the frequency of the input grid voltage v_g is locked by the SOGI-PLL (i.e., $\omega' = \omega$), v_α and v_β will be in-quadrature and also filtered, contributing to an improved phase detection associated by the Park transform. It can also be anticipated that the performance of the IPT-PLL and the SOGI-PLL will be similar if the control parameters (i.e., k_{ipt} and k) are designed appropriately. However, as it is shown in Fig. 6, the PD system of the SOGI-PLL has two feedback variables (ω' for the in-quadrature filtering system and θ' for the Park transform). Thus, the implementation of the SOGI-PLL is more complicated than the other three PLLs. However, it should be noted that, seen from the harmonic rejection capability, the SOGI-PLL system is a good candidate for single-phase applications in contrast with the other three.

E. Multi-Harmonic Decoupling Cell PLL (MHDC-PLL)

Although the SOGI-PLL system can minimizes the impacts from the grid voltage background distortions to some extent, inaccuracy may still occur in the case of a very weak grid, e.g. containing both low- and high-order harmonics [14], [26]. In light of this issue, the Multi-Harmonic Decoupling Cell PLL (MHDC-PLL) was introduced in [14] for single-phase applications. The structure of the MHDC-PLL system is depicted in Fig. 7, which shows that the in-quadrature system $\mathbf{v}_{\alpha\beta}$ is a combination of a $T/4$ Delay system and an IPT in-quadrature system (Figs. 3 and 4). By this mean, the MHDC-PLL system can maintain the strength of an IPT in-quadrature system to attenuate the high-order harmonics of the input grid voltage, but it also inherits the delay effect of a $T/4$ Delay system that is sensitive to frequency variations. Nonetheless, the MHDC-PLL is focused on a mitigation of the harmonic impacts on the output locked phase θ' and frequency f' with a relatively high performance in terms of fast dynamic responses. As a result, the grid current control can be enhanced.

It can be observed in Fig. 7 that the MHDC is designed in multiple synchronous reference frames ($\alpha\beta \to dq^h$) in order to cancel out the low-order harmonic effects, and i.e., the MHDC is using multiple Park transforms to dynamically extract the harmonics. Therefore, the rotational speed should be $h\omega'$ for the Park transform (i.e., $\theta^h = h\omega' t$), where h is the harmonic order. The harmonic cancellation of the MHDC can be illustrated in details as following.

If the grid voltage v_g is distorted by low-order harmonics, and thus the in-quadrature grid voltages $\mathbf{v}_{\alpha\beta}$ will inevitably contain certain low-order harmonics that are not (or cannot be) filtered out by the IPT in-quadrature system. Without loss of generality, $\mathbf{v}_{\alpha\beta}$ can be expressed as a summation of the fundamental component ($\mathbf{v}^1_{\alpha\beta}$) and each harmonic component ($\mathbf{v}^h_{\alpha\beta}$). Thus, by transforming $\mathbf{v}_{\alpha\beta}$ in any synchronous rotating frame (i.e, $dq^{n\cdot\text{sgn}(n)}$–frame rotating with the rotational speed of $n \cdot \text{sgn}(n)\omega'$), an oscillation-free term will appear due to the corresponding voltage component, and several oscillation terms will appear due to the cross-coupling effect of the rest voltage components. Therefore, the MHDC system can dynamically and accurately estimate each voltage component in

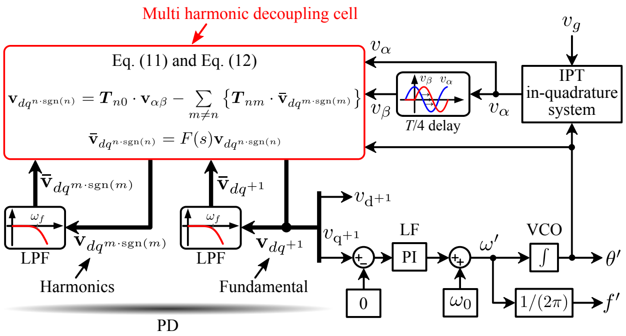

Fig. 7. Multi harmonic decoupling cell based phase locked loop system (MHDC-PLL) [14].

the corresponding $dq^{n\cdot\mathrm{sgn}(n)}$–frame by subtracting all the existing oscillation terms as,

$$\mathbf{v}_{\mathrm{dq}^{n\cdot\mathrm{sgn}(n)}} = \boldsymbol{T}_{n0} \cdot \mathbf{v}_{\alpha\beta} - \sum_{m\neq n} \left\{\boldsymbol{T}_{nm} \cdot \bar{\mathbf{v}}_{\mathrm{dq}^{m\cdot\mathrm{sgn}(m)}}\right\} \quad (11)$$

and

$$\bar{\mathbf{v}}_{\mathrm{dq}^{n\cdot\mathrm{sgn}(n)}} = F(s)\mathbf{v}_{\mathrm{dq}^{n\cdot\mathrm{sgn}(n)}} \quad (12)$$

in which $F(s)$ is the transfer function of the LPF, $\mathrm{sgn}(\cdot)$ is the sign function defining the rotational direction of the harmonic component, and $\boldsymbol{T}_{nm}$ is the Park transform matrix in the corresponding $dq^{n\cdot\mathrm{sgn}(n)}$–frame. Furthermore, the LPF $F(s)$, $\mathrm{sgn}(\cdot)$, and T_{nm} can be expressed as,

$$F(s) = \frac{\omega_f}{s+\omega_f} \quad (13)$$

with ω_f being its cut-off frequency,

$$\mathrm{sgn}(i) = \begin{cases} +1, \text{ for } i = 1,\, 5,\, 9,\, \cdots \\ 0, \quad \text{for } i = 0 \\ -1, \text{ for } i = 3,\, 7,\, 11,\, \cdots \end{cases} \quad (14)$$

and

$$\boldsymbol{T}_{nm} = \begin{bmatrix} \cos\theta_{nm} & \sin\theta_{nm} \\ -\sin\theta_{nm} & \cos\theta_{nm} \end{bmatrix} \quad (15)$$

where $\theta_{nm} = \{n\cdot\mathrm{sgn}(n) - m\cdot\mathrm{sgn}(m)\}\cdot\omega' t$. $\boldsymbol{T}_{n0}$ is the case when $m = 0$ for $\boldsymbol{T}_{nm}$ shown in (15).

Further noted in Fig. 7, the MHDC is using (11) and (12) once for the fundamental and once for each harmonic component in a decoupling cross-feedback network. Therefore, the MHDC enables the dynamically estimation of the fundamental voltage component (i.e., $\bar{\mathbf{v}}_{\mathrm{dq}^{+1}}$ that is free of any harmonic distortion). Subsequently, as it is shown in Fig. 7, the fundamental component $v_{\mathrm{q}^{+1}}$ can be used for an accurate synchronization. In respect to the parameter design of the MHDC system, there is only the cut-off frequency (i.e., ω_f) of the LPF $F(s)$, but it can affect the quality factor, the oscillation damping and the dynamic response of the MHDC recursive filter. The analysis conducted in [14] reveals that a reasonable trade-off can be achieved by setting $\omega_f = \omega_0/3$ with ω_0 being the nominal grid angular frequency as defined previously. In that case, the recursive filtering characteristic of the MHDC enables an almost-complete mitigation of the harmonic effect while maintains a fast response similar to that in the three-phase systems [26], [27]. Additionally, the cut-off frequency ω_c of the IPT system in the MHDC-PLL should be tuned according to § III.B.

It is worth mentioning that, the fast synchronization response of the MHDC-PLL is particularly desired for the proper low voltage ride-through operation of the grid-connected inverter systems [22], while the good immunity against harmonic distortion is beneficial for the power quality of the injected current [23], [27], [28]. Thus, in terms of accuracy, dynamic response and harmonic immunity, the MHDC-PLL synchronization might be a good solution for single-phase systems connected to weak grids with severe harmonic distortions, but the implementation complexity of the MHDC-PLL is increased, which is one of the drawbacks. In addition, since the $T/4$ Delay system has been employed in the MHDC-PLL system, similar to the $T/4$ Delay PLL, this further weakens the frequency adaptability of the MHDC-PLL system.

IV. Benchmarking of the Selected PLLs (Experimental Results)

A. Test-Rig Description

In order to benchmark the selected PLL synchronization methods, a 1-kW grid-connected single-phase inverter system has been built up referring to Fig. 1. Instead of an LCL-filter, an LC-filter is adopted and it is connected to a grid simulator (California Instruments MX-30) through an isolation transformer. Considering the transformer leakage inductance, an equivalent LCL filter is formed, where the capacitor voltage is measured for synchronization. Since a commercial DC source was used, the outer control loop is not necessary. Instead, the current reference I_g^* is set in the control system by commanding the active power reference, i.e., $I_g^* = 2P_{\mathrm{n}}^*/V_g$. A Proportional Resonant (PR) controller $G_{\mathrm{PR}}(s)$ with Harmonic Compensators (HC) $G_{\mathrm{HC}}(s)$ is adopted as the current controller $G_{\mathrm{CC}}(s)$ [1], and it can be expressed as,

$$G_{\mathrm{CC}}(s) = \underbrace{k_{\mathrm{pr}} + \frac{k_{\mathrm{r}}s}{s^2+\omega_0^2}}_{G_{\mathrm{PR}}(s)} + \underbrace{\sum_{h=3,\,5,\,7} \frac{k_{\mathrm{r}}^h s}{s^2+(h\omega_0)^2}}_{G_{\mathrm{HC}}(s)} \quad (16)$$

where k_{pr} is the proportional control gain, k_{r} is the resonant control gain, and k_{r}^h is the resonant control gain of the HC with h being the harmonic order. All the PLLs and the entire current control system were implemented in a dSPACE DS 1103 system. The system parameters are listed in Table I. The current controller and the LF parameters are designed as shown in Table II. For a fair comparison, the parameters of the LF (i.e., the PI controller) are the same for all the selected PLL systems as shown in Table II, while the control parameters for the PD systems as shown in Table III are designed according to the discussions in § III for an optimal performance. Fig. 8 shows the experimental system layout and the detailed current control system.

B. Experimental Results

The five selected PLL candidates were tested firstly under a normal grid condition (Total Harmonic Distortion,

TABLE I
PARAMETERS OF THE SINGLE-PHASE GRID-CONNECTED SYSTEM.

Parameter	Symbol	Value
Rated power	P_n^*	1 kW
DC-link voltage	V_dc	450 V
Grid voltage amplitude	V_g	$230\times\sqrt{2}$ V
Grid nominal frequency	ω_0	$2\pi\times 50$ rad/s
DC-link capacitor	C_dc	1100 μF
LC filter	L_1	3.6 mH
	C_f	2.35 μF
Transformer leakage inductance	L_g	4 mH
Sampling frequency	f_s	10 kHz
Switching frequency	f_sw	10 kHz

TABLE II
CURRENT CONTROLLER AND LOOP FILTER PARAMETERS.

Controller	Symbol	Value
PLL loop filter (PI)	k_p	0.283
	k_i	5.663
PR controller	k_pr	22
	k_r	1300
HC controller	$k_\mathrm{r}^{3,\,5}$	1000
	k_r^{7}	600

TABLE III
PARAMETERS OF THE PHASE DETECTOR SYSTEMS OF THE SELECTED SINGLE-PHASE PLLS.

PLL	Symbol	Value
IPT-PLL	k_ipt	1.4
EPLL	τ	8 ms
SOGI-PLL	k	1.4
MHDC-PLL	$^*\omega_c$	$2\pi\times 50\times\sqrt{2}$ rad/s
	ω_f	$2\pi\times 50/3$ rad/s

* LPF cut-off freq. in the IPT in-quadrature system.

$\mathrm{THD}_{v_g}\approx 0.71\%$), and the experimental results are presented in Fig. 9, where the frequency error $\Delta f = f' - 50$ and v_d error $\Delta v_\mathrm{d} = v_\mathrm{d} - 1$ (or $v_\mathrm{d}' - 1$). Since the capacitor voltage is measured as the grid voltage v_g for synchronization which thus contains switching frequency harmonics, it is observed in Fig. 9 that the outputs of both the $T/4$ Delay PLL and the EPLL consist of high-order harmonics. This indicates the poor harmonic immunity of the $T/4$ Delay PLL and the EPLL systems. Moreover, the $T/4$ Delay PLL is more sensitive to the harmonics, as its in-quadrature system is based on a quarter phase delay of the input voltage, thus inevitably inheriting the harmonics. As a result, in the case of grid-connected applications using the $T/4$ Delay PLL or the EPLL, a LPF may be required and should be incorporated at point "A" shown in Fig. 8(b), which however can affect the dynamics of the entire system. In contrast, the IPT-PLL, the SOGI-PLL, and the MHDC-PLL are all good at eliminating these switching harmonics due to the presence of the low pass filters or the adaptive notch filter.

However, in the case of a very weak grid which contains not only low-order but also high-order harmonics, the PLL systems will be challenged. Fig. 10 further benchmarks the dynamic performances of the selected PLL methods

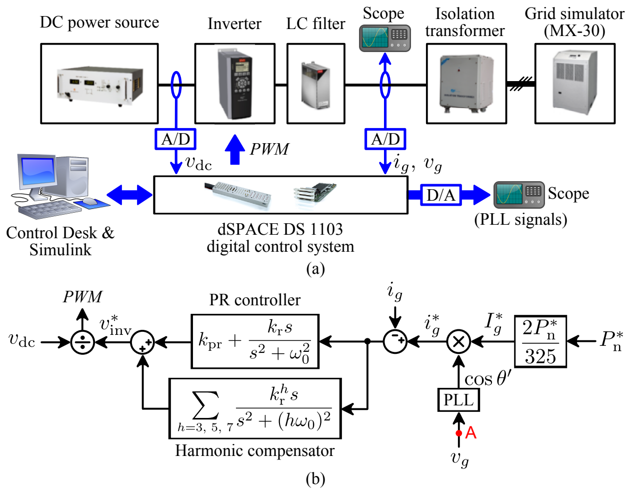

Fig. 8. Experimental setup of a 1-kW single-phase grid-connected system: (a) dSPACE platform and (b) current control system.

when the grid voltage experiences several disturbances. The harmonic sensitivity of the $T/4$ Delay PLL and the EPLL is clearly verified by the results shown in Fig. 10(a), where it also shows that the IPT-PLL and the SOGI-PLL are slightly affected by the low order harmonics of the grid voltage. In contrast, it can be observed in Fig. 10(a) that the estimated output frequency of the MHDC-PLL system is free of oscillations after a short period of transient. This means that the MHDC-PLL is significantly immune to the harmonics in the grid voltage.

Moreover, it can be observed in Figs. 9 and 10 that the performances of the IPT-PLL and the SOGI-PLL systems are quite alike, since the in-quadrature systems of both PLLs have similar filtering capability (i.e., $\mathbf{v}_{\alpha\beta}$-to-v_g) according to (7) and (10). In addition, as it is shown in Fig. 10 (c), the $T/4$ Delay PLL and the MHDC-PLL systems present poor synchronization performances in the case of grid frequency variations, which may occur especially in the micro grid systems due to an injection of a large amount of fluctuating power, e.g., PV and/or wind power. This poor frequency adaptability is because of the adoption of the delay unit with a constant duration for the in-quadrature systems. Nevertheless, the two PLLs present fast dynamics. For the MHDC-PLL, the dynamics are even comparable with the IPT-PLL and the SOGI-PLL in terms of a fast response and a small overshooting, as it is verified by Fig. 10(b) and (d). In all, the test results are in close agreement with the discussions in § III.

In addition to the above verification, a comparison between the SOGI-PLL and the MHDC-PLL has also been conducted with a programmed background distortion of the grid voltage (i.e., THD_{v_g} = 2.91%). In this case study, the HC is disabled in order to compare how the PLL synchronization will impact the injected grid current quality. The experimental results are demonstrated in Fig. 11. It can be seen in Fig. 11 that, if the MHDC-PLL system is adopted as the synchronization, the grid current THD_{i_g} is slightly reduced in contrast to the case when the SOGI-PLL is used. Actually, when looking at the

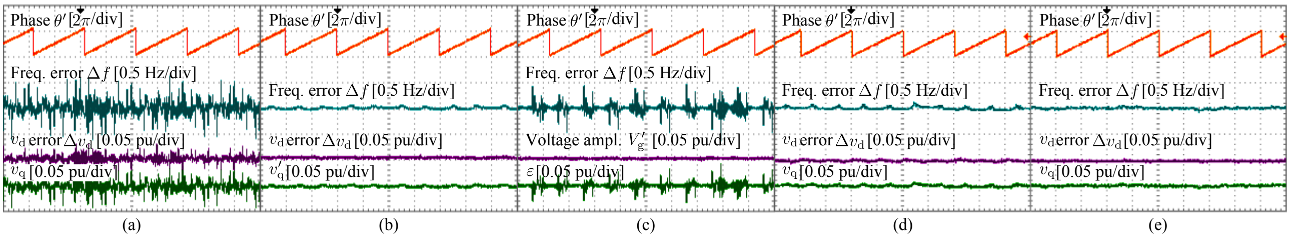

Fig. 9. Steady-state performance of the selected PLL synchronization methods under a nominal grid condition (time [10 ms/div]): (a) $T/4$ Delay PLL, (b) IPT-PLL, (c) EPLL, (d) SOGI-PLL, and (e) MHDC-PLL.

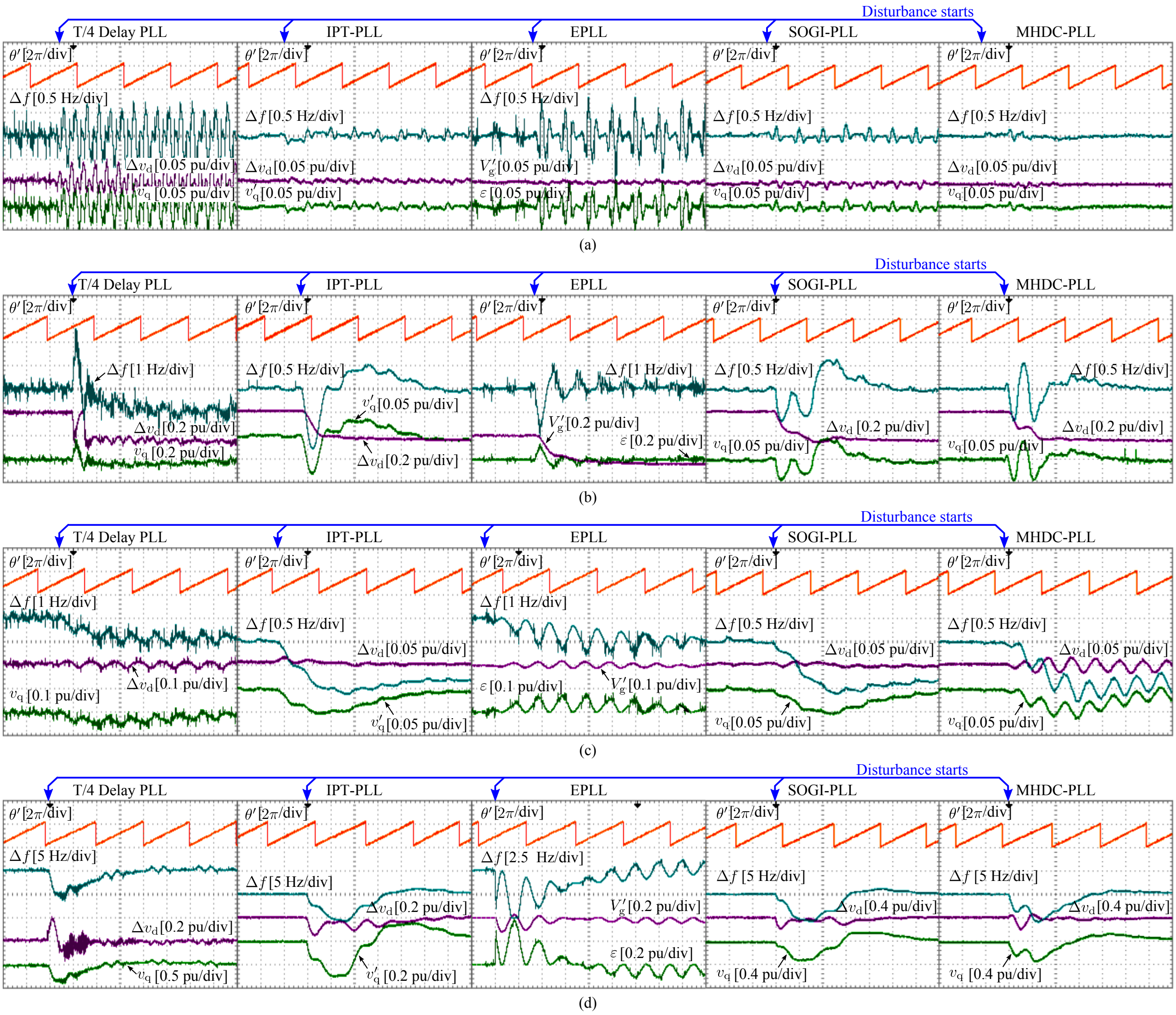

Fig. 10. Dynamic responses of the selected PLL synchronization methods under various grid disturbances (time [10 ms/div]): (a) harmonics (THD_{v_g} changes from 0.71% to 2.91%), (b) voltage sag ($V_g = 0.75$ pu), (c) frequency jump (-0.8 Hz), and (d) phase shift ($-30°$).

individual low-order harmonics, the same conclusion can be reached. For example, the Root Mean Square (RMS) value of the 7$^{\text{th}}$ harmonic is 112 mA when the grid current is synchronized through the SOGI-PLL system, while the 7$^{\text{th}}$ harmonic of 106 mA is achieved using the MHDC-PLL system. The experimental results have demonstrated that the synchronization will affect the entire control systems as mentioned in § I. It should be emphasized that efforts can be devoted to the advancement of synchronization methods in order to achieve a better current injection from the grid-connected inverter systems.

V. Conclusion

In this paper, a benchmarking of the most popular PLL methods (i.e., T/4 Delay PLL, EPLL, IPT-PLL, SOGI-PLL, and MHDC-PLL) for single-phase grid-connected systems has been presented. Benchmarks include the accuracy, the transient response, the harmonic immunity under

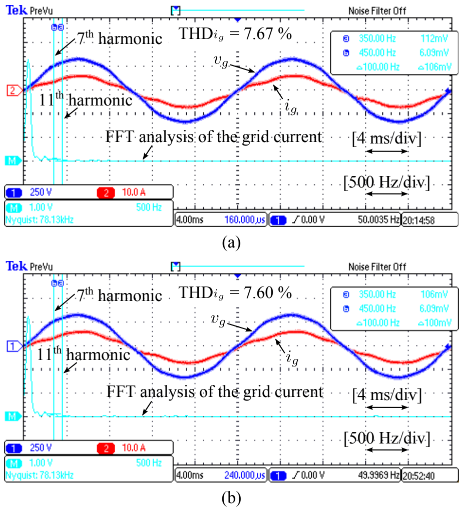

Fig. 11. Experimental results of a 1-kW single-phase grid-connected system with different PLL systems (CH1 - grid voltage v_g [250 V/div], CH2 - grid current i_g [10 A/div], CH M - FFT analysis of the grid current [1 A/div]): (a) SOGI-PLL system and (b) MHDC-PLL.

grid disturbances, and the implementation complexity. As a result, the benchmarking results provide a flexibility to choose an appropriate PLL-based synchronization technique according to a specific application. For example, the SOGI-PLL is suitable for fault ride-through operations in terms of high accuracy and a fast response speed. In contrast, the MHDC-PLL also with fast dynamic responses is good for use in a weak grid that is distorted by non-linear loads , while its performance is poor in response to grid frequency variations due to the T/4 delay mechanism. Experimental tests on a single-phase grid-connected system have supportively verified the benchmarking.

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