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# Small-Signal Modeling, Analysis and Testing of Parallel Three-Phase-Inverters with A Novel Autonomous Current Sharing Controller

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**Abstract**—A novel simple and effective autonomous current-sharing controller for parallel three-phase inverters is employed in this paper. The novel controller is able to endow to the system high speed response and precision in contrast to the conventional droop control as it does not require calculating any active or reactive power, instead it uses a virtual impedance loop and a SFR phase-locked loop. The small-signal model of the system was developed for the autonomous operation of inverter-based microgrid with the proposed controller. The developed model shows large stability margin and fast transient response of the system. This model can help identifying the origin of each of the modes and possible feedback signals for design of controllers to improve the system stability. Experimental results from two parallel 2.2 kVA inverters verify the effectiveness of the novel control approach.

**Keywords**—three-phase parallel inverters; modeling; autonomous current control

## I. INTRODUCTION

In microgrids, droop control method has been dominated the autonomous control of parallel inverters in the last decade [1], [2]. Although this technique only needs local information to operate, it presented a number of problems that were solved along the literature [3]-[9].

The first one is that the droop coefficients that regulate frequency and amplitudes are basically proportional terms, so that in order to increase their range of values, derivative terms were added [3]-[5]. The second one is that frequency and voltage are respectively related to active and reactive power when the output impedance of the generator is mainly inductive, however in an inverter the output impedance can be fixed by means of virtual impedance [6], [7]. The third one is that in case of resistive lines/virtual impedances, active power is controlled by the inverter voltage amplitude, while the reactive power flow is dominated by the angle [8], [9].

Based on these three improvements, a control architecture based on a virtual resistance,  $P$ - $V$  and  $Q$ - $f$  droops can be used to deal with the autonomous control of parallel connected inverters [8], [10]. The stability of autonomous micro-grids is a critical issue considering the low-inertia nature of such inverter dominated systems. Small-signal-based stability analysis has

been reported in [4], [11]-[15] to study the stability of the autonomous droop-controlled microgrid system. However, power droop control has the inherent drawback that it needs to calculate instantaneous active and reactive powers and then average through low pass filters, whose bandwidth may impact the transient response of the system [6], [13], [16]. To cope with these problems, a simpler and faster controller is proposed in this paper, which consists of a phase-locked loop (PLL) and a virtual resistance loop that will provide for both instantaneous current sharing and fast dynamic response of the paralleled inverter system. A small signal model is developed in order to analyze the system stability and its modes. Simulation and experimental results are presented to evaluate the feasibility of the novel approach.

## II. CONTROL STRUCTURE AND PRINCIPLE

Fig. 1 shows the power stage of an inverter which consists of a three-leg three-phase inverter connected to a DC link, loaded by an  $LC$  filter, and connected to the AC bus. The controller includes a synchronous reference frame-based phase locked loop (SRF-PLL) which substitutes the two loops droop control, a virtual resistance loop ( $R_{vir}$ ), a DC link voltage feed-forward loop, and the conventional PR inner current and voltage loops ( $G_i$  and  $G_v$ ) that generates a PWM signal to drive the IGBTs the inverter. Capacitor currents and voltages are transformed to the stationary reference frame ( $i_{ca\beta}$  and  $v_{ca\beta}$ ).

The voltage reference  $v_o^*$  is generated by using the amplitude reference ( $|v_o^*|$ ) and the phase generated by a SRF-PLL. The PLL has the objective to synchronize all the inverters near to the same frequency ( $\omega^*$ ). Even though the PLL is trying to synchronize the inverter with the common AC bus, in case of supplying reactive loads, the current flowing through the virtual resistance will create unavoidable voltage drop that will cause an increase of frequency in the PLL. This way the mechanism inherently endows an droop characteristic in each inverter.

Thus, the relationship between  $I_{o\alpha}$ ,  $I_{o\beta}$  and  $R_{vir}$  can be generalized and expressed for a number  $N$  of converters as[17]

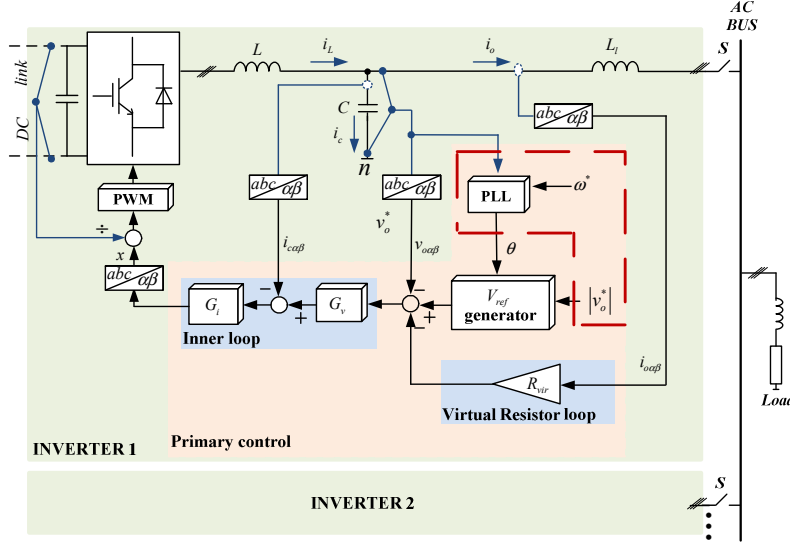


Fig. 1. Control structure of the proposed control method.

$$I_{o\alpha 1} R_{vir1} = I_{o\alpha 2} R_{vir2} = \dots = I_{o\alpha N} R_{virN} \quad (1)$$

$$I_{o\beta 1} R_{vir1} = I_{o\beta 2} R_{vir2} = \dots = I_{o\beta N} R_{virN} \quad (2)$$

The output  $\alpha$  and  $\beta$  axis output currents of paralleled inverters are inversely proportional to their virtual resistances. It can be easily observed that current sharing performance is just influenced by the output impedance ratio instead of the output impedance value of the two inverter modules.

### III. SMALL SIGNAL MODEL

In order to analysis the stability and parameters sensitivity, the small-signal model of the inverters with the proposed controller has been developed in this paper. Each inverter is modeled on its individual reference frame whose rotation frequency is set by its PLL. The inverter model includes the reference voltage generation dynamics, voltage and current controller dynamics,  $LC$  filter dynamics, line impedance dynamics and PLL dynamics. In order to get the equilibrium point, the small-signal model should be developed in the synchronous rotating reference frame. Note that the proportional + resonant (PR) controllers which are used in voltage control loop in stationary reference frame should also be transferred to the synchronous reference frame to keep its frequency characteristic. In the following sub-sections the internal modeling is discussed in more detail.

#### A. Voltage reference generation and virtual impedance

As mentioned above, in the proposed controller, the voltage reference  $v_o^*$  is generated by using the amplitude reference ( $|v_o^*|$ ) and the phase generated by a SRF-PLL. And then, the voltage reference  $v_o^*$  is modified by the virtual impedance loop which feedback the product of the virtual resistance with their corresponding output current components. In droop-controlled

parallel inverters, virtual impedance loop has also been added to the voltage reference in order to fix the output impedance of the voltage source inverter (VSI) and to compensate the differences of line impedances for parallel inverters. Beside these, the most important functionality of the virtual resistors here is to determine the load sharing ratio of the paralleled inverters. The modified voltage references which are generated in stationary reference frame which can be easily transferred to the synchronous reference frame can be expressed in dq-coordinates as follows:

$$\begin{aligned} v_{od}^{*'} &= v_{od}^* - R_{vir} i_{od} \\ v_{oq}^{*'} &= v_{oq}^* - R_{vir} i_{oq} \end{aligned} \quad (3)$$

The algebraic equations of voltage reference generation can be expressed as:

$$[\Delta v_{odq}^{*'}] = C_{gen} [\Delta v_{odq}^*] - D_{gen} [\Delta i_{odq}] \quad (4)$$

Where

$$C_{gen} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}, \quad D_{gen} = \begin{bmatrix} R_{vir} & 0 \\ 0 & R_{vir} \end{bmatrix} \quad (5)$$

#### B. Voltage loop controller

The inner voltage loop controller is based on a PR structure in stationary reference frame, where generalized integrators are used to achieve zero steady-state error. Based on the  $abc / \alpha\beta$  - coordinate transformation principle, a three-phase system can be modeled in two independent single-phase systems. In order to integrate the entire system, the PR controller needs to be transferred to the synchronous reference frame to maintain its

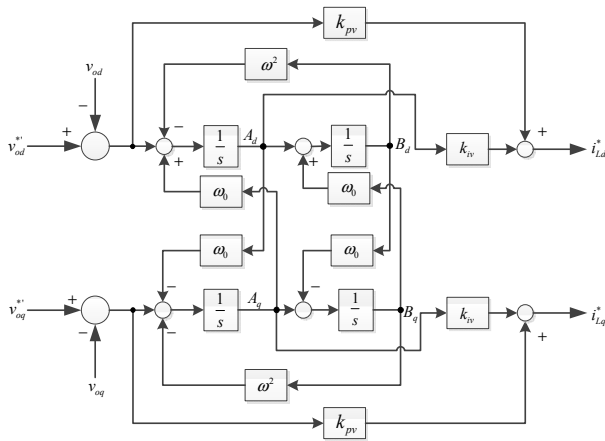


Fig. 2. Voltage PR controller in dq frame

frequency characteristic which will make sure the inverter operating at the zero crossing point in the bode diagrams of the PR controller.

Fig. 2 shows the voltage controller block diagram in synchronous reference frame including all feed-back and feed-forward terms.

It can be seen that there are four states  $A_{dq}$  and  $B_{dq}$  in Fig. 2. The corresponding state equations can be expressed as:

$$\begin{aligned} \frac{dA_d}{dt} &= (v_d^* - v_d) + \omega_0^2 B_d + \omega_0 A_q \\ \frac{dA_q}{dt} &= (v_q^* - v_q) - \omega_0^2 B_q - \omega_0 A_d \end{aligned} \quad (6)$$

The variable  $A_{dq}$  and  $B_{dq}$  do not have any particular physical meanings but they are states to develop the state-space model.

$$\begin{aligned} \frac{dB_d}{dt} &= A_d + \omega_0 B_q \\ \frac{dB_q}{dt} &= A_q - \omega_0 B_d \end{aligned} \quad (7)$$

As well as the algebraic equations

$$\begin{aligned} i_{Ld}^* &= K_{pv} (v_d^* - v_d) + K_{iv} B_d \\ i_{Lq}^* &= K_{pv} (v_q^* - v_q) + K_{iv} B_q \end{aligned} \quad (8)$$

The linearized small-signal state-space models of the voltage loop controller are presented in (9) to (12).

$$\begin{bmatrix} \Delta \dot{A}_{dq} \\ \Delta \dot{B}_{dq} \end{bmatrix} = A_{vol} \begin{bmatrix} \Delta A_{dq} \\ \Delta B_{dq} \end{bmatrix} + B_{vol1} [\Delta v_{odq}^*] + B_{vol2} \begin{bmatrix} \Delta i_{Ldq} \\ \Delta v_{odq} \end{bmatrix} \quad (9)$$

Where

$$A_{vol} = \begin{bmatrix} 0 & \omega_0 & -\omega_0^2 & 0 \\ -\omega_0 & 0 & 0 & -\omega_0^2 \\ 1 & 0 & 0 & \omega_0 \\ 0 & 1 & -\omega_0 & 0 \end{bmatrix}, \quad B_{vol1} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad (10)$$

$$B_{vol2} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix}$$

$$[\Delta i_{Ldq}^*] = C_{vol} \begin{bmatrix} \Delta A_{dq} \\ \Delta B_{dq} \end{bmatrix} + D_{vol1} [\Delta v_{odq}^*] + D_{vol2} \begin{bmatrix} \Delta i_{Ldq} \\ \Delta v_{odq} \end{bmatrix} \quad (11)$$

Where

$$\begin{aligned} C_{vol} &= \begin{bmatrix} 0 & 0 & K_{iv} & 0 \\ 0 & 0 & 0 & K_{iv} \end{bmatrix}, \quad D_{vol1} = \begin{bmatrix} K_{pv} & 0 \\ 0 & K_{pv} \end{bmatrix}, \\ D_{vol2} &= \begin{bmatrix} 0 & 0 & -K_{pv} & 0 \\ 0 & 0 & 0 & -K_{pv} \end{bmatrix} \end{aligned} \quad (12)$$

### C. Current loop controller

The inner current loop controller is based on a proportional structure in stationary reference frame as shown in Fig. 3.

The algebraic equations of current loop controller can be expressed as:

$$\begin{aligned} v_{PWMd}^* &= K_{pi} (i_{Ld}^* - i_{Ld}) \\ v_{PWMq}^* &= K_{pi} (i_{Lq}^* - i_{Lq}) \end{aligned} \quad (13)$$

The linearized small-signal state-space models of the voltage loop controller are presented in (14) to (16).

$$[\Delta v_{PWMdq}^*] = D_{cur1} [\Delta i_{Ldq}^*] + D_{cur2} \begin{bmatrix} \Delta i_{Ldq} \\ \Delta v_{odq} \end{bmatrix} \quad (14)$$

Where

$$D_{cur1} = \begin{bmatrix} K_{pi} & 0 \\ 0 & K_{pi} \end{bmatrix}, \quad D_{cur2} = \begin{bmatrix} -K_{pi} & 0 & 0 & 0 \\ 0 & -K_{pi} & 0 & 0 \end{bmatrix} \quad (15)$$

Based on (11) and (14), the output of current loop controller  $\Delta v_{PWMdq}^*$  can be derived as follows:

$$\begin{aligned} [\Delta v_{PWMdq}^*] &= D_{cur1} C_{vol} \begin{bmatrix} \Delta A_{dq} \\ \Delta B_{dq} \end{bmatrix} + D_{cur1} D_{vol1} [\Delta v_{odq}^*] \\ &\quad + (D_{cur1} D_{vol2} + D_{cur2}) \begin{bmatrix} \Delta i_{Ldq} \\ \Delta v_{odq} \end{bmatrix} \end{aligned} \quad (16)$$

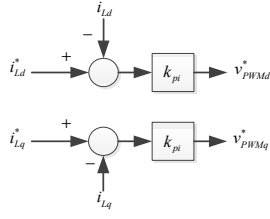


Fig. 3. Current loop controller

#### D. Three-phase half-bridge circuit and output LC filter

The structure of three-phase half-bridge circuit and output LC filter is shown in Fig. 4. Here, the three-phase half-bridge circuit is equivalent to a voltage gain  $K_{PWM}$ . The corresponding state equations can be expressed as:

$$\begin{aligned}\frac{di_{Ld}}{dt} &= -r/L i_{Ld} + \omega_0 i_{Lq} + K_{PWM}/L v_{PWMd}^* - 1/L v_{od} \\ \frac{di_{Lq}}{dt} &= -r/L i_{Lq} - \omega_0 i_{Ld} + K_{PWM}/L v_{PWMq}^* - 1/L v_{oq} \\ \frac{dv_{od}}{dt} &= \omega_0 v_{oq} + 1/C i_{Ld} - 1/C i_{od} \\ \frac{dv_{oq}}{dt} &= -\omega_0 v_{od} + 1/C i_{Lq} - 1/C i_{oq}\end{aligned}\quad (17)$$

The output variables of the LC filter are the state variables  $v_{odq}$ . The following equations represent the linearized small-signal state-space models of the three-phase half-bridge circuit and output LC filter at the equilibrium point.

$$\begin{bmatrix} \Delta \dot{i}_{Ldq} \\ \Delta \dot{v}_{odq} \end{bmatrix} = A_{LC} \begin{bmatrix} \Delta i_{Ldq} \\ \Delta v_{odq} \end{bmatrix} + B_{LC1} [\Delta v_{PWMdq}^*] + B_{LC2} [\Delta i_{odq}] \quad (18)$$

$$\begin{aligned}A_{LC} &= \begin{bmatrix} -r/L & \omega_0 & -1/L & 0 \\ -\omega_0 & -r/L & 0 & -1/L \\ 1/C & 0 & 0 & \omega_0 \\ 0 & 1/C & -\omega_0 & 0 \end{bmatrix}, \\ B_{LC1} &= \begin{bmatrix} K_{PWM}/L & 0 \\ 0 & K_{PWM}/L \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, B_{LC2} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ -1/C & 0 \\ 0 & -1/C \end{bmatrix}\end{aligned}\quad (19)$$

In (18), the output of current loop controller  $\Delta v_{PWMdq}^*$  can be substituted by (16), then the (18) can be expressed as:

$$\begin{aligned}\begin{bmatrix} \Delta \dot{i}_{Ldq} \\ \Delta \dot{v}_{odq} \end{bmatrix} &= A_{LC} \begin{bmatrix} \Delta i_{Ldq} \\ \Delta v_{odq} \end{bmatrix} + B_{LC1} D_{cur1} C_{vol} \begin{bmatrix} \Delta A_{dq} \\ \Delta B_{dq} \end{bmatrix} \\ &+ B_{LC1} D_{cur1} D_{vol1} [\Delta v_{odq}^*] \\ &+ B_{LC1} (D_{cur1} D_{vol2} + D_{cur2}) \begin{bmatrix} \Delta i_{Ldq} \\ \Delta v_{odq} \end{bmatrix} + B_{LC2} [\Delta i_{odq}]\end{aligned}\quad (20)$$

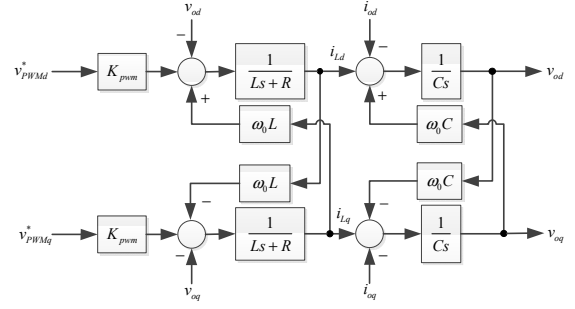


Fig. 4. Equivalent three-phase half-bridge circuit and LC filter

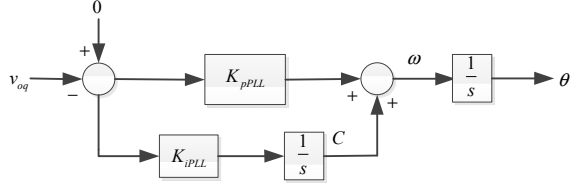


Fig. 5. PLL model

#### E. Line impedance

The line impedance is quite small as there are only cables between each inverter and common bus. The virtual impedances which are equivalent to series connection with the line impedance in this control strategy dominate the  $R/X$  ratio. Only the real line impedance is considered here, since the virtual impedances are already modeled in part A.

The corresponding state equations can be expressed as:

$$\begin{aligned}\frac{di_{od}}{dt} &= -r_i/L_i i_{od} + \omega_0 i_{oq} + 1/L_i v_{od} - 1/L_i v_{busd} \\ \frac{di_{oq}}{dt} &= -r_i/L_i i_{oq} - \omega_0 i_{od} + 1/L_i v_{oq} - 1/L_i v_{busq}\end{aligned}\quad (21)$$

The output variables of the line impedance are the state variables  $i_{odq}$ . The linearized small-signal state-space models are as follows.

$$\begin{bmatrix} \Delta \dot{i}_{odq} \end{bmatrix} = A_l \begin{bmatrix} \Delta i_{odq} \end{bmatrix} + B_{l1} \begin{bmatrix} \Delta i_{Ldq} \\ \Delta v_{odq} \end{bmatrix} + B_{l2} [\Delta v_{busdq}] \quad (22)$$

$$\begin{aligned}A_l &= \begin{bmatrix} -r_i/L_i & \omega_0 \\ -\omega_0 & -r_i/L_i \end{bmatrix}, \\ B_{l1} &= \begin{bmatrix} 0 & 0 & 1/L_i & 0 \\ 0 & 0 & 0 & 1/L_i \end{bmatrix}, B_{l2} = \begin{bmatrix} -1/L_i & 0 \\ 0 & -1/L_i \end{bmatrix}\end{aligned}\quad (23)$$

#### F. Phase locked loop (PLL)

The SRF-PLL is an important control loop in this proposed controller. Even though the PLL is trying to synchronize the inverter with the common AC bus, in case of supplying reactive loads, the current flowing through the virtual

resistance will create unavoidable voltage drop that will cause an increase of frequency in the PLL. This way the mechanism inherently endows an  $I_{o\beta} - \omega$  droop characteristic to each inverter. A detailed block diagram of the SRF-PLL is shown in Fig. 5.

The corresponding state equations can be expressed as:

$$\begin{aligned} \frac{dC}{dt} &= -K_{iPLL} v_{oq} \\ \frac{d\theta}{dt} &= \omega = C - K_{pPLL} v_{oq} \end{aligned} \quad (24)$$

The variable  $C$  does not have a particular physical meaning but it is a state to facilitate the development of the state-space model. The linearized small-signal model of PLL are given by

$$\begin{bmatrix} \Delta \dot{C} \\ \Delta \dot{\theta} \end{bmatrix} = A_{PLL} \begin{bmatrix} \Delta C \\ \Delta \theta \end{bmatrix} + B_{PLL} \begin{bmatrix} \Delta v_{odq} \\ \Delta i_{Ldq} \end{bmatrix} \quad (25)$$

Where

$$A_{PLL} = \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix}, \quad B_{PLL} = \begin{bmatrix} 0 & -K_{iPLL} & 0 & 0 & 0 & 0 \\ 0 & -K_{pPLL} & 0 & 0 & 0 & 0 \end{bmatrix} \quad (26)$$

#### G. Combined inverter model

A complete state-space small-signal model of the inverter can be obtained by combining the state-space models of the voltage reference generator, voltage controller, current controller, output  $LC$  filter, line impedance and PLL, given by (4), (9), (18), (22) and (25). There are totally 10 states in each individual inverter model.

$$\begin{bmatrix} \Delta \dot{x} \end{bmatrix} = A \begin{bmatrix} \Delta x \end{bmatrix} + B_1 \begin{bmatrix} \Delta v_{odq}^* \end{bmatrix} + B_2 \begin{bmatrix} \Delta v_{busdq} \end{bmatrix} \quad (27)$$

Where

$$\Delta x = \begin{bmatrix} \Delta A_{dq} & \Delta B_{dq} & \Delta i_{Ldq} & \Delta v_{odq} & \Delta i_{odq} & \Delta C & \Delta \theta \end{bmatrix}^T \quad (28)$$

The (29) are shown at the bottom of the page.

#### IV. STABILITY ANALYSIS BASED ON ROOT LOCUS

In this section, stability and sensitivity analysis are conducted to understand the parametric influences on the stability and dynamic performance of the DG system equipped

with the proposed controller. The study is based on the eigenvalue analysis of the developed system state space models. Three factors are investigated in this paper: the virtual resistor, the proportional parameter of voltage loop controller, and the proportional parameter of current loop controller. The system parameters for the base case are presented in Table I.

Figs. 6 shows the trajectories of the modes in function of the virtual resistance values  $R_{vir}$ . Notice that this system has six roots: four conjugated poles and two real pole. The arrows indicate the evolution of the corresponding pole when the coefficient increases.

It can be seen that when the parameters increasing, the complex poles become dominant, resulting in a near second order behavior. But it also can be seen that the low sensibility of virtual impedance value over the system dynamics, through the smaller movement of eigenvalues during the large increments of  $R_{vir}$ .

Since in both cases the poles remain in the left half-plane in the reasonable virtual impedance value range, the system is stable in the range of concern. As above mentioned, by adjusting the virtual resistances, the current-sharing ratio can be fixed, while they have negligible impact on system stability.

Fig. 7 shows that when the parameter  $K_{pv}$  of the voltage loop PR controller increases, the dominant modes which are in cluster C move apart from real axis. The modes in clusters A and B move toward real axis which will deteriorate the system stability if the parameter  $K_{pv}$  continuously increasing.

Fig. 8 shows that when the parameter  $K_{pi}$  of the current loop P controller increases, the dominant modes which are in cluster C move apart from real axis. The modes in clusters A and B move toward real axis and show low sensibility of parameter  $K_{pi}$  over the system dynamics, through the smaller movement of eigenvalues during the increments of  $K_{pi}$ .

TABLE I. SYSTEM PARAMETERS

Parameters	Values	Parameters	Values
$U_{dc}$	650V	$ v_o^* $	320V
$L$	1.8mH	$C$	9uF
$R_{vir}$	2 $\Omega$	$\omega_0$	314rad/s
$K_{pv}$	0.053	$K_{iv}$	3.24
$K_{pi}$	0.603	$K_{iPLL}$	20000
$K_{pPLL}$	314.14		

$$A = \begin{bmatrix} A_{vol} & B_{vol2} & -B_{vol1}D_{gen} & 0 \\ B_{LC1}D_{cur1}C_{vol} & A_{LC} + B_{LC1}(D_{cur1}D_{vol2} + D_{cur2}) & B_{LC2} - B_{LC1}D_{cur1}D_{vol1}D_{gen} & 0 \\ 0 & B_{I1} & A_I & 0 \\ 0 & B_{PLL} & 0 & A_{PLL} \end{bmatrix}, B_1 = \begin{bmatrix} B_{vol1}C_{gen} \\ B_{LC1}D_{cur1}D_{vol1}C_{gen} \\ 0 \\ 0 \end{bmatrix}, B_2 = \begin{bmatrix} 0 \\ 0 \\ B_{I2} \\ 0 \end{bmatrix} \quad (29)$$

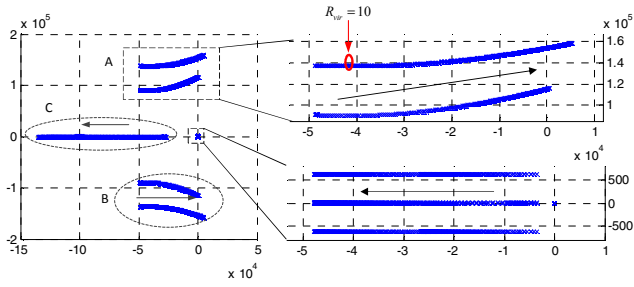


Fig. 6. Trace of nodes as function of  $0.1 \leq R_{vir} \leq 100$ .

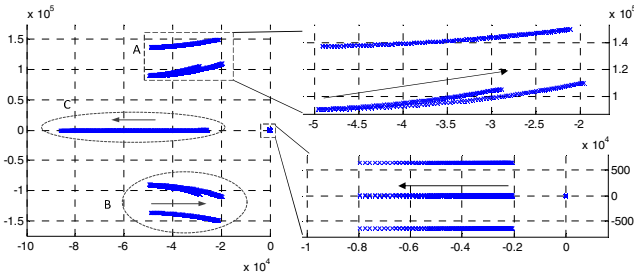


Fig. 7. Trace of nodes as function of  $0.01 \leq K_{pi} \leq 1$ .

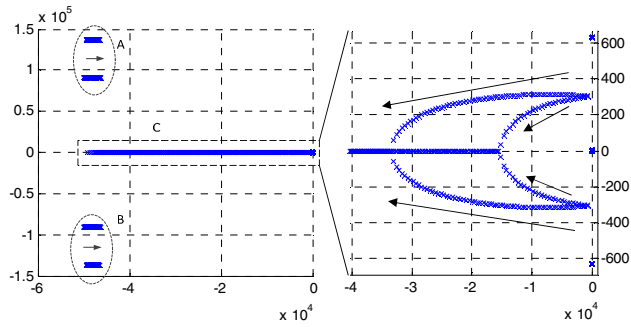


Fig. 8. Trace of nodes as function of  $0.01 \leq K_{pi} \leq 1$ .

## V. EXPERIMENTAL RESULTS

In order to verify the effectiveness of the proposed controller and its stability, a scale-down laboratory prototype is built according to Fig.1. The experimental setup consists of two Danfoss 2.2 kW inverters, a dSPACE1006 control board, LC filters, LEM sensors and two resistive loads, as shown in Fig.9. The electrical setup and control system parameters are listed in Table I.

Fig. 10 shows the experimental results of the paralleled inverter system when sharing a resistive load by using the proposed control scheme. In this case, the virtual resistance ( $R_{vir}$ ) ratio is suddenly changed from 2:1 to 1:1 and then back to 2:1. It can be seen that after about 140ms, the direct currents can be precisely controlled according to the ratio of their virtual resistances. Notice the smooth and fast transient response of the currents. Here, the active power and reactive power which do not participate in the control loop are only for observing.

Fig. 11 shows the transient response of the paralleled inverter system employing the novel controller during suddenly

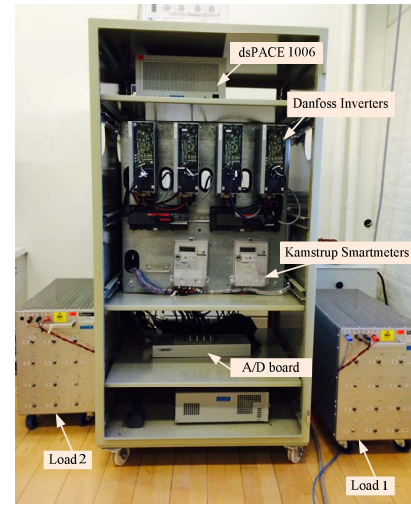
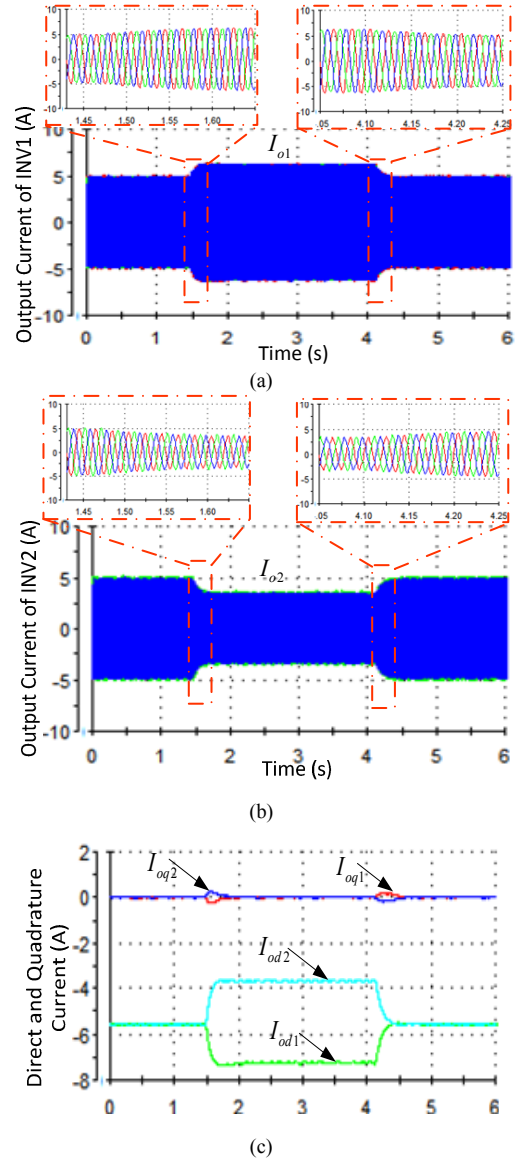
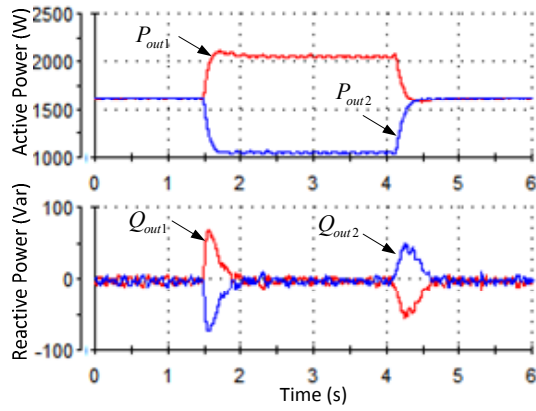


Fig. 9. Experimental setup.



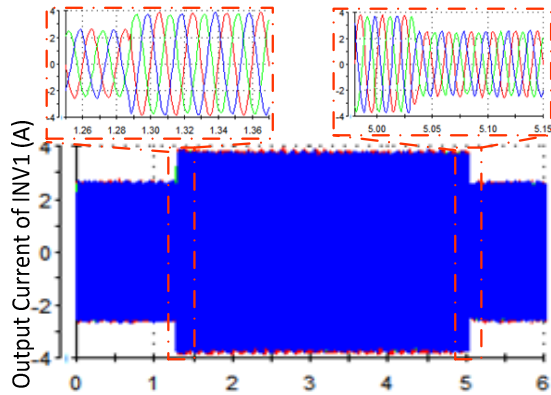




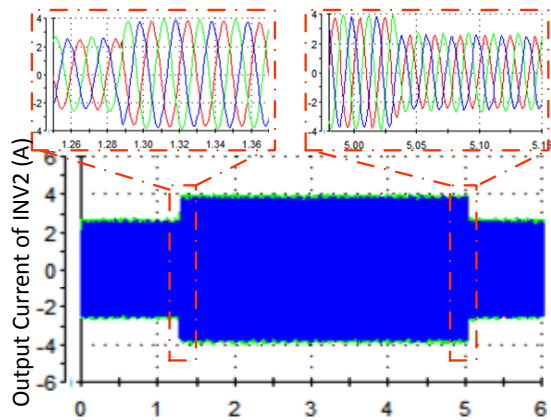
(d)

Fig. 10. Transient response of paralleled inverters sharing resistive load during the virtual resistance ratio changing. (a) output currents of inverter#1, (b) output currents of inverter#1, (c) output direct and quadrature currents of inverter#1, #2, (d) active and reactive power of inverter#1, #2.

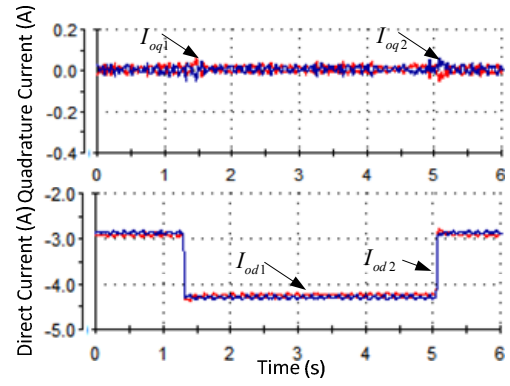
770W load step changes (from 5.6A to 8A and back to 5.6A). It can be observed the fast transient response of the system during load step changes, while maintaining precisely current sharing performances.



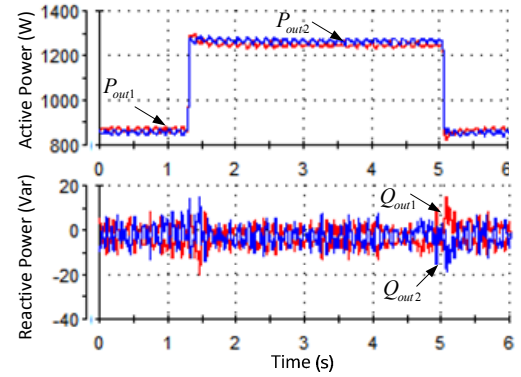
(a)



(b)



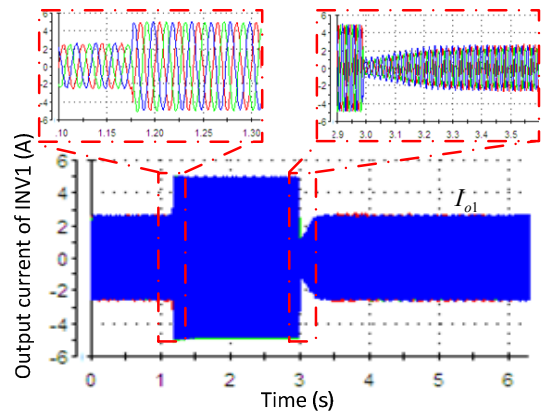
(c)



(d)

Fig. 11. Transient response of paralleled inverters sharing resistive load when load stepping up/down. (a) output currents of inverter#1, (b) output currents of inverter#1, (c) output direct and quadrature currents of inverter#1, #2, (d) active and reactive power of inverter#1, #2.

Fig. 12 shows the transient response of the paralleled inverter system employing the novel controller during suddenly connecting and disconnecting one of the VSI. It can be seen that the slowest transient time is around 0.6s.



(a)

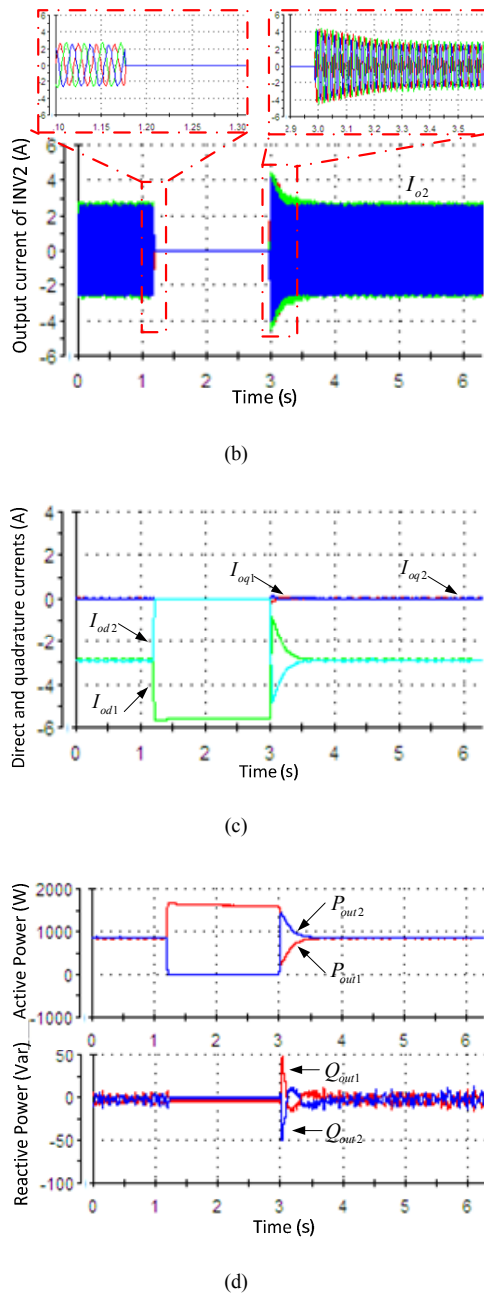


Fig. 12. Transient response of paralleled inverters sharing resistive load when inverter #2 connecting and disconnecting. (a) output currents of inverter#1, (b) output currents of inverter#1, (c) output direct and quadrature currents of inverter#1, #2, (d) active and reactive power of inverter#1, #2.

## VI. CONCLUSION

A simpler and faster controller which consists of a phase-locked loop and a virtual resistance loop for controlling output load current among parallel three-phase inverters is employed. The small signal model is developed based on the novel controller of inverter-based microgrids. The model was analyzed in terms of the system eigenvalues and their sensitivity in different scenarios. Experimental results verify the effectiveness of the proposed controller.

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