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A Novel Harmonic Elimination Approach in Three-Phase Multi-Motor Drives

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***Abstract*— Power electronics technology has been widely used for decades in the modern motor drive systems. Beyond the control flexibility, the power electronics devices (e.g., diode rectifiers) are also the main harmonic source to the grid due to their nonlinearity, which deteriorate the power grid quality and may cause unnecessary losses in power system transformers. Both degradations are apt to occur in motor drive applications. As a consequence, it calls for advanced and intelligent control strategies for the power electronics based drive systems like adjustable speed drives in industry. At present, many industrial drives are still equipped with three-phase diode rectifiers. Thus, it is difficult to implement the prior-art harmonic control strategies for active front-ends. Moreover, the total cost and complexity has become an obstacle for these harmonic elimination approaches in multiple drive systems. Therefore, in this paper, a new cost-effective harmonic mitigation approach has been proposed for multiple drives. The proposed approach can control the generated current harmonics by benefiting of the nonlinearity of the drive units and through a novel current modulation scheme. Simulation and experimental results have validated the effectiveness of the proposed approach in terms of harmonic elimination in three-phase multi-drive systems.**

Keywords—adjustable speed drives; harmonic elimination; multiple drives; three-phase rectifiers;

I. INTRODUCTION

Electrical motor drive systems consume a considerable amount of global electrical energy. As the electricity demand is growing faster worldwide, industry has been pushed towards an era of developing more energy-efficient drives. Employing intelligent control techniques for the power electronics based drive systems can improve the efficiency to some extent [1]. However, generated harmonics as a consequence of employing power electronics devices deteriorates the power grid quality [2]-[4]. The high level imposed harmonic input currents may cause unnecessary losses and heat in power system transformers and nuisance tripping of circuit breakers and over-stressing of power factor correction capacitors. This highlights the necessity for the drive systems to comply with international standards such as IEC61000 standard [5], and it calls for more smart harmonic elimination strategies for the drive systems.

Typically, a standard motor drive system comprises of three main sections: the front-end power converter that converts AC power from the mains to DC power, an energy storage unit called the DC-link, and finally an inverter as the rear-end power converter which converts the DC back to AC at the voltage and frequency demanded by the motor. A three-phase diode bridge rectifier is usually employed at the front-end stage, thus being the main harmonic source. A vast array of methods have been introduced to improve the input current quality by shaping it as close as possible to a sinusoidal waveform [3], [4], [6]-[8] as well as using active damping methods [9]-[14]. However, the complexity and cost are significantly increased. Therefore, diode rectifiers (uncontrolled) or thyristor-based rectifiers (phase-controlled) of less complexity and cost are still widely used in Adjustable Speed Drives (ASD).

In addition, the undesirable nonlinearity of the conventional AC-DC conversion stage may become significant, when a large number of industrial converters and ASDs are connected to the Point of Common Coupling (PCC). It has been found that a proper arrangement of these nonlinear loads can contribute to an effective harmonic mitigation, where some of the harmonics from one unit (e.g., diode rectifier) can be cancelled out by the other/s units [15]. The feasibility of this solution is attained only when suitable and accessible communication among the nonlinear units can be performed. For instance, it can be observed in some practical applications, where many ASD based industrial pumps, fans or compressors are operated all together. In fact, improving the input current quality by combining the nonlinear loads was first introduced in multi-pulse rectifiers [16]. In this method, by employing phase-shifting transformers, the harmonics of each unit can be phase-displaced with respect to each other, and thus they can cancel out each other. Depending on the number of connected units a range of harmonics can be eliminated. Taking a 24-pulse rectifier [16] as an example, the current Total Harmonic Distortion (THD_i) can significantly be improved (< 5 %) by using this method. Despite the effectiveness in harmonic mitigation, the volume, associated losses, and also the cost of the phase-shifted transformer are the main concerns.

In this paper, a novel harmonic elimination approach is proposed to tackle the aforementioned challenges. The proposed method does not require any phase-shifting transformers like what have been used in multi-pulse rectifiers. Instead, as depicted in Fig. 1, it combines a three-phase diode rectifier with a three-phase Silicon Controlled Rectifier (SCR) unit to cancel out the harmonics. Additionally, in order to improve the performance and flexibility of the system, each

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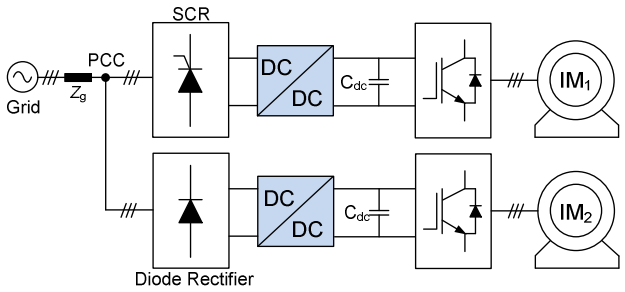


Fig. 1. Typical configuration for a multi-drive application with the proposed harmonic mitigation method.

unit is equipped with a novel current modulation technique, which can individually mitigate a certain number of current harmonics. Obtained simulation and experimental results have verified the effectiveness of the proposed method.

The rest of this paper is organized as follows. Section II presents the detailed analysis of the proposed harmonic elimination method along with the optimum harmonic solutions. In Section III, implementation details and hardware setup are pointed out. The performance of the proposed method is validated through simulation and experimentation in Section IV. Finally, concluding remarks are given in Section V.

II. Proposed Harmonic Elimination Method

A. Nonlinear Loads Comibinaton for Harmonic Cancellation

In order to demonstrate and evaluate the proposed method a multi-drive system of two three-phase rectifier units is built up as shown in Fig. 1. The details of system operation are illustrated in Fig. 2, where it is assumed that the current source at the DC-link side of the rectifier draws a constant current (i.e., I_{dc}). In practice, the current source can be implemented in a DC-DC converter (e.g., a boost converter), which can emulate an ideal inductor behavior [17]-[20]. Therefore, for both rectifiers as shown in Fig. 2, the input currents (i.e., i_s and i_d) will be a square-wave with the conduction angle of 120°, since at each instant of time interval only two phases conduct and circulate the DC-link current through the grid.

For the rectifier system shown in Fig. 2, Fourier series analysis has been adopted to identify the harmonic content of the input currents. According to Fig. 2(a), in a controlled rectifier (SCR), the harmonics (i.e., $i_s(n)$) of the square-wave input current with the 120° conduction angle and an adjustable phase angle of α_0 ($\alpha_0 = \alpha_f + 30^o$) can be identified as:

$$i_s(n) = \sqrt{(a_n)^2 + (b_n)^2}$$

with

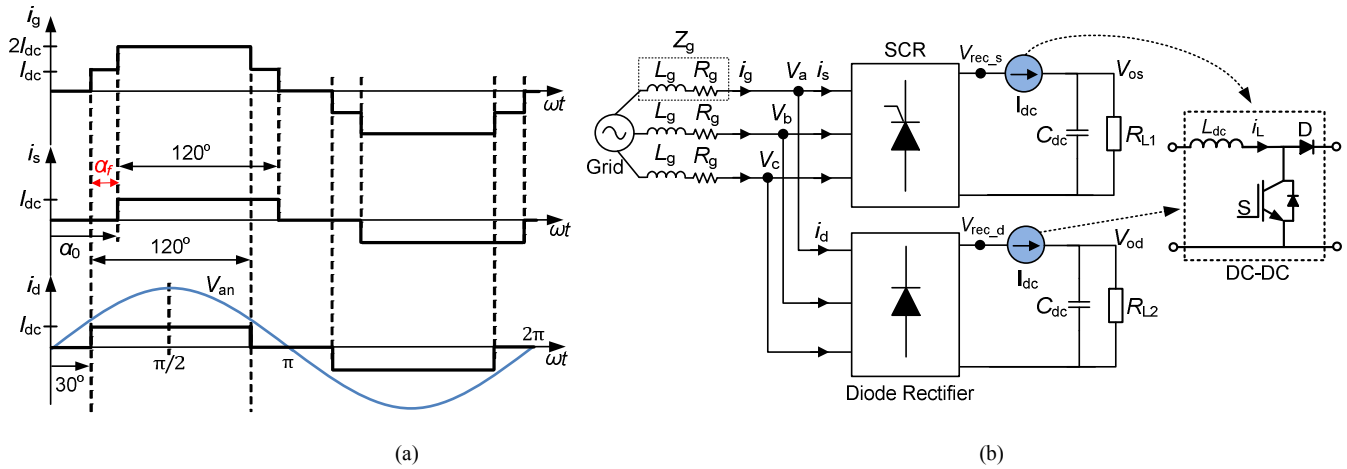
$$\begin{cases} a_n = \dfrac{2I_{dc}}{n\pi}\left[-\sin(n\alpha_0) + \sin\left(n\alpha_0 + \dfrac{2\pi n}{3}\right)\right] \\ b_n = \dfrac{2I_{dc}}{n\pi}\left[\cos(n\alpha_0) - \cos\left(n\alpha_0 + \dfrac{2\pi n}{3}\right)\right] \end{cases} \quad (1)$$

in which n is the harmonic order. As for the three-phase diode rectifier, it can be taken as a special case of the SCR with a fixed phase angle of $\alpha_0 = 30^o$ ($\alpha_f = 0^o$). In that case, $a_n = 0$ according to (1), and thus the harmonics of the input current induced by the diode rectifier can be calculated as:

$$i_d(n) = \frac{4I_{dc}}{n\pi}\cos\left(\frac{n\pi}{6}\right) \quad (2)$$

According to Fig. 2, the harmonics appearing in the line current ($i_g = i_s + i_d$) can be expressed as,

$$i_g(n) = \sqrt{(a_n)^2 + \left(i_d(n) + b_n\right)^2} \quad (3)$$



(a) (b)

Fig. 2. Current distribution at the PCC of a multi-drive system with one diode rectifier and one SCR unit: (a) ideal currents and (b) system schematic.

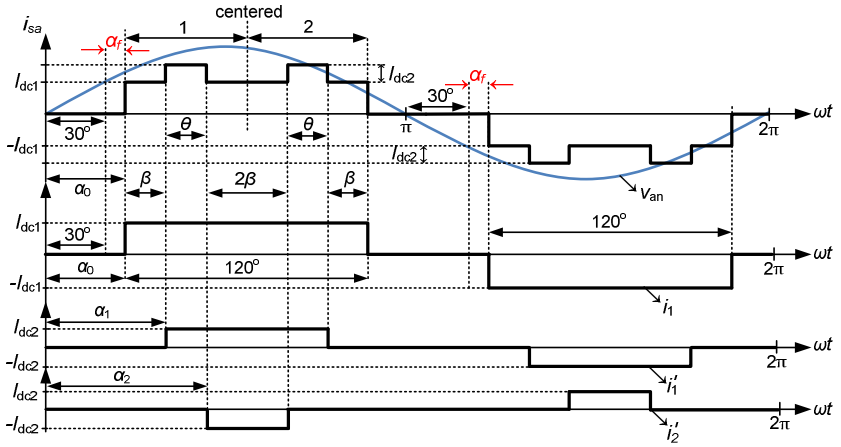


Fig. 3. Illustration of the proposed current modulation waveform with selected harmonic cancellation for a single rectifier unit (α_f = 0 in the case of a diode rectifier).

In order to cancel out any *n*-th harmonics and maintain the desired fundamental content of the grid current as the modulation index, the transcendental equations given in (4) should be solved.

$$\begin{cases} i_g(1) = M_a \\ a_n = 0 \\ b_n + i_d(n) = 0 \end{cases} \tag{4}$$

where M_a is the desired modulation index.

B. *Novel Current Modulation Technique*

Although an appropriate adjustment of the phase angle of the SCR unit can contribute to an improvement of the current quality, a new current modulation technique is further applied to each DC-DC converter in order to improve the current quality. In the new current modulation approach, certain low frequency harmonics in the three-phase input line currents can be eliminated by adding (or subtracting) phase-displaced current levels, thus leading to a better overall grid power quality. This technique is based on a pre-programmed switching pattern for the DC-link current to obtain input currents with zero content at those specific harmonics [7].

The basic idea of the proposed current modulation method for only one rectifier unit (SCR) is demonstrated in Fig. 3. For simplicity, the waveforms have been centralized in respect to the grid voltage to analyze the harmonic characteristics. In order to mitigate the triple harmonics, new added current levels should be repeated every 1/6 of the fundamental period. For instance, in the two sectors of 1 and 2 shown in Fig. 3, where in each sector i_{sa} is circulated through one of the other phase currents, if the new current level is added into sector 1, it should be exactly repeated in sector 2. This means that the frequency of the added pulses at the DC-link should be six times of the fundamental frequency. As it is shown in Fig. 3, the proposed current waveform consists of three square-wave signals with different magnitudes and angles. The first current waveform has the magnitude of I_{dc1} with the conduction phase angle of α_0 ($\alpha_0 = \alpha_f + 30^o$). Notably, for a three-phase diode rectifier this conduction phase angle is constant, α_0=30°. The second current waveform has the magnitude of I_{dc2} with the conduction phase angle of α_1. The third current waveform has the magnitude of I_{dc2} but with a conduction phase angle of α_2. According to (1) the input current harmonics can be calculated.

$$i_s(n) = \sqrt{(a_n + a_n')^2 + (b_n + b_n')^2}$$

with

$$\begin{cases} a_n' = \sum_{j=1}^{2} \dfrac{2I_{dc2}(-1)^{j+1}}{n\pi}\left[-\sin(n\alpha_j) + \sin\left(2n\alpha_0 - n\alpha_j + \dfrac{2\pi n}{3}\right)\right] \\ b_n' = \sum_{j=1}^{2} \dfrac{2I_{dc2}(-1)^{j+1}}{n\pi}\left[\cos(n\alpha_j) - \cos\left(2n\alpha_0 - n\alpha_j + \dfrac{2\pi n}{3}\right)\right] \end{cases} \tag{5}$$

where i_a is the phase A current of the grid, a'_n and b'_n are the Fourier coefficients of the new added current levels that conduct at α_1 and α_2, and $\alpha_0 < \alpha_1 < \alpha_2 < \alpha_0 + 60°$. Hence, in order to individually cancel out up to two low order harmonics, e.g., $i_a(m)$ and $i_a(k)$, the following condition holds,

$$2\beta + \theta = 60 \quad \text{or} \quad 2(\alpha_1 - \alpha_0) + (\alpha_2 - \alpha_1) = 60 \tag{6}$$

As for the three-phase diode rectifier α_0=30° (α_f = 0°) and in that case $a_n = a'_n = 0$. Therefore, the harmonics of the input current represented in (5) can be simplified as:

$$i_d(n) = \frac{4}{n\pi}\left[I_{dc1}\cos\left(\frac{n\pi}{6}\right) + I_{dc2}\cos(n\alpha_1) - I_{dc2}\cos\left(\frac{2\pi n}{3} - \alpha_1\right)\right] \tag{7}$$

Hence, applying the proposed current modulation technique to both of the rectifier units can significantly improve the input current quality. Notably, the harmonics appearing in the supply line (i.e., i_g) can be calculated as,

$$i_g(n) = \sqrt{(a_n + a_n')^2 + (i_d(n) + b_n + b_n')^2} \tag{8}$$

C. Optimum Harmonic Solution

The above illustrates the impact on the harmonics by selecting proper modulation parameters (amplitudes and switching angles) for the proposed current modulation scheme. However, an optimization for these parameters may result in a more suitable solution and also higher flexibility to eliminate the harmonics of interest. The following demonstrates the harmonic optimization solution considering the maximum allowable harmonic level defined by the application or the grid code. In other words, instead of fully nullifying the distortions, the harmonics could be reduced to acceptable levels by adding suitable constraints (L_n). Then, an optimization problem (Obj_n) that searches a set of α_n and I_{dc} values over the allowable intervals can be defined as,

$$\begin{cases} Obj_1 = M_a - \left|i_g(1)\right| \le L_1 \\ Obj_n = \dfrac{\left|i_g(n)\right|}{\left|i_g(1)\right|} \le L_n \end{cases} \tag{9}$$

Based on (9) an objective function F_{obj} has to be formed to minimize the error. The objective function plays an important role in leading the optimization algorithm to the suitable solution set. Here, F_{obj} is formed based on a squared error with more flexibility by adding constant weight values (w_n) to each squared error function [21]:

$$F_{obj} = \sum w_n \cdot \left(Obj_n - L_n\right)^2 \tag{10}$$

Moreover, the THD_i restriction could also be the objective function or included in (10) and prioritized with a suitable weight value. In addition to the optimization constraint L_n, the following condition needs to be included as well:

$$\alpha_0 < \alpha_1 < \alpha_2 < \cdots < \alpha_m < \alpha_0 + \frac{\pi}{3} \tag{11}$$

III. Single Switch Three-Phase Boost Rectifier System

In order to control the DC-link current shape and magnitude following the waveforms shown in Fig. 2, a boost converter topology based on the electronic inductor [17]-[20] concept is employed. Using the conventional boost topology has the advantage of boosting the output DC voltage to a suitable level when it is fed to an inverter. Moreover, as the DC-link current is controlled based on the load power, it has the advantage of keeping the THD_i independent of the load profile.

Fig. 4 depicts the block diagram of the overall control structure for the multi-rectifier units, where a hysteresis controller is adopted as the current controllers for the boost converters. The reference tracking performance of the current controller has an important role in the harmonic mitigation, thus fast current control methods such as hysteresis or dead-beat control should be employed. In order to synchronize the current controllers with the grid, for each rectifier unit a Second-Order Generalized Integrator (SOGI) based Phase

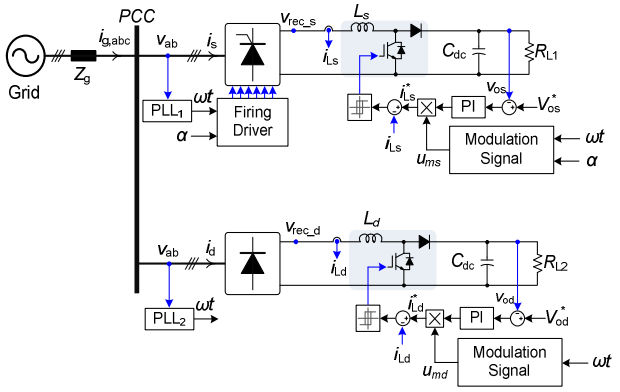


Fig. 4. Block diagram of the overall control structure implemented for the multi-rectifier system.

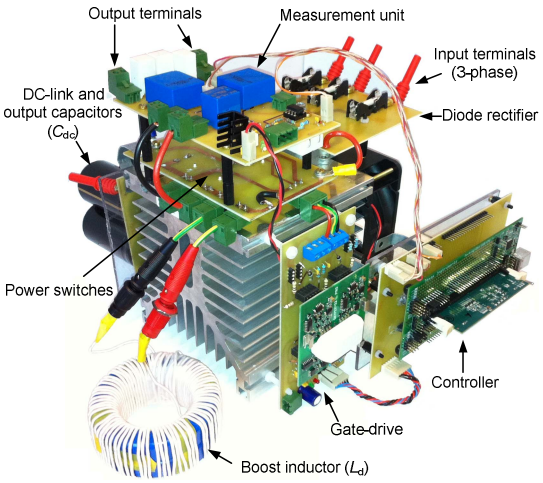
Locked Loop (PLL) system is adopted [22]. For simplicity, assuming a balanced system, only one line-to-line voltage is fed to the PLL. Therefore, the result will have a phase shift of 30^o in respect to the phase voltage, which should be corrected within the reference current generator algorithm. In order to obtain a discretization for the PLL and the Proportional Integrator (PI) controller, a trapezoidal method is used. Moreover, as it can be seen from the system schematics shown in Fig. 4, the firing angle of the thyristor based rectifier (SCR) should be applied according to the phase detected by the PLL.

Fig. 5 shows the developed prototypes for the three-phase rectifier systems, where Fig. 5(a) depicts a photograph of the three-phase diode rectifier unit and Fig. 5(b) shows the three-phase SCR unit including the boost converter for each unit. Table I summarizes the employed modules in the implemented prototypes.

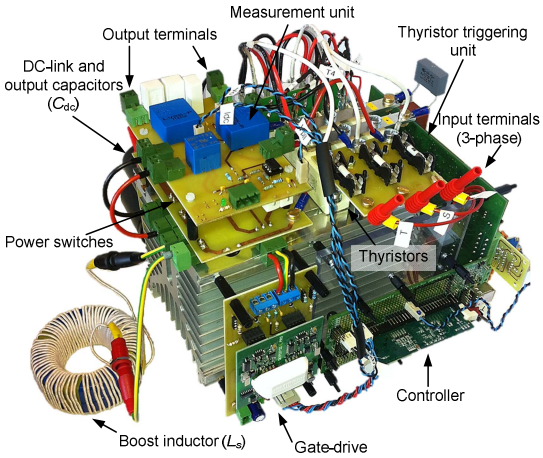
IV. Results

Simulations have firstly been done to verify the effectiveness of the proposed method. A comparison with other systems (see Fig. 6) in terms of harmonic mitigation has been carried out. For the first two systems shown in Fig. 6, a constant current source (implemented by a boost converter) at the DC-link side has been considered. Actually, the SCR without any current modulation in the second system has a fixed 30^o phase-shift in respect to the other unit. The grid impedance L_g and R_g (Z_g) as shown in Figs. 2 and 4 are set to 0.1 mH and 0.01 Ω, respectively. For the 12-pulse phase-shifting transformer impedance components are selected to be 160 µH and 5 mΩ. The grid phase voltage is 220 V_{RMS} and the grid frequency is 50 Hz. The output voltage of the boost converter is maintained at 700 V_{DC} by employing a proportional integrator controller and a hysteresis controller is adopted as the current controller. A MATLAB function – "fmincon" has been used for optimization. The results are shown in Figs. 7 and 8.

Since only the low-order harmonics are of much interest, the proposed method has been optimized according to (9)-(11) in order to attenuate the 5^{th}, 7^{th} and 11^{th} harmonics to be less than 1 % of the fundamental component (i.e., selected optimization constraints). In addition, THD_i is also included in the objective function (THD_i < 12.5 %). Fig. 7 (a) presents the



(a)



(b)

Fig. 5. Photograph of implemented single switch three-phase boost rectifier for (a) diode rectifier and (b) SCR system.

results of the multi-drive system shown in Fig. 2 (b) with the proposed modulation strategy, which confirms that a multi-level input current is achieved by the phase-shift based modulation scheme, contributing to a lower THD_i. This benefit is further verified by the comparison with other configurations

TABLE I
EMPLOYED MODULES IN THE IMPLEMENTED PROTOTYPE (FIG. 5)

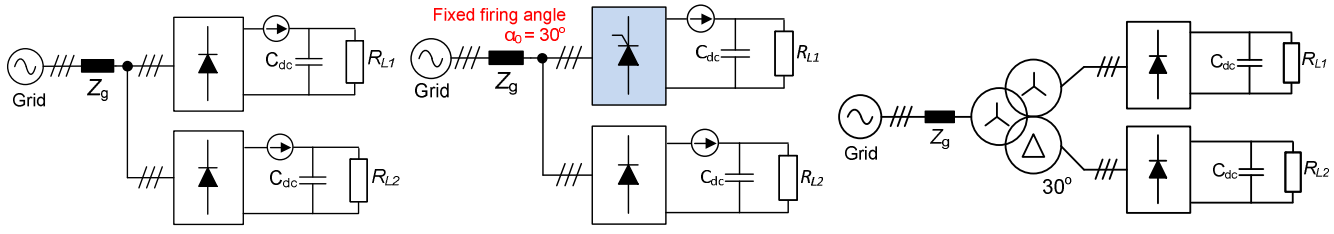
Module	Part-Number	Qty
Three-phase diode rectifier	SKD30	1
Three-phase SCR	SKKT 106/16	3
IGBT-diode	SK60GAL125	2
IGBT gate drive	Skyper 32-pro	2
SCR triggering circuit	RT380T	1
Current measurement	HX-15	2
Voltage measurement	LV25-P	2
SCR snubber branch	R_{snub} = 100 Ω, C_{snub} = 0.1 µF	6
Controller	TMS320F28335	2

(see Fig. 6), where the low-order harmonics (5th, 7th, and 11th) have been controlled (optimized) to a relatively low level by the proposed method, as it is shown in Fig. 7(b). However, the 7th and the 11th harmonics are slightly higher than the optimization target (less than 1 %) due to the effect of the grid impedance.

In addition, the flexibility of the proposed method is demonstrated in another case study, where the THD_i is selected as the optimization objective function. It can be observed in Fig. 8(a) that a THD_i of 10.5 % is attained in the multi-drive system with the proposed method regardless of output power levels (load profiles) in contrast to the 12-pulse based drive system. Although some individual harmonics are higher when compared to the 12-pulse rectifier as shown in Fig. 8(b), the THD_i is minimized in contrast to that in Fig. 6(b). Table II summarizes the detailed harmonic content of the rectifier systems at a constant output power level of 5.5 kW.

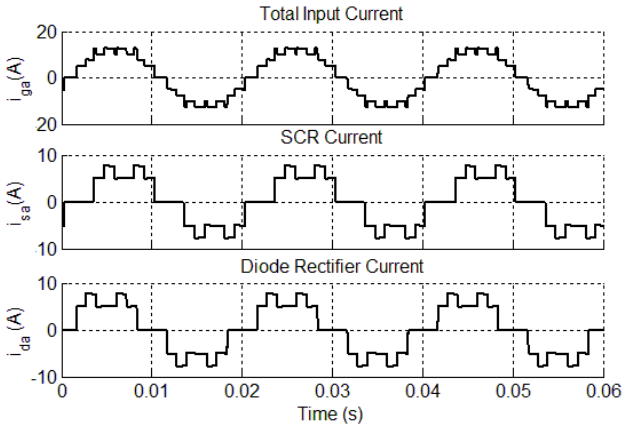
It should be noted that the optimization was performed based on an assumption that each rectifier unit draws equal amount of current from the grid; otherwise, the rectified voltages V_{rec_s} and V_{rec_d} (see Fig. 4) are different due to the phase-shift and thus leading to different boost conversion gain ratio and may complicate the harmonic distributions.

In addition to the effect of the phase-shift, in real-world applications the two rectifier units do not necessarily operate at the same power level. Since the system is not dependent on the load profile, the power level itself is not the concern, and the ratio between output-power levels of the rectifier units are of importance. Therefore, as long as the following equation holds true, the rectifiers draw equal amount of current from the grid; otherwise it should be reflected in the optimization process in one of the objective functions.

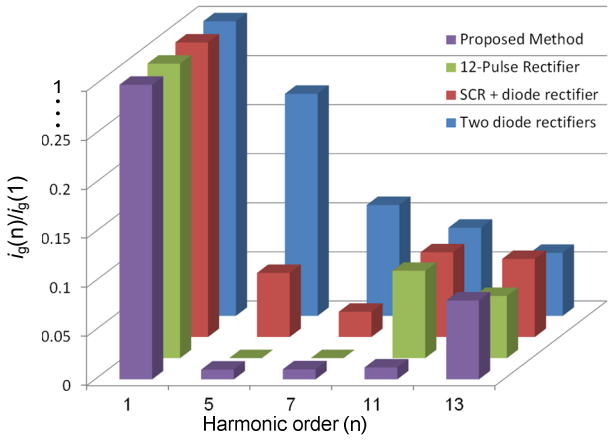


(a) (b) (c)

Fig. 6. Different rectifier units: (a) two diode rectifiers, (b) one diode rectifier and one SCR with a fixed phase shift of 30° and (c) 12-pulse rectifier.

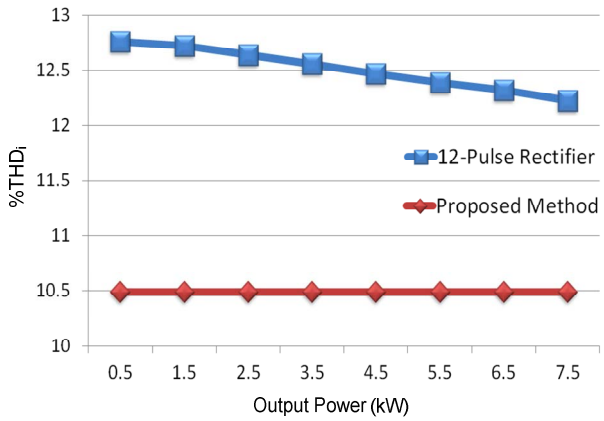


(a)

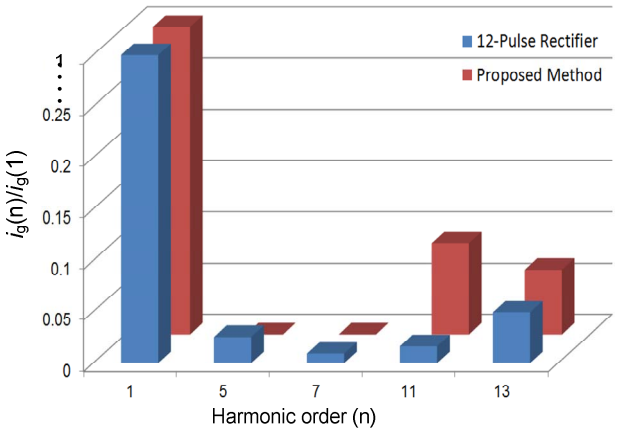


(b)

Fig. 7. Performance of a multi-drive system shown in Fig. 2(b) with the proposed method: (a) current waveforms and (b) comparison of the low-order harmonics with other configurations (see Fig. 4) at the total output power level of 5.5 kW.



(a)



(b)

Fig. 8. Performance of the multi-drive system with the proposed method and the 12-pulse rectifier based system: (a) total input current THDi at varied power levels and (b) input current spectrums of the two systems at the total output power level of 5.5 kW.

$$\frac{P_{o\_d}}{P_{o\_s}} \times \cos(\alpha_f) = 1 \tag{12}$$

where P_{o_d} and P_{o_s} are the output power of the diode rectifier and SCR unit, respectively. Notably, to save computation complexity different pre-calculated current modulation parameters with their corresponding power ratios should be included as a look-up table in the controller. Therefore, by including a communication between each rectifier units suitable combination of the input currents at the PCC can be made under varied situation.

In order to verify the effectiveness of the proposed method, experimental tests have been carried out on a 5.5-kW multi-rectifier system (Fig. 5). Firstly, the control objective is to lower the THD_i and also to reduce the 5^{th}, 7^{th}, and 11^{th} harmonics. It can be seen in Fig. 9 that the 5^{th}, 7^{th}, and 11^{th} – order harmonics are almost completely eliminated, since they are considered in the optimization function as shown in (10). In addition, a THD_i of 11.5 % of the grid current is also obtained,

TABLE II.
HARMONIC DISTRIBUTION OF DIFFERENT SIMULATED RECTIFIER SYSTEMS AT A TOTAL OUTPUT POWER LEVEL OF 5.5 KW.

System Configuration	Harmonic Distribution and THD_i (%)				
	$i_{g(5)}/i_{g(1)}$	$i_{g(7)}/i_{g(1)}$	$i_{g(11)}/i_{g(1)}$	$i_{g(13)}/i_{g(1)}$	THD_i
Two Diode Rectifiers (Fig. 6(a))	22.6	11.3	9	6.4	29.4
SCR + Diode Rectifier (Fig. 6(b))	6.5	2.6	8.6	8	15.6
12-Pulse Rectifier (Fig. 6(c))	0	0	8.9	6.3	12.4
[1]Proposed Method	1	1	1.2	8	12.3
[2]Proposed Method	2.6	0.95	1.7	4.9	10.5

1. Optimization objective is to minimize the low order harmonics including the THD_i (see Fig. 7)
2. Optimization objective is to achieve a lower THD_i (see Fig. 8(b))

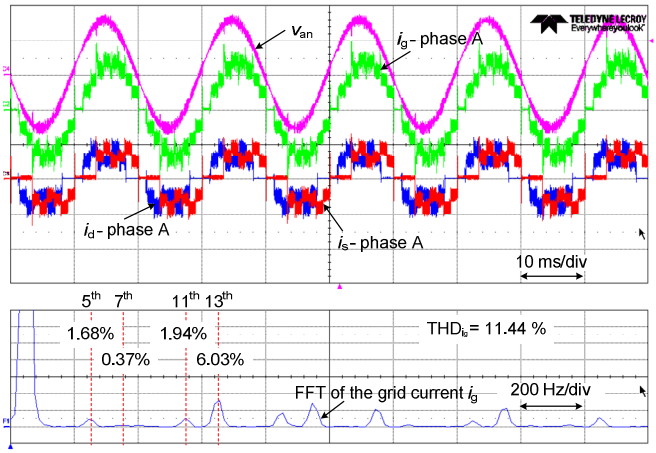


Fig. 9. Experimental results (phase A) of the multi-drive system with the novel current modulation scheme at $P_o \approx 5.5$ kW, $V_o = 700$ V_{DC}, targeting at reducing the low order harmonics and also a lower THD$_i$: grid current i_g [10 A/div], grid phase voltage v_{an} [200 V/div], diode rectifier input current i_d [10 A/div], SCR unit input current i_s [10 A/div], and Fast Fourier Transform (FFT) analysis of the grid current [500 mA/div].

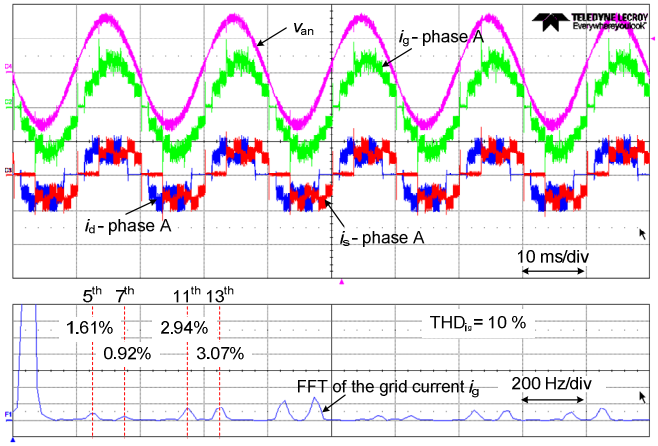


Fig. 10. Experimental results (phase A) of the multi-drive system with the novel current modulation scheme at $P_o \approx 5.5$ kW, $V_o = 700$ V_{DC}, targeting at a minimized THD$_i$: grid current i_g [10 A/div], grid phase voltage v_{an} [200 V/div], diode rectifier input current i_d [10 A/div], SCR unit input current i_s [10 A/div], and Fast Fourier Transform (FFT) analysis of the grid current [500 mA/div].

when applying the novel modulation scheme to both rectifier units. The occurrence of the current spikes in the SCR current (e.g. i_s) at the point of commutation is due to presence of the snubber branches in the SCR unit. In practice, to avoid SCR unit failures and to reduce the overvoltage to a reasonable limit an RC snubber branch is connected across each thyristor. In order to damp the current spikes, small AC-side inductors can be placed in series prior to the SCR unit.

To further validate the performance of the proposed method minimizing the THD$_i$ was only considered as the optimization target. Fig. 10 presents the performance of the multi-rectifier system where a THD$_i$ of around 10 % is achieved. At the same time, the low order harmonics are at relatively low levels. The results are quite in agreement with the simulations. Table III

TABLE III.
HARMONIC DISTRIBUTION OF DIFFERENT EXPERIMENTAL CASES FOR RECTIFIER SYSTEMS AT A TOTAL OUTPUT POWER LEVEL OF 5.5 KW.

Optimization Objective	Harmonic Distribution and THD$_i$ (%)				
	$i_{g(5)}/i_{g(1)}$	$i_{g(7)}/i_{g(1)}$	$i_{g(11)}/i_{g(1)}$	$i_{g(13)}/i_{g(1)}$	THD$_i$
[1]Proposed method	1.7	0.4	1.9	6	11.4
[2]Proposed method	1.6	0.9	2.9	3	10

1. Optimization objective is to minimize the low order harmonics including the THD$_i$ (see Fig. 9)
2. Optimization objective is to achieve a lower THD$_i$ (see Fig. 10)

TABLE IV.
OPTIMIZED CALCUALTED MODULATION PARAMETERS (WITH $M_a = 1$).

Optimization Objective	Normalized Parameters			
	I_{dc1}	I_{dc2}	α_1	α_f
[1]Proposed method	0.4	0.22	50°	36°
[2]Proposed method	0.4	0.2	50°	38.7°

1. Optimization objective is to minimize the low order harmonics including the THD$_i$ (see Fig. 9)
2. Optimization objective is to achieve a lower THD$_i$ (see Fig. 10)

summarizes the harmonic distribution of the conducted experimental cases.

As stated before, the pre-calculated switching parameters for the modulation strategy under different situations should be included as a look-up table in the controller. Table IV illustrates the estimated current modulation parameters for the two optimized cases with normalized amplitudes. Notably, the same parameters are applied to both rectifier units with a phase-shift of α_f.

To sum up, both the experimental tests and the simulations have demonstrated the effectiveness of current harmonic mitigations in multi-rectifier systems by means of: a) phase-shifting the currents drawn by SCR unit and b) a novel current modulation scheme at the boost inductor. Those can significantly contribute to a good power quality in both the single-drive and the multi-drive systems.

V. CONCLUSIONS

In this paper, a new harmonic elimination approach by combining different non-linear loads has been proposed for three-phase multi-drive systems, where also a Silicon Controlled Rectifier (SCR) is adopted. The proposed method can enable the selected harmonic cancellation by adjusting the phase angle of the SCR, and thus it can contribute to an improved power quality of the main grid. Moreover, in order to further reduce the harmonics, a novel modulation scheme has been applied to the DC-DC converter in the drive systems. The modulation scheme is able to eliminate the harmonics of interest by adding or subtracting specific current levels with respect to the conventional modulation approach. As a consequence, the combination of multiple non-linear loads with the new modulation scheme offers much flexibility as well as

cost-effectiveness for the multi-drive systems in terms of harmonic elimination. A main advantage of the proposed method is that the harmonic distribution remains the same regardless of load profile variations. Simulation and experimental results have verified the effectiveness of the proposed harmonic elimination approach.

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