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# Leakage Current Elimination of Four-Leg Inverter for Transformerless Three-Phase PV Systems

Xiaoqiang Guo, Ran He, Jiamin Jian, Zhigang Lu, Xiaofeng Sun, and Josep M. Guerrero

***Abstract*—Eliminating the leakage current is one of the most important issues for transformerless three phase photovoltaic (PV) systems. In this paper, the leakage current elimination of a three-phase four-leg PV inverter is investigated. With the common mode loop model established, the generation mechanism of the leakage current is clearly identified. Different typical carrier-based modulation methods and their corresponding common mode voltages are discussed. A new modulation strategy with Boolean logic function is proposed to achieve the constant common mode voltage for the leakage current reduction. Finally the different modulation methods are implemented and tested on the TMS320F28335 DSP +XC3S400 FPGA digital control platform. The experimental results verify the effectiveness of the proposed solution.**

***Index Terms*—Transformerless photovoltaic system, three-phase four-leg inverter, pulse width modulation, leakage current**

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## I. INTRODUCTION

Transformerless photovoltaic (PV) inverters have been receiving more and more attention due to small size, low cost and high efficiency. But the leakage current arises due to lack of galvanic isolation. The leakage current is prone to result in the electromagnetic interferences and potential safety problems. Therefore, the leakage current should be limited below the VDE 0126-01-01 standard of 30 mA [1].

Many interesting methods have been reported to deal with the leakage current for transformerless PV inverters. They can be classified into two groups: single-phase and three-phase solutions. For single-phase applications, the basic idea is to achieve both the unipolar three-level PWM and constant common mode voltage by integrating the auxiliary switches into H-bridge inverter [2]–[10]. It has the advantages such as the small filter inductor due to the low current ripple and negligible leakage current. Another insightful contribution by Zhou and Li is the leakage current suppression solution for the cascaded multilevel PV inverter [11]. Note that all the abovementioned single-phase topologies operate in the hard-switching mode. In order to further increase the efficiency, Xiao, et al proposed the soft-switching transformerless PV inverter [12], [13]. It can achieve the higher efficiency with the leakage current suppression capability. On the other hand, for three-phase applications, a solution proposed by Cavalcanti, et al, utilizes the improved modulation techniques for the constant common mode voltage to reduce the leakage current [14]. In [15], a space vector modulation is presented to keep the common mode voltage constant for eliminating the leakage current in three-level neutral point clamped inverters. Another interesting space vector modulation was proposed by Lee, et al to reduce the leakage current for three-phase 3-level T type inverters [16]. Both solutions are based on the space vector modulation, which is interesting and insightful, but needs the high computational burden due to the space vector sector selection, dwell time calculation and pulse sequence arrangement [17]. It should be noted that most of abovementioned three-phase solutions are limited to three-leg PV inverters, while the solutions for three-phase four-leg PV inverters are not received much attention. In [18], a four-leg inverter with a phase-shifting modulation has been presented to eliminate the common mode voltage. However, its operation is limited with a modulation index less than 0.666 or more than 1.108. In typical PV system applications, the modulation index is generally higher than 0.666 and lower than 1.0 for an effective dc-link voltage utilization and linear modulation operation range. Therefore, the new modulation strategy with leakage current elimination for three-phase four-leg PV inverter needs further investigation.

The objective of this paper is to develop a new modulation strategy for the leakage current elimination in three-phase four-leg PV inverter. The rest of the paper is organized as follows. Section II presents the theoretical analysis of the common-mode loop model for the three-phase four-leg PV inverter, and then the factors which affect the leakage current are clearly clarified. In Section III, the conventional modulation strategies are discussed, and then a new modulation strategy with Boolean logic function is proposed. Section IV evaluates the performance of the different modulation strategies of the four-leg PV inverter in term of the leakage current. Finally, the conclusion is provided in Section V.

## II. COMMON-MODE MODEL OF FOUR-LEG PV INVERTER

Fig. 1 shows the schematic of three-phase four-leg PV inverter, where $C_{pv}$ is the parasitic capacitor between the PV panel and ground. The common-mode loop model is shown in Fig. 2, where $U_{PV}$ is parasitic capacitor voltage, $I_{CM}$ is leakage current, $U_{AN}$, $U_{BN}$, $U_{CN}$, $U_{DN}$ are the voltages between the inverter outputs and the negative terminal of the PV array, $V_{Ci(i=1,2,3,4)}$ is filter capacitor $C_i$ voltage.

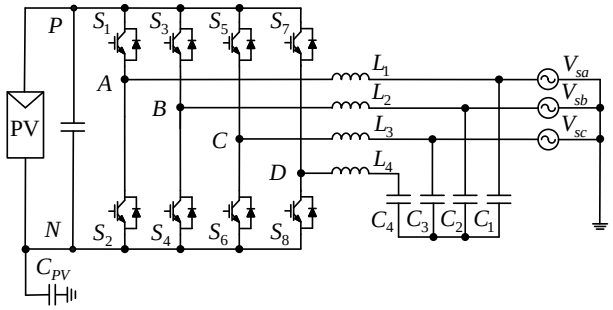



Fig. 1 Schematic of three-phase four-leg PV inverter.

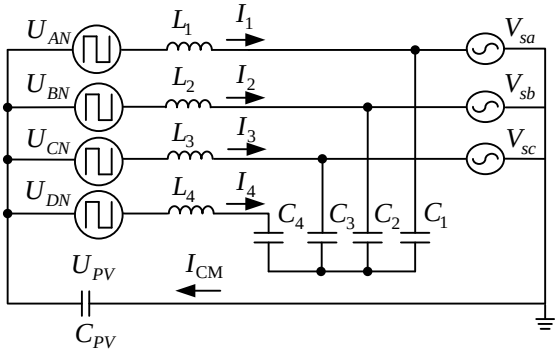



Fig. 2 Common-mode loop model.

To better understand the common-mode loop model, the following mathematical equations are derived from Fig. 2 with the Kirchhoff laws.

$$U_{PV} = U_{AN} + sL_1 I_1 + V_{sa} \quad (1)$$

$$U_{PV} = U_{BN} + sL_2 I_2 + V_{sb} \quad (2)$$

$$U_{PV} = U_{CN} + sL_3 I_3 + V_{sc} \quad (3)$$

$$U_{PV} = U_{DN} + sL_4 I_4 + V_{c4} - V_{c1} + V_{sa} \quad (4)$$

$$U_{PV} = U_{DN} + sL_4 I_4 + V_{c4} - V_{c2} + V_{sb} \quad (5)$$

$$U_{PV} = U_{DN} + sL_4 I_4 + V_{c4} - V_{c3} + V_{sc} \quad (6)$$

$$I_1 + I_2 + I_3 + I_4 = I_{CM} \quad (7)$$

The common mode voltage is defined as:

$$U_{CM} = (U_{AN} + U_{BN} + U_{CN} + U_{DN})/4 \quad (8)$$

The parasitic capacitor voltage of $U_{PV}$ can be derived from (1) ~ (8) as follows.

$$U_{PV}(s) = \frac{4}{4 + s^2 LC_{PV}} U_{CM}(s) + \frac{1}{4 + s^2 LC_{PV}} \frac{3C + C_4}{3C} V_{c4}(s) \quad (9)$$

where $C_1$=$C_2$=$C_3$=C, $L_1$=$L_2$=$L_3$=$L_4$=L.

The capacitor voltage of $V_{C4}$ can be also be derived as follows.

$$V_{c4}(s) = \frac{b_0 s^2 + b_2}{a_0 s^4 + a_2 s^2 + a_4} [4U_{CM}(s) - V_{od}(s)] \quad (10)$$

where $b_0$=3LC$C_{PV}$, $b_2$=12C, $a_0$=-3$L^2$C$C_4C_{PV}$, $a_2$=-(12LC$C_4$+3LC$C_{PV}$+L$C_4C_{PV}$), $a_4$=-(9C+3$C_4$) and $V_{od}$=($V_{AN}$+$V_{BN}$+$V_{CN}$).

The leakage current can be calculated:

$$i_{CM}(t) = -C_{PV} \frac{du_{PV}(t)}{dt} \quad (11)$$

From (11), it can be observed that the leakage current depends on both the parasitic capacitance of $C_{pv}$ and $du_{PV}(t)/dt$. In practice, the parasitic capacitance is unknown and dependent on many factors such as the humidity, weather conditions, dust covering the PV panel, and so on. However, the value of the parasitic capacitance is generally small, e.g. 220nF in [14]. On the other hand, the leakage current can be effectively suppressed if the voltage of $u_{PV}(t)$ is constant. From (9) and (10), it can be observed that $u_{PV}(t)$ is dependent on the common mode voltage of $U_{CM}$ and the fourth-leg capacitor voltage $V_{C4}$. Whereas $V_{C4}$ is relevant to $U_{CM}$. Therefore, the common mode voltage of $U_{CM}$ is the main concern.

For a three-phase four-leg inverter, there are $2^4$=16 switching states as shown in Tab. I, where $V_{dc}$ is the dc-link voltage.

Tab. I COMMON MODE VOLTAGE (CMV) AND SWITCHING STATES

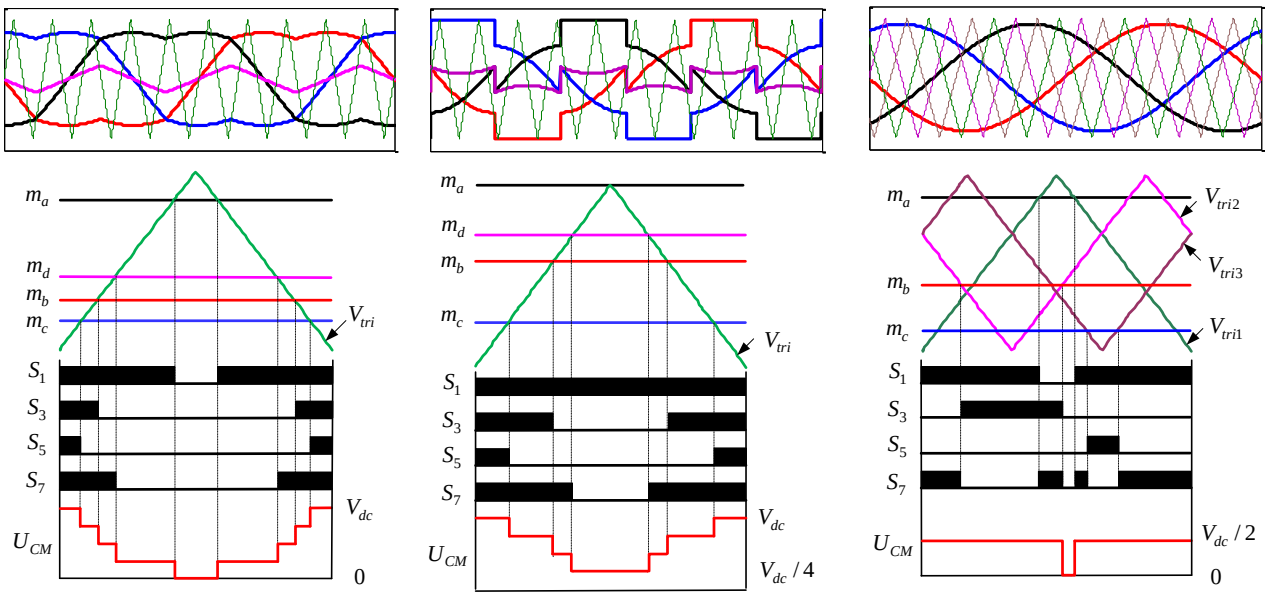
| CMV | Switching states |
|---|---|
| $V_{dc}$ | 1111 |
| $3V_{dc}/4$ | 1110, 1101, 1011, 0111 |
| $V_{dc}/2$ | 1100, 1001, 0011, 0101, 1010, 0110 |
| $V_{dc}/4$ | 0001, 0010, 0100, 1000 |
| 0 | 0000 |

As shown in Tab. I, the CMV varies in case of different switching states. The following section will discuss the effect of the different modulation methods on the switching states and common mode voltages.

## III. ANALYSIS OF DIFFERENT MODULATION STRATEGIES

### *A. Conventional modulation strategies*

The carrier-based PWM method is widely used for three-phase four-leg inverters, e.g. SVPWM and discontinuous PWM (DPWM). The switching pulse patterns are shown in Fig. 3 (a) and (b). In the case of Fig. 3 (a) and (b), $m_a$, $m_b$, $m_c$ and $m_d$ are modulation signals and zero-sequence component respectively. The switching signal of the fourth leg is generated by comparing $m_d$ with the triangle wave $V_{tri}$. In this way, the major difference between SVPWM and DPWM is $m_d$.



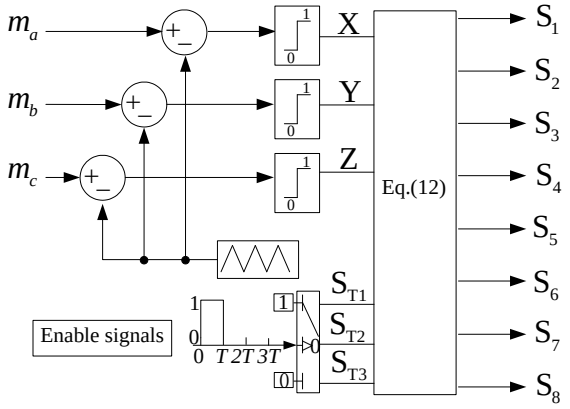

(a) (b) (c)

Fig. 3 Switching states and CMV in case of different modulation strategies (m=0.9). (a) SVPWM. (b) DPWM. (c) Phase-shifting modulation.

As shown in Fig.3, the peak-peak value of CMV is $V_{dc}$ in SVPWM. Although the peak-peak value of CMV is reduced in DPWM, but the CMV is still time-varing. In phase-shifting modulation, the peak-peak value of CMV is reduced, but the CMV is not constant. Therefore, the above three modulation methods are not able to eliminate the leakage current due to the high frequency CMV.

*B. Proposed modulation strategy*

In order to achieve the constant common mode voltage to eliminate the leakage current, a new modulation strategy is proposed, as shown in Fig. 4. The relationship between switching states and logic signals is listed in Table II.




$$
\begin{aligned}
&S_1=(X\bar{Y}+X\bar{Z}+\bar{Y}\bar{Z})S_{T1}+X\bar{S}_{T1} \quad && S_2=\bar{S}_1\\
&S_3=(\bar{X}Y+Y\bar{Z}+\bar{X}\bar{Z})S_{T2}+Y\bar{S}_{T2} && S_4=\bar{S}_3\\
&S_5=(\bar{X}Z+\bar{Y}Z+\bar{X}\bar{Y})S_{T3}+Z\bar{S}_{T3} && S_6=\bar{S}_5\\
&S_7=S_1\oplus S_3\oplus S_5 && S_8=\bar{S}_7
\end{aligned}
\tag{12}
$$

Fig. 4 Proposed modulation strategy

Tab. II Relationship between switching states and logic signals

| $S_{T1}$ ~$S_{T3}$ | XYZ | $S_1$ | $S_3$ | $S_5$ | $S_7$ | $U_{CM}$ |
|---|---|---|---|---|---|---|
| 100 | 000 | 1 | 0 | 0 | 1 | $V_{dc}/2$ |
| 010 | 000 | 0 | 1 | 0 | 1 | $V_{dc}/2$ |
| 001 | 000 | 0 | 0 | 1 | 1 | $V_{dc}/2$ |
| | 001 | 0 | 0 | 1 | 1 | $V_{dc}/2$ |
| | 010 | 0 | 1 | 0 | 1 | $V_{dc}/2$ |
| | 011 | 0 | 1 | 1 | 0 | $V_{dc}/2$ |
| | 100 | 1 | 0 | 0 | 1 | $V_{dc}/2$ |
| | 101 | 1 | 0 | 1 | 0 | $V_{dc}/2$ |
| | 110 | 1 | 1 | 0 | 0 | $V_{dc}/2$ |
| 100 | 111 | 0 | 1 | 1 | 0 | $V_{dc}/2$ |
| 010 | 111 | 1 | 0 | 1 | 0 | $V_{dc}/2$ |
| 001 | 111 | 1 | 1 | 0 | 0 | $V_{dc}/2$ |

In Fig. 4, the input signals XYZ are obtained by comparing the modulation signals $m_a$, $m_b$, $m_c$ and triangle carrier. When the modulation signal is larger than triangle wave, the output is 1, otherwise is 0. The rotation operation of $S_{T1}$, $S_{T2}$ or $S_{T3}$ works for each switching cycle of T. Thus it can be divided into three cases:

*Case I*: During the period [0~T], $S_{T1}$ is 1, while $S_{T2}$ and $S_{T3}$ are 0. Take Line 2 for example, when $S_{T1}$~$S_{T3}$ is 100 and XYZ is 000, the output signals $S_1$~$S_8$ can be obtained from (12) as follows.

$$\begin{aligned} &S_1=(X\overline{Y}+X\overline{Z}+\overline{Y}\overline{Z})S_{T1}+X\overline{S}_{T1}=1 \quad S_2=\overline{S}_1=0 \\ &S_3=(\overline{X}Y+Y\overline{Z}+\overline{X}\overline{Z})S_{T2}+Y\overline{S}_{T2}=0 \quad S_4=\overline{S}_3=1 \\ &S_5=(\overline{X}Z+\overline{Y}Z+\overline{X}\overline{Y})S_{T3}+Z\overline{S}_{T3}=0 \quad S_6=\overline{S}_5=1 \\ &S_7=S_1\oplus S_3\oplus S_5=1 \qquad\qquad S_8=\overline{S}_7=0 \end{aligned} \tag{13}$$

In this case, the output voltages are $U_{AN}=U_{DN}=V_{dc}$, $U_{BN}=U_{CN}=0$, thus the CMV is $U_{CM}=(U_{AN}+U_{BN}+U_{CN}+U_{DN})/4= V_{dc}/2$. Similarly, the CMV can be kept constant as $V_{dc}/2$ with other states in Case I.

*Case II*: During the period [T~2T], $S_{T2}$ is 1 and $S_{T1}$ and $S_{T3}$ are 0. Take Line 3 for example, when $S_{T1}$~$S_{T3}$ is 010 and XYZ is 000, the output signals $S_1$~$S_8$ can be obtained from (12) as follows.

$$\begin{aligned} &S_1=(X\overline{Y}+X\overline{Z}+\overline{Y}\overline{Z})S_{T1}+X\overline{S}_{T1}=0 \quad S_2=\overline{S}_1=1 \\ &S_3=(\overline{X}Y+Y\overline{Z}+\overline{X}\overline{Z})S_{T2}+Y\overline{S}_{T2}=1 \quad S_4=\overline{S}_3=0 \\ &S_5=(\overline{X}Z+\overline{Y}Z+\overline{X}\overline{Y})S_{T3}+Z\overline{S}_{T3}=0 \quad S_6=\overline{S}_5=1 \\ &S_7=S_1\oplus S_3\oplus S_5=1 \qquad\qquad S_8=\overline{S}_7=0 \end{aligned} \tag{14}$$

In this case, the output voltages are $U_{AN}=U_{CN}=0$, $U_{BN}=U_{DN}=V_{dc}$, thus the CMV is $U_{CM}=(U_{AN}+U_{BN}+U_{CN}+U_{DN})/4= V_{dc}/2$. Similarly, the CMV can be kept constant as $V_{dc}/2$ with other states in Case II.

*Case III*: During the period [2T~3T], $S_{T3}$ is 1 and $S_{T1}$ and $S_{T2}$ are 0. Take Line 4 for example, when $S_{T1}$~$S_{T3}$ is 001 and XYZ is 000, the output signals $S_1$~$S_8$ can be obtained from (12) as follows.

$$\begin{aligned} &S_1=(X\overline{Y}+X\overline{Z}+\overline{Y}\overline{Z})S_{T1}+X\overline{S}_{T1}=0 \quad S_2=\overline{S}_1=1 \\ &S_3=(\overline{X}Y+Y\overline{Z}+\overline{X}\overline{Z})S_{T2}+Y\overline{S}_{T2}=0 \quad S_4=\overline{S}_3=1 \\ &S_5=(\overline{X}Z+\overline{Y}Z+\overline{X}\overline{Y})S_{T3}+Z\overline{S}_{T3}=1 \quad S_6=\overline{S}_5=0 \\ &S_7=S_1\oplus S_3\oplus S_5=1 \qquad\qquad S_8=\overline{S}_7=0 \end{aligned} \tag{15}$$

In this case, the output voltages are $U_{AN}=U_{BN}=0$, $U_{CN}=U_{DN}=V_{dc}$, thus the CMV is $U_{CM}=(U_{AN}+U_{BN}+U_{CN}+U_{DN})/4= V_{dc}/2$. Similarly, the CMV can be kept constant as $V_{dc}/2$ with other states in Case III.

In summary, the CMV can be kept constant as $V_{dc}/2$ with the proposed modulation strategy.

## IV. EXPERIMENTAL RESULTS

In order to verify the effectiveness of the proposed modulation strategy, the experimental tests are carried

out. The system parameters are listed as follows. The DC bus voltage is 120V, the switching frequency is 10 kHz, filter inductor is 5 mH, filter capacitors are 9.9 uF, the modulation index is 0.9, and parasitic capacitor is 300 nF. The modulation algorithms are implemented in TMS320F28335 DSP, and the logic operations are programmed with XC3S400 FPGA. A performance comparison between conventional and proposed modulation strategies is presented as follows.

Fig. 5 shows the experimental results of the line-line voltage and output current. It can be observed that the line-line voltage is unipolar with SVPWM and DPWM, while bipolar in phase-shifting and proposed modulations. The THDs of four modulation methods are 78.82%, 78.94%, 106.65% and 110.11% respectively. However, after the output filter, the voltage and current will be sinusoidal, as shown in Fig. 5.

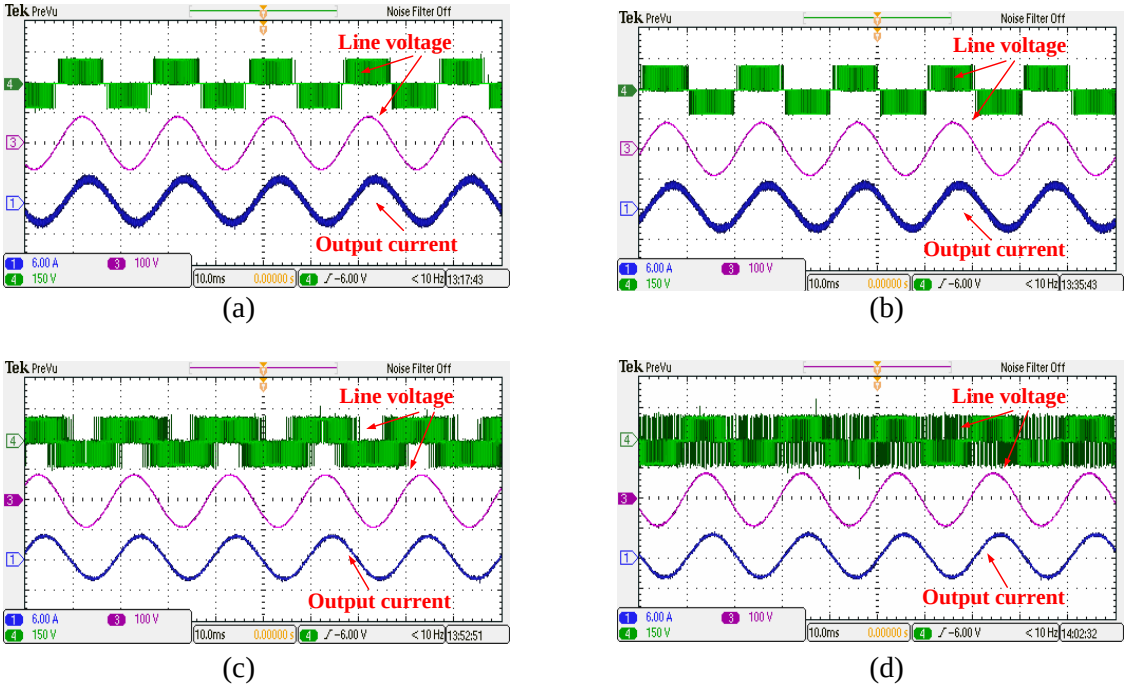



Fig. 5 Experimental results: Line-line voltage and output current. (a) SVPWM. (b) DPWM. (c) Phase-shifting modulation. (d) Proposed modulation.

Fig. 6 shows the experiment results of the parasitic capacitor voltage and leakage current. In agreement with the theoretical analysis, the parasitic capacitor voltage is time-varying with higher amplitude with SVPWM and DPWM. Therefore, the leakage currents are much higher than 1A in both cases.

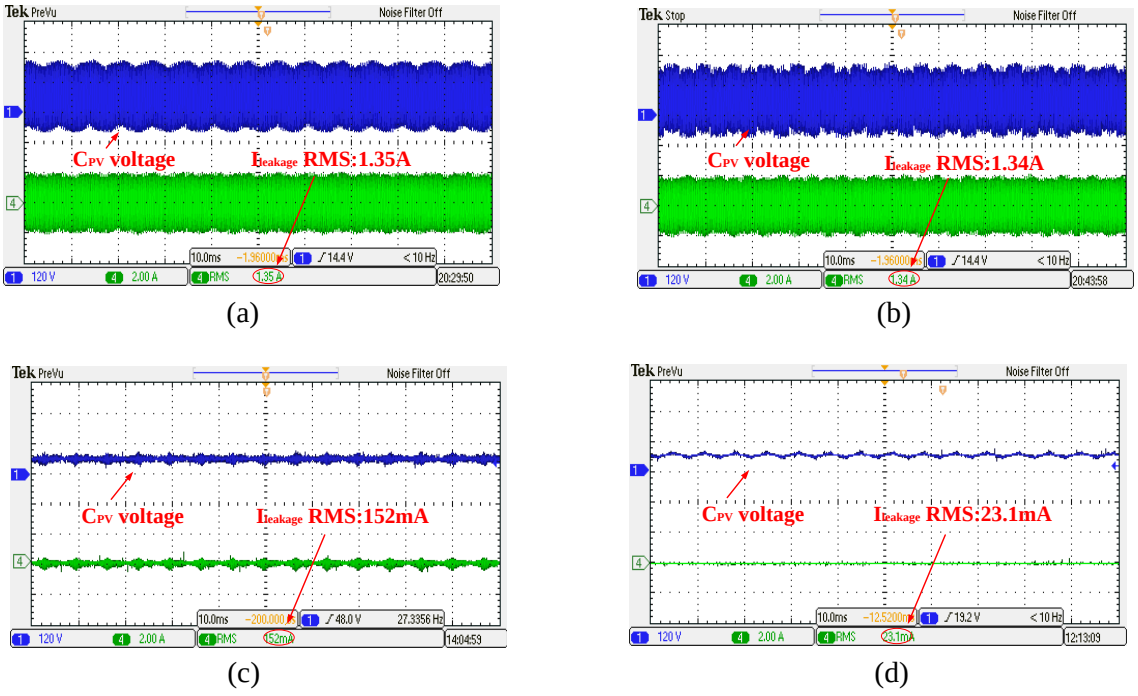



Fig. 6 Experiment results: the parasitic capacitor voltage and leakage current. (a) SVPWM. (b) DPWM. (c) Phase-shifting modulation. (d) Proposed modulation.

With the phase-shifting modulation, the peak-peak value of the parasitic capacitor voltage is still time-varying with small amplitude. So the leakage current can be reduced, but still as high as 152 mA. By using the proposed modulation method, the parasitic capacitor voltage remains almost constant without any high-frequency components. Therefore, the leakage current can be significantly reduced well below 30mA, which complies with the VDE 0126-1-1 standard.

In summary, only the proposed method can meet the leakage current requirements, and the proposed solution successfully solves the modulation index limitation in [18], and paves a way of applications of four-leg topology to three-phase transformerless PV systems.

A brief comparison with three-level converters such as NPC and T-type inverters is carried out. The four-leg topology requires less switches than NPC and T-type topologies, which reduces the system costs with high reliability due to less switches used [19]. On the other hand, the switch voltage stress of NPC topology is much lower than that of T-type and four-leg topologies. Therefore, the switching loss and system efficiency of NPC are better than that of T-type and four-leg topologies. In terms of harmonics, the line-line voltages of NPC and T-type topologies are five-level with lower harmonics, and the line-line voltage of four-leg topology are three-level with low harmonics. For the common mode leakage current, all three topologies can achieve the constant CMV and low leakage current. In practical applications, the system cost

is one of the most important factors. As for three topologies, the four-leg topology is the best choice, especially for the low voltage applications, due to less switches used. For high voltage applications, NPC and T-type topologies are better choices. Therefore, the selection of topologies is dependent on the specific applications. It should be noted that the brief comparison is done in this paper. A comprehensive comparison with the existing solutions needs a systematic investigation, and will be reported in the future paper.

## V. CONCLUSION

This paper has presented the analysis and experimental verification of a new modulation strategy to eliminate the leakage current of four-leg inverter for three-phase transformerless PV systems. The findings reveal that the conventional carried-based modulations are not able to keep the common mode voltage constant, and thus fail to reduce the leakage current in an effective way. On the other hand, the proposed modulation solution can achieve the constant common mode voltage. Therefore, the leakage current can be significantly suppressed well below 30 mA, as specified in the standard VDE-0126-1-1. In addition, the proposed modulation is simple to implement with no need of any space vector modulation. Therefore, it is attractive for three-phase transformerless PV systems.

## REFERENCES


[1] W. Li, Y. Gu, H. Luo, W. Cui, X. He, and C. Xia, "Topology review and derivation methodology of single-phase transformerless photovoltaic inverters for leakage current suppression," *IEEE Trans. Ind. Electron*., vol. 62, no. 7, pp. 4537–4551, Jul. 2015.

[2] L. Zhang, K. Sun, L. L. Feng, H. F. Wu, and Y. Xing, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters," *IEEE Trans. Power Electron*., vol. 28, no. 2, pp. 730–739, Feb. 2013.

[3] L. Zhang, K. Sun, Y. Xing, and M. Xing, "H6 transformerless full-bridge PV grid-tied inverters," *IEEE Trans. Power Electron*., vol. 29, no. 3, pp. 1229–1238, Mar. 2014.

[4] O. Lopez, F. D. Freijedo, A. G. Yepes, P. Fernandez-Comesaa, J. Malvar, R. Teodorescu, and J. Doval-Gandoy, "Eliminating ground current in a transformerless photovoltaic application," *IEEE Trans. Energy Convers*., vol. 25, no. 1, pp. 140–147, Mar. 2010.

[5] S. V. Araujo, P. Zacharias, and R. Mallwitz, "Highly efficient single phase transformerless inverters for

grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3118–3128, Sep. 2010.

[6] H. F. Xiao and S. J. Xie, "Transformerless split-inductor neutral point clamped three-level PV grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1799–1808, Apr. 2012.

[7] B. Yang, W. H. Li, Y. J. Gu, and W. F. Cui, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 752–762, Feb. 2012.

[8] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 184–191, Jan. 2011.

[9] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li and X. He, "Transformerless inverter with virtual dc bus concept for cost-effective grid-connected PV power systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 793-805, Feb. 2013.

[10] T. K. S. Freddy, N. A. Rahim,W. P. Hew, and H. S. Che, "Comparison and analysis of single-phase transformerless grid-connected PV inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5358–5369, Oct. 2014

[11] Y. Zhou and H. Li, "Analysis and suppression of leakage current in cascaded-multilevel-inverter-based PV systems," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5265–5277, Oct. 2014.

[12] H. F. Xiao, X. P. Liu, and K. Lan, "Zero-voltage-transition full bridge topologies for transformerless photovoltaic grid-connected inverter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5393-5401, Oct. 2014.

[13] H. Xiao, K. Lan, B. Zhou, L. Zhang, and Z. Wu, "A family of zero-current-transition transformerless photovoltaic grid-connected inverter," *IEEE Trans. Power Electron.*, *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3156–3165, Jun. 2015.

[14] M. C. Cavalcanti, K. C. de Oliveira, A. M. de Farias, F. A. S. Neves, G. M. S. Azevedo, and F. Camboim, "Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1360-1368, Apr. 2010.

[15] M. C. Cavalcanti, A. M. Farias, K. C. Oliveira, F. A. S. Neves, and J. L. Afonso, "Eliminating leakage currents in neutral point clamped inverters for photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 435–443, Jan. 2012.

[16] J. S. Lee, and K. B. Lee, “New modulation techniques for a leakage current reduction and a neutral-point voltage balance in transformerless photovoltaic systems using a three-level inverter,” *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1720–1732, Apr. 2014.

[17] K. Zhou and D. Wang, “Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis,” *IEEE Trans. Ind. Electron*., vol. 49, no. 1, pp. 186–196, Jan. 2002.

[18] A. Julian, T. Lipo, and G. Oriti, “Elimination of common-mode voltage in three-phase sinusoidal power converters,” *IEEE Trans. Power Electron*., vol. 14, no. 5, pp. 982–989, Sep. 1999.

[19] Y. Song, Y, B. Wang, "Survey on reliability of power electronic systems," *IEEE Trans. Power Electron*., vol. 28, no. 1, pp. 591-604, Jan. 2013.