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# A New Way of Controlling Parallel-Connected Inverters by Using Synchronous Reference Frame Virtual Impedance Loop – Part I: Control Principle

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***Abstract*—A novel simple and effective autonomous current-sharing controller for parallel three-phase inverters is proposed in this paper. The proposed controller provides faster response and better accuracy in contrast to the conventional droop control, since this novel approach does not require any active or reactive power calculations. Instead, a synchronous-reference-frame (SRF) virtual impedance loop and an SRF-based phase-locked loop are used. Stationary analysis is provided in order to identify the inherent mechanism of the direct and quadrature output currents in relation to the voltage amplitude and frequency with different line impedances by means of the system transfer functions. Comparison experiments from two parallel inverters are presented to compare the control performance of the conventional droop control and the proposed control with different line impedances. In addition, experimental results from a setup with three parallel 2.2 kW inverters verify the effectiveness of the proposed control strategy in different scenarios.**

***Index Terms*—Parallel inverters, synchronous reference frame, phase-locked loop, virtual impedance, droop control.**

## I. Introduction

DROOP control method has been widely used in the last decade as the decentralized control of parallel converters in several applications such as parallel redundant uninterruptible power supplies (UPS) to avoid critical communication among units, distributed power systems, microgrids (MGs), and so forth [1]-[12]. This well-known control technique aims to proportionally share active and reactive powers which adjusting frequency and output voltage amplitudes of each inverter locally in order to emulate the behavior of a synchronous generator [3]. Although this technique only requires local information, it presents a number of stability issues that have been solved along the literature [4]-[7].

One of the main problems is that the droop coefficients which regulate frequency and amplitudes are basically proportional terms, so that in order to increase their range of values for improving system dynamics, derivative terms were added [13]-[16]. Unlike the conventional droop controllers which yield 1- dimension of freedom (DOF) tunable control, the improved droop controllers yield 2-DOF tunable control. Subsequently, the dynamic performance of the system can be adjusted to damp the oscillatory behavior of the power sharing controllers without affecting the static droop gains.

Another issue with regards to conventional droop is that the frequency and voltage are respectively related to active and reactive power when the output impedance of the generator is mainly inductive, e.g. induction generators. Hence, by using the droop method, the power sharing performance is affected by the output impedance of the distributed generation (DG) units and the line impedances. However, the output impedance can be fixed by means of a fast control loop named virtual impedance in an inverter [17], [18]. In this sense, the output impedance can be treated as another control loop which enforces the inverter to behave in accordance to the inductance-to-resistance ratio (*X/R*) line impedance, e.g. mainly resistive in case of low voltage networks [19].

In case of resistive lines and/or virtual impedances, the active power is controlled by the inverter voltage amplitude, while the reactive power flow is dominated by the angle, so that it can be controlled by the frequency of the system [20]-[24]. In this sense, the active power-voltage (*P-V*) droop control needs to be used instead of the conventional active power-frequency (*P-f*) droop control, which is contrary to the conventional electrical transmission systems or induction generation dominated systems.

Several control methodologies with different implementations for conventional droop controller have been also proposed [25]-[28]. A $Q - V\ dot$ droop control method is mostly used to improve reactive power sharing [29].

Based on the abovementioned issues, a control architecture based on a virtual resistance, *P-V* and *Q-f* droops is used for dealing with the autonomous operation of parallel connected inverters [20], [30]. However, this approach has the inherent drawback that it needs to calculate instantaneous active and

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reactive powers and then average them through low-pass filters (LPF) whose bandwidth deteriorate the system transient response [15]. Even in three phase systems that the active and reactive power can be calculated by using the instantaneous power theory, a post-filter processing is necessary in order to completely remove the distorted power components [31]. Furthermore, in a practical situation, the load sharing performance of the conventional droop control is degraded when short lines with small impedance are used, especially in low voltage networks. In this case, a small deviation in voltage frequency and amplitude will result in large power oscillation and even instabilities [32]. The drawbacks of droop control can be summarized as listed below:

- Slow dynamic response: Since it requires LPFs with reduced bandwidth to calculate the average values of the active and reactive powers both in islanded and grid-connected modes.
- Active/reactive power coupling.
- Slow responses when active/reactive power sharing ratios are suddenly changed.
- Performance is serious affected by the line impedance.
- Complex design.
- The power sharing could be degraded if the sum of the output impedance and the line impedance is unbalanced.

Another possible solution is the combination of current sharing control and power droop control techniques. A voltage-power droop/frequency-reactive power boost (VPD/FQB) control scheme which allows multiple voltage source converters (VSCs) to operate in parallel in MGs and to share a common load power in proportion to a predetermined ration is presented in [33], [34]. In [33], an additional virtual resistance loop is necessary since the inverter output impedance cannot be equal to zero due to the PI controller in voltage control loop. A decentralized control for redundant parallel connection of multiple UPS using only current sensors is proposed [35], [36]. The active and reactive components of output current are used instead of active and reactive power to mimic the droop control, while the LPFs are still necessary. A novel piecewise linear V-I droop controller has been proposed to exploit the flexibility and fast dynamics of the inverter-based distributed energy resources [37], however a global positioning system (GPS) signal as the communication is used to synchronize each DG unit and allow for constant frequency operation. A voltage and frequency droop control based on mixed voltage and current source concept and finite output impedance emulation for single phase inverter based low voltage grid has been proposed [22], [38]. This method can provide not only wireless parallel operation control, but also has the capability of mitigation of voltage harmonics and short-circuit behavior as it takes the *R* to *X* line impedance ratio into account. However, this control approach is complex, since a Kalman filter estimator and a linear quadratic regulator are required.

To cope with all the aforementioned, a simpler and faster controller is proposed in this paper, which consists of a synchronous-reference-frame (SRF) virtual impedance loop, an SFR phase-locked loop (PLL) and a proportional-resonant (PR) controller in voltage control loop. The proposed control strategy provides both instantaneous current sharing and fast dynamic response for paralleled voltage controlled inverters (VCIs). The virtual resistance loop which contains a *d*-axis virtual resistance loop and a *q*-axis virtual resistance loop is used to achieve direct and quadrature load currents sharing separately among three-phase inverters. The concept is derived from the current-sharing control schemes already used in dc paralleled converters [39]-[42]. In contrast with the conventional droop control, there is no need to calculate active/reactive powers. An additional PLL is needed to adjust the phase of the voltage reference and ensure the synchronization among the paralleled VCIs. The paper is organized as follows. Section II reviews the conventional droop control principle. Section III analyzes the current flow when virtual resistive impedance in the stationary reference frame is used. Section IV introduces the proposed control structure and the control principle. Section V presents the inherent droop characteristic and coupling analysis of the proposed control with different line impedances. Experimental results are shown in Section VI in order to evaluate the feasibility of the proposed approach and to compare the control performance with the conventional droop control. Section VII concludes the paper. Finally, the appendix provides the derivative process of the mathematic equations. This paper is the first part of a two-part paper focusing on the control principle and steady state performance analysis. The second part of this paper deals with the small-signal state-space models and stability analysis of the proposed parallel-VCI-based system.

## II. Review of the Droop Control Principle

Fig. 1 shows the equivalent circuit of a two-paralleled inverter system including generated voltages ($\vec{V}_{g1}$ and $\vec{V}_{g2}$), output impedances ($\vec{Z}_{o1}$ and $\vec{Z}_{o2}$), virtual impedances ($\vec{Z}_{vir1}$ and $\vec{Z}_{vir2}$), output voltage ($\vec{V}_{o1}$ and $\vec{V}_{o2}$) and line impedances ($\vec{Z}_{line1}$ and $\vec{Z}_{line2}$) of each inverter. It can be considered as a subset of distributed power network operating in autonomous islanded mode.

The phase differences between the output voltage ($\varphi_{gn}$) and the point of common coupling (PCC) voltage ($\varphi_{bus}$), as well as the amplitude of equivalent impedance ($Z_n\angle\varphi_n$), which consists of inverter output impedance ($Z_{on}\angle\varphi_{oZn}$), line impedance ($Z_{linen}\angle\varphi_{linen}$), and virtual impedance ($Z_{virn}\angle\varphi_{virn}$), are considered in this study. The active and reactive power output can be derived as:

$$P_n = \frac{V_{gn}^2\cos\varphi_n - V_{gn}V_{bus}\cos(\varphi_{gn}-\varphi_{bus}+\varphi_n)}{Z_n} \tag{1}$$

$$Q_n = \frac{V_{gn}^2\sin\varphi_n - V_{gn}V_{bus}\sin(\varphi_{gn}-\varphi_{bus}+\varphi_n)}{Z_n} \tag{2}$$

In traditional power systems, the equivalent impedances between the paralleled inverters present high *X/R* ratio. The

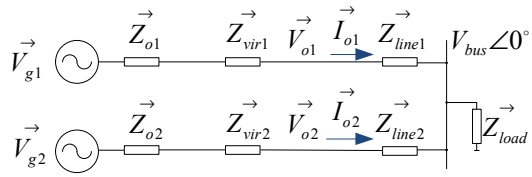



Fig. 1. Equivalent circuit of a parallel inverter system with virtual resistances.

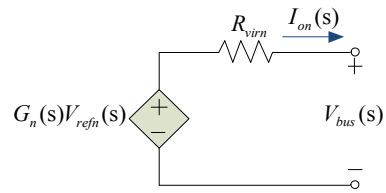



Fig. 2. Equivalent Thévenin circuit of closed-loop inverter.

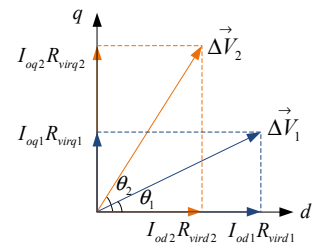



Fig. 3. Vector diagram of the concept.

active power ( $P_n$ ) can be adjusted with the voltage angle ($\varphi_{gn}$), and reactive power ( $Q_n$ ) can be regulated with voltage amplitude ($V_{gn}$) separately. Based on this power flow analysis, the droop control law can be expressed as:

$$\omega_n = \omega_n^* + k_{p\omega}(P_n^* - P_n) \tag{3}$$

$$V_n = V_n^* + k_{qV}(Q_n^* - Q_n) \tag{4}$$

where $\omega_n^*$ and $V_n^*$ are the normal angular frequency and output voltage amplitude, respectively, $k_{p\omega}$ and $k_{qV}$ are the droop coefficients.

However, the load sharing performance of the conventional droop control is degraded in a practical situation when using short lines with small impedances, especially in low voltage networks. Output power ( $P_n$ and $Q_n$ ), output voltage amplitude and frequency are coupled, because $[\sin(\varphi_{on} - \varphi_{bus})]/Z_n \approx (\varphi_{on} - \varphi_{bus})/Z_n$ cannot be neglected when $\varphi_n - \varphi_{bus} \neq 0$ or $Z_n$ is too small, that may result in imprecise power control. Furthermore, the stability problems would arise for conventional droop controlled systems with small equivalent line impedance $Z_n$, since small frequency or voltage amplitude deviations can result in large power oscillations.

## III. Current Flow Analysis

Each inverter in Fig.1 can be modeled by a two-terminal Thévenin equivalent circuit in Laplace as follows:

$$V_{bus}(\mathrm{s}) = G_n(\mathrm{s})V_{refn}(\mathrm{s}) - [Z_{on}(\mathrm{s}) + Z_{linen}(\mathrm{s}) + Z_{virn}(\mathrm{s})]I_{on}(\mathrm{s}) \tag{5}$$

where $V_{refn}(\mathrm{s})$ is the output voltage reference; $G_n(s)$ is the voltage gain. The inner current and voltage loops are responsible for minimizing $Z_{on}(s)$, i. e. by using a proportional + resonant (PR) controller tuned at the line frequency. In this sense, $Z_{on}(s)$ is approximately equal to zero, whereas $G_n(\mathrm{s})$ is equal to 1 at the resonant frequency of PR controller.

Considering that $Z_{linen}(s)$ is practically very small in low scale systems such as low voltage MGs, $Z_{virn}(\mathrm{s})$ becomes the predominant component. Thus, (5) can be simplified as:

$$V_{bus}(\mathrm{s}) = G_n(\mathrm{s})V_{refn}(\mathrm{s}) - Z_{virn}(\mathrm{s})I_{on}(\mathrm{s}) \tag{6}$$

When only virtual resistance is adopted, an equivalent Thévenin circuit can present the closed loop inverter, as illustrated in Fig. 2. The voltage difference between the generated voltage and common bus voltage at the line frequency can be expressed in *dq* reference frame as follows:

$$\vec{V}_{refn} - \vec{V}_{bus} = I_{odn}R_{virdn} + jI_{oqn}R_{virqn} \tag{7}$$

where $I_{odn}$ and $I_{oqn}$ are the *d* and *q*-axis components of output current, respectively.

In this case, because the voltage reference phasor ($\vec{V}_{ref}$) and common bus voltage phasor ($\vec{V}_{bus}$) are identical for each DG unit, the different values of $R_{vird}$ and $R_{virq}$ will result in different voltage drop that will cause different current output vectors ( $\vec{I}_o$ ), as shown in Fig. 3. The relationship of $I_{od}$, $I_{oq}$, $R_{vird}$ and $R_{virq}$ can be generalized and expressed for number *N* of converters as follows:

$$I_{od1}R_{vird1} = I_{od2}R_{vird2} = \ldots = I_{odN}R_{virdN} \tag{8a}$$

$$I_{oq1}R_{virq1} = I_{oq2}R_{virq2} = \ldots = I_{oqN}R_{virqN} \tag{8b}$$

The *d*- and *q*-axis output currents $I_{od}$ and $I_{oq}$ of the paralleled inverters are inversely proportional to the corresponding virtual resistances. Therefore, the direct and quadrature currents output of each inverter can be regulated independently by adjusting the virtual impedances based on different power rates, commands from energy management system (EMS) or other superior control loops.

Furthermore, the active and reactive power output sharing strategy among the paralleled inverters can be obtained from (8) by multiplying the voltage reference. Hence, considering that the voltage references ($V_{ref}$) of each inverter are equal, the active and reactive power output will also be properly shared based on the virtual resistances, as shown in (9):

$$P_{o1}R_{vird1} = P_{o2}R_{vird2} = \ldots = P_{oN}R_{virdN} \tag{9a}$$

$$Q_{o1}R_{virq1} = Q_{o2}R_{virq2} = \ldots = Q_{oN}R_{virqN} \tag{9b}$$

where $P_{on}$ and $Q_{on}$ are the active and reactive power output of inverter #*n*.

## IV. Proposed Autonomous Current-Sharing Controller

Follow the above analysis, a simpler and faster controller is proposed in this paper. The novel control strategy is shown in Fig. 4(b). Compared with the improved droop controller in Fig. 4(a), the droop controller could be replaced by a novel controller which comprises of an SRF-PLL and a virtual resistance loop in SRF.

### A. Configuration of the proposed controller

The power stage consists of a three-leg three-phase inverter connected to a DC link, loaded by an $L_f$-$C_f$ filter, and connected to the AC bus through a power line ($Z_{line}$). Indeed, the proposed control strategy can also be extended to single-phase systems. The main difference between the single-phase systems and three-phase systems is that the orthogonal voltage system in single-phase systems needs to be generated by an extra control loop [43], [44].

The controller including an SRF-PLL, a virtual resistance loop ($R_{vird}$ and $R_{virq}$), a DC link voltage feed-forward loop, and the conventional PR inner voltage and current controllers ($G_v$ and $G_i$) generates a PWM signal to drive the IGBT inverter gates. Inductive currents and capacitor voltages are transformed to the stationary reference frame ( $i_{L\alpha\beta}$ and $v_{c\alpha\beta}$ ). Output currents are transformed to the SRF ( $i_{odq}$ ). The direct and quadrature output currents are independently controlled by the virtual impedance loop in *dq* axis. The inner voltage and current loops are implemented in $\alpha\beta$ reference frame since the PR controller can deal with both positive and negative sequence voltage when the negative sequence voltage and current appear.

Fig. 5 shows the simplified proposed control block diagram, which includes the three-leg three-phase inverter, $L_f$-$C_f$ filter, line impedance, virtual impedance loop, the PLL and the inner voltage and current control loops.

The closed loop transfer function $T_{plant}(s)$ can be described as follows:

$$T_{plant}(s)=\frac{V_o(s)}{V_{ref}(s)}=\frac{G(s)\left[1+G_{Lequ}(s)Z_{line}(s)\right]}{1+G_{Lequ}(s)Z_{line}(s)+G_{vir}(s)G(s)+G_{Lequ}(s)Z_o(s)} \tag{10}$$

being

$$G(s)=\frac{G_v(s)G_i(s)K_{PWM}}{L_fC_fs^2+(rC_f+G_i(s)K_{PWM}C_f)s+1+G_v(s)G_i(s)K_{PWM}}$$

$$Z_o(s)=\frac{sL_f+r}{L_fC_fs^2+(rC_f+G_i(s)K_{PWM}C_f)s+1+G_v(s)G_i(s)K_{PWM}}$$

$$G_v(s)=K_{pv}+\frac{K_{iv}s}{s^2+\omega_c^2},\ G_i(s)=K_{pi},\ G_{Lequ}(s)=\frac{1}{R_{Lequ}}+\frac{1}{sL_{Lequ}}$$

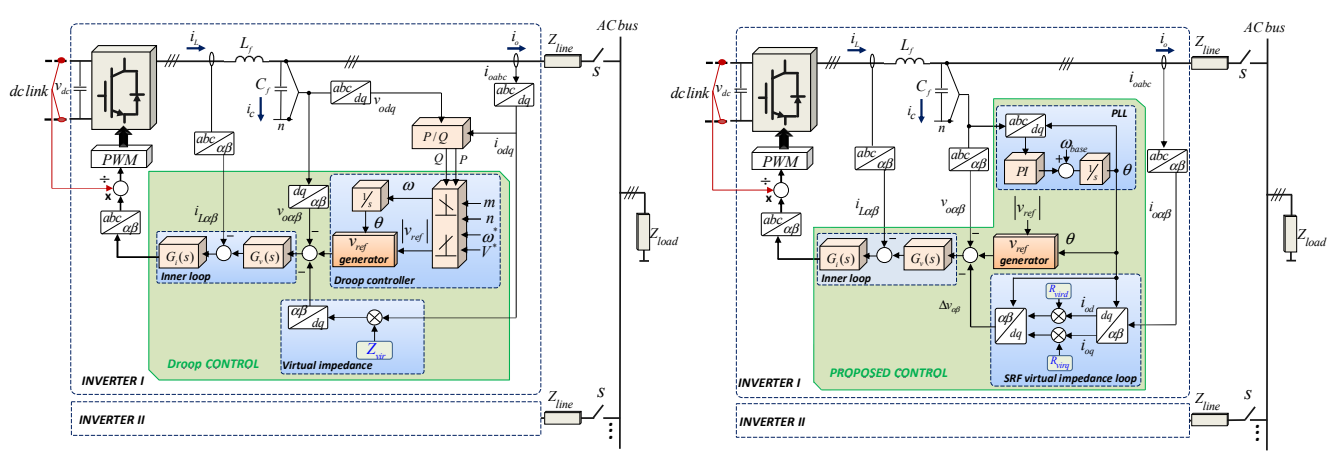
$$Z_{line}(s)=R_{line}+sL_{line},\ G_{vir}(s)=\frac{R_{vird}}{R_{Lequ}}+\frac{R_{virq}}{sL_{Lequ}}$$

where *G(s)* presents the tracking performance of the output voltage following the voltage reference, $Z_o(s)$ is the equivalent output impedance of the inverter, $Z_{line}(s)$ is the line impedance, $R_{line}$ is the line resistor, $L_{line}$ is the line inductance, $G_{Lequ}(s)$ is the equivalent load admittance, $R_{Lequ}$ is the equivalent resistor, $L_{Lequ}$ is the equivalent inductance, $V_o(s)$ is the output voltage, $V_{ref}(s)$ is the reference voltage, $i_o(s)$ is the output current, $G_v(s)$ is the PR voltage control loop, $G_i(s)$ is the proportional current control loop, $K_{PWM}$ is the gain of three phase inverter, $L_f$ , $C_f$ and *r* are the inductor, capacitor, and inductor ESR of *LC* filter respectively, $K_{pv}$ and $K_{iv}$ are the proportional and integral coefficients of voltage control loop, $\omega_c$ is the resonant frequency of the PR voltage control loop, $K_{pi}$ is the proportional coefficients of current control loop, $R_{vird}$ and $R_{virq}$ are the *d*-axis and *q*-axis virtual resistors.

The detailed derivative process is provided in the Appendix.

### B. Control Principle

The proposed controller supplies a reference voltage to the




(a) (b)

Fig. 4. Control structure comparison between (a) the conventional droop control and (b) the proposed control method.

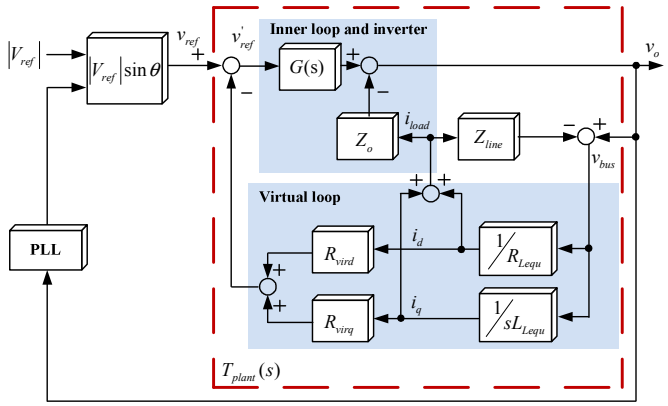



Fig. 5. Simplified control block diagram.

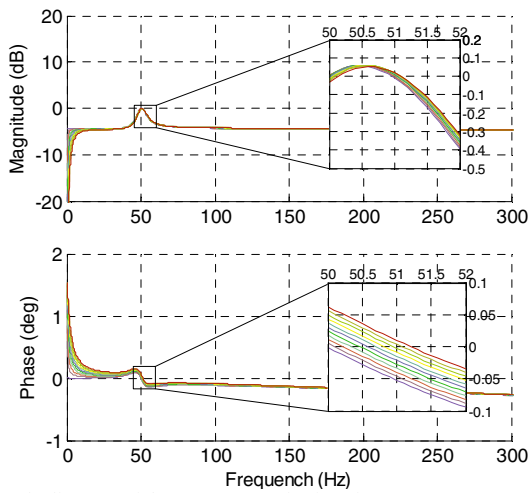



Fig. 6. Bode diagram of the system transfer function.

inner loop. The voltage reference $\vec{V}_{ref}$ is generated by combining the amplitude reference ($|V_{ref}|$) and the phase generated ($\theta$) by the PLL.

Even though the PLL is trying to synchronize the inverter with common AC bus, in case of supplying reactive loads, the quadrature current flowing through the virtual resistance will produce an unavoidable quadrature voltage drop, which will cause an increase in PLL frequency. In other words, the PLL will compel the inverter to be stabilized at a frequency point with zero phase delay (ZPD) obtained from the system transfer function. The frequency of ZPD is affected by the quadrature current as shown in Fig. 6. Thus, the mechanism inherently endows an $I_{oq}-\omega$ droop characteristic in each inverter.

Similarly, in case of supplying active loads, the direct current flowing through the virtual resistance will drop the direct voltage, causing a decrease in the output voltage amplitude. Hence, a droop characteristic is also imposed by the virtual resistance adapting the amplitude of output voltage, which endows to the system an $I_{od}-V$ droop characteristic.

Moreover, the settling time can be considerably improved because the proposed controller does not require any power calculation. The bandwidth of the PLL can be designed through the linearized model [45], [46] to be higher than the bandwidth of the LPF that is used for *PQ* calculation purposes in the

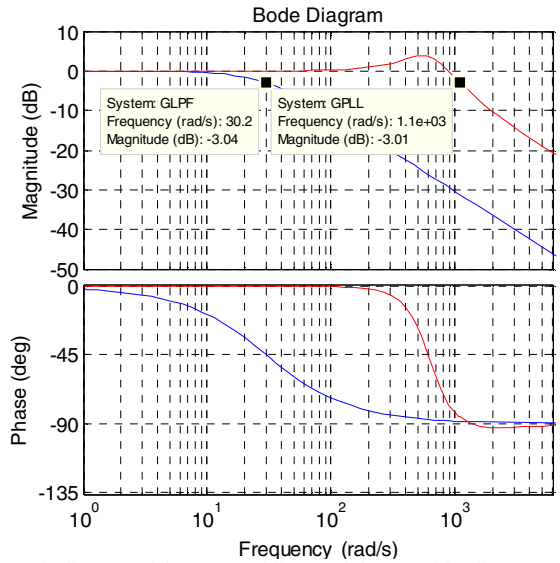



Fig. 7 Bode diagram of the PLL (red line) and the LPF (blue line)

conventional droop controller [47]. The cutoff frequency of the LPF in the power droop control loop is usually preassigned to 30 rad/s to obtain the average power while avoiding undesirable interaction [45], [46]. The bandwidth of the PLL in the proposed control is 1100 rad/s when $k_{p_PLL}$ and $k_{i_PLL}$ are equal to 1.4 and 1000 respectively. The Bode diagram is shown in Fig. 7. However, the fastest transient response of PLL should be almost equal to the transient response speed of the inner voltage control loop to ensure the system stability.

## V. Inherent Droop Characteristic and Coupling Analysis

Considering the inherent mechanism of $I_{od}$ with voltage amplitude and $I_{oq}$ with frequency, two virtual resistances $R_{vird}$ and $R_{virq}$ are employed to share the quadrature and direct load currents among the inverters individually.

### A. $I_{oq}$ sharing

When the inverters and loads all connect to the common AC bus, the proposed controller will make the system stable at a frequency-stable operation point which may has a small deviation from 50 Hz. The small deviation is determined by the function of PLL, $R_{virq}$ and $I_{oq}$. The frequency-stable operation should be the cross zero point of the phase-frequency characteristics of the closed-loop transfer function of the system, as depicted in the dashed part in Fig. 5.

Therefore, the parallel inverters will operate on the same system frequency, but with different phase angles that depend on the output quadrature current and *q*-axis virtual resistance value.

Based on (10), as $s=j\omega$, the relationship of $R_{vird}$, $R_{virq}$, $I_{od}$, $I_{oq}$ and angular frequency ($\omega$) can be calculated based on

$$arc\tan\left[T_{plant}(j\omega)\right]=0^{\circ} \tag{11}$$

In order to analyze the relationship of $R_{virq}$, $I_{oq}$ and $\omega$, $R_{vird}$ and $I_{od}$ are preset to a fixed value. The relationship of $R_{virq}$, $I_{oq}$ and $\omega$ with different line impedances is shown in Fig. 8. Figs. 8 (a.1) and 8 (b.1) show the relationship with zero line impedance. Figs. 8 (a.2) and 8 (b.2) describe the relationship with resistive-inductive line impedance ($L_{line}$ = 1.7 mH, $R_{line}$ = 1 Ω). Figs. 8 (a.3) and 8 (b.3) present the relationship with purely inductive line impedance ($L_{line}$ = 1.8 mH). The inherent mechanism of the proposed $I_{oq}-\omega$ droop controller with different line impedances are depicted in Figs. 8 (b.1), 8 (b.2) and 8 (b.3). Fig. 8 indicates that the line impedances in this range barely have effect on the relationship of $R_{virq}$, $I_{oq}$ and $\omega$, as well as $I_{oq}-\omega$ droop characteristics. This is because the influence of the inductive line impedance in this range has been compensated by the virtual resistors. As observed in Figs. 8 (b.1), 8 (b.2) and 8 (b.3), the quadrature current sharing among the parallel inverters can be adjusted by regulating the *q*-axis virtual resistance ratio.

By contrast, the relationships of variables $R_{vird}$, $I_{od}$ and $\omega$ with different line impedances are derived by assigning $R_{virq}$ and $I_{oq}$ to certain values. The relationships of $R_{vird}$, $I_{od}$ and $\omega$ with zero, resistive-inductive, and purely inductive line impedance are shown in Figs. 9 (a.1) to 9 (a.3) respectively. Additionally, Figs. 9 (b.1), 9 (b.2) and 9 (b.3) are obtained by assuming $R_{vird}$ to different values based on the relationships of $R_{vird}$, $I_{od}$ and $\omega$ under different line impedance conditions.

As observed from Figs. 9 (b.1) to 9 (b.3), the influence of direct output current on angular frequency changes by an exponential dependence when it getting closer to the resonance frequency of PR controller, which means that the impact of $R_{vird}$ and $I_{od}$ on $\omega$ can be neglected.

### B. $I_{od}$ sharing

In order to share active loads, the parallel inverters will have different output voltage amplitude deviations from the voltage amplitude reference $|V_{ref}|$, which depend on the output direct current and *d*-axis virtual resistance value of each inverter.

The voltage drop ($\Delta V$) can be divided into two parts as follows:

$$\Delta V = I_{od} R_{vird} + |V_{ref}| \left[ 1 - \left| T_{plant}(\mathrm{j}\omega_0^{'}) \right| \right] \tag{12}$$

where the $\omega_0^{'}$ is the angular frequency of frequency-stable operation point.

The first part of (12) is the product of *d*-axis virtual resistance $R_{vird}$ and direct current output $I_{od}$, which dominantly affects the output voltage amplitude drop. The second part of (12) is caused by the magnitude attenuation of closed-loop transfer function which results from the small but nonlinear frequency deviation due to the characteristic of PR controller. However, as discussed above, the system frequency will be stable and the deviations among the parallel inverters will be equal to each other, that is, the voltage deviations resulting from the second part of (12) are also the same among inverters. Therefore, the influence on the deviations can be neglected. Thus, the per-unit value of output voltage amplitude can be derived from (10) as follows:

$$\frac{|V_o|}{|V_{ref}|} = \left| T_{plant}(\mathrm{s}) \right| = f(I_{od}, I_{oq}, R_{vird}, R_{virq}, \omega) \tag{13}$$

The parameters of $R_{virq}$ and $I_{oq}$ are fixed to analyze the

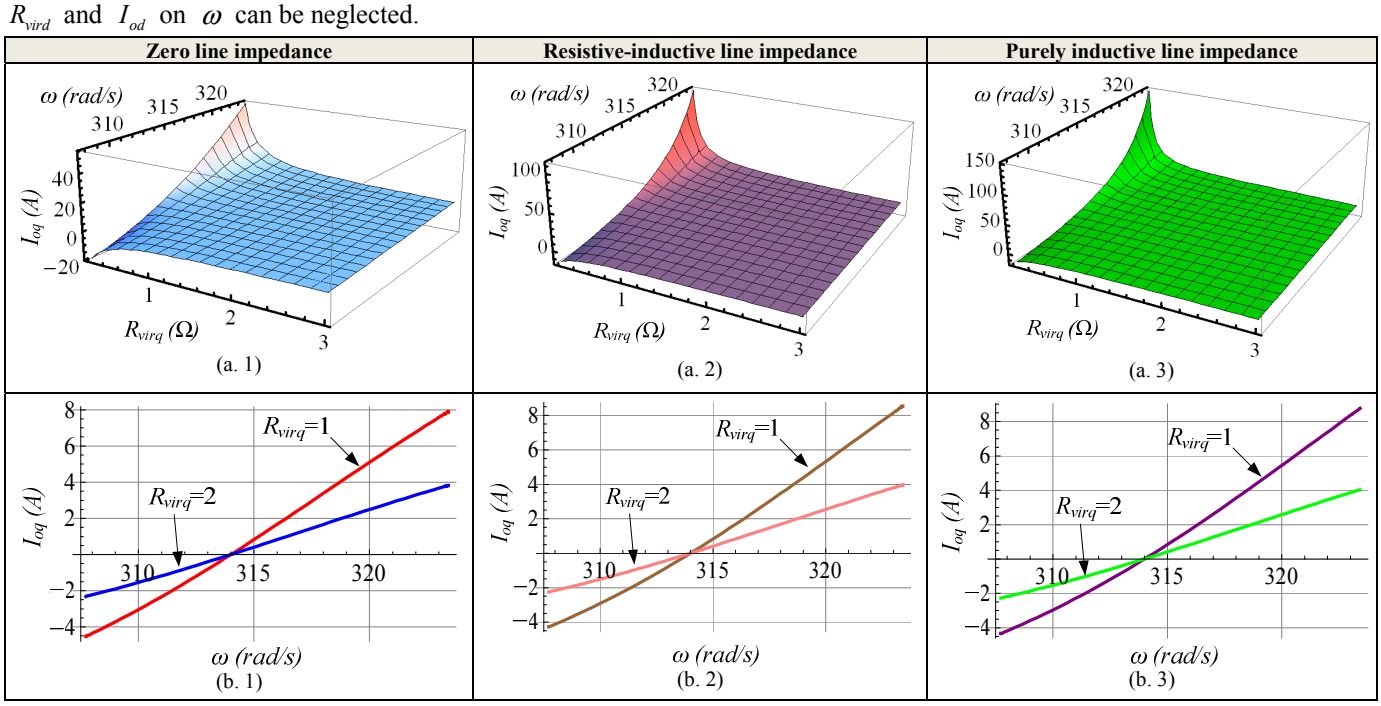



Fig. 8. The relationship of $R_{virq}$, $I_{oq}$ and $\omega$ with different line impedances. (a) The relationship of $R_{virq}$, $I_{oq}$ and $\omega$ with different line impedances, (b) The relationship of $I_{oq}$ and $\omega$ when $R_{virq}$=1Ω/2Ω with different line impedances.

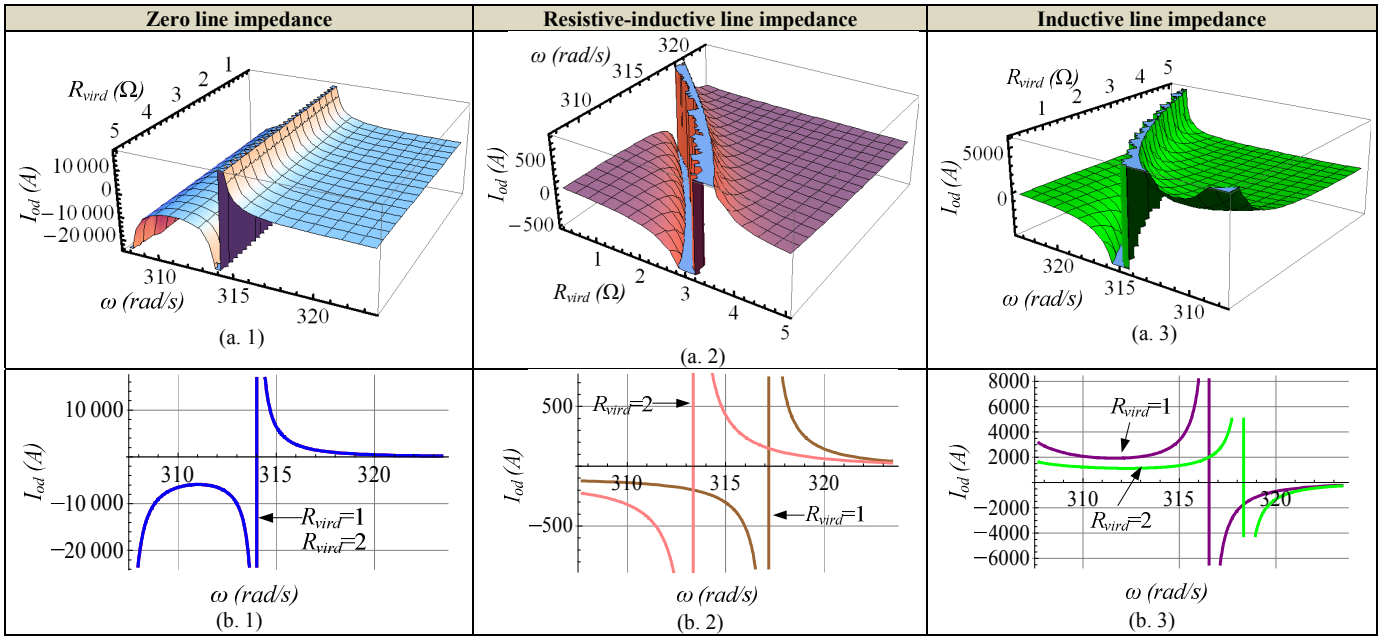



Fig. 9. The relationship of $R_{vird}$, $I_{od}$, and $\omega$ with different line impedances. (a) The relationship of $R_{vird}$, $I_{od}$, and $\omega$ with different line impedances, (b) The relationship of $I_{od}$ and $\omega$ when $R_{vird}$=1Ω/2Ω with different line impedances respectively.

relationship of $R_{vird}$, $I_{od}$ and $V_o$. The relationship of $R_{vird}$, $I_{od}$ and $V_o$ with zero, resistive-inductive, and purely inductive line impedances line impedance are shown in Fig. 10. As it can be seen that the line impedances in the certain range barely have effect on the relationship of $R_{vird}$, $I_{od}$ and $V_o$. Figs. 10 (b.1) to 10 (b.3) shows the inherent $I_{od}-V_o$ droop mechanism of the proposed controller under different line impedance conditions. As observed, as the output direct current $I_{od}$ increases, the voltage amplitude $V_o$ decreases with different ratio corresponding to different $R_{vird}$ values. Thus, the direct current sharing among the parallel inverters can be adjusted by regulating the *d*-axis virtual resistance ratio.

Similarly, $R_{vird}$, $I_{od}$ are fixed to analyze the effect of frequency deviation on the voltage amplitude $V_o$ with different line impedances. The relationships of $R_{virq}$, $\omega$ and $V_o$ with zero, resistive-inductive, and purely inductive line impedance are shown in Figs. 11 (a.1) to 11 (a.3) respectively. Figs. 11 (b.1) to 11 (b.3) indicate that the relationship $V_o-\omega$ almost immune

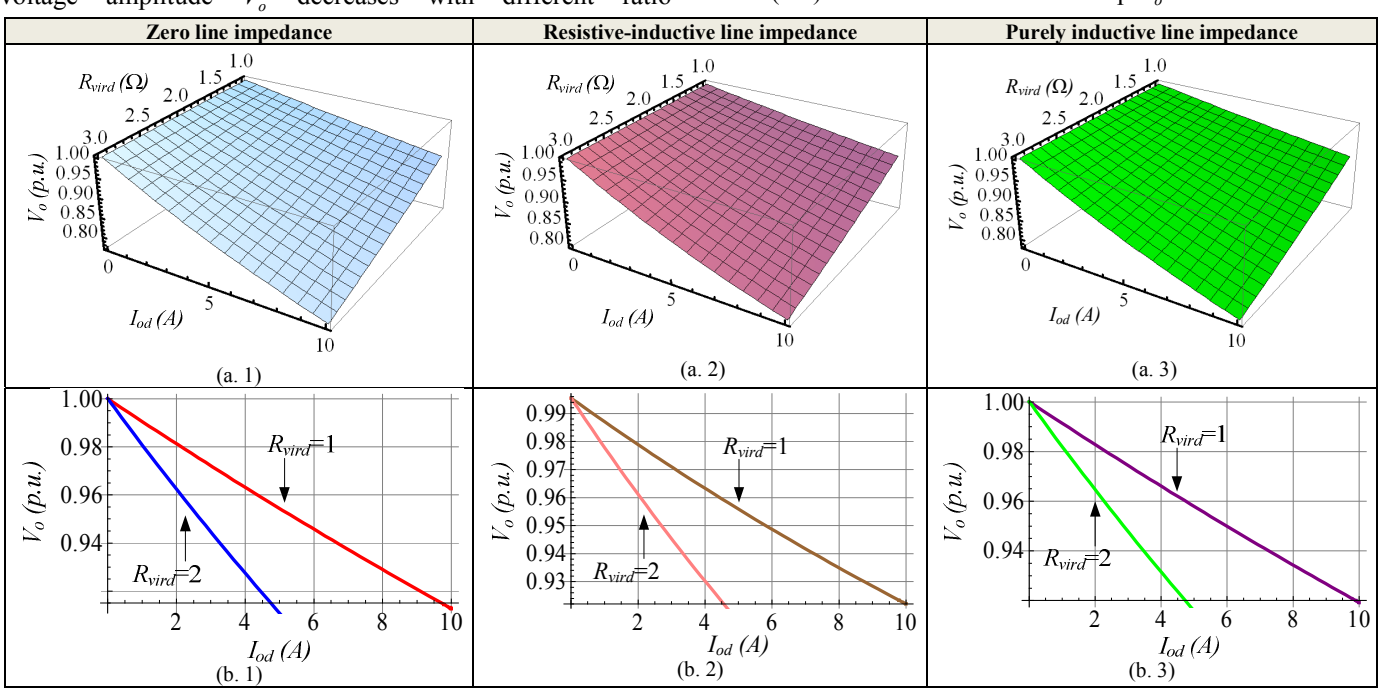



Fig. 10. The relationship of $R_{vird}$, $I_{od}$ and $V_o$ with different line impedances. (a) The relationship of $R_{vird}$, $I_{od}$ and $V_o$ with different line impedances, (b) The relationship of $I_{od}$ and $V_o$ when $R_{vird}$=1Ω/2Ω with different line impedances respectively.

to both $R_{virq}$ and different line impedances. The effects of $R_{virq}$ and $\omega$ on $V_o$ are nonlinear but quite small in comparison with the voltage drop caused by adjusting $R_{vird}$ and $I_{od}$. Considering that the voltage drop caused by $\Delta\omega$, is approximately the same in each inverter, it can be neglected.

Consequently, it can be observed a very well decoupling between $I_{od}$ and $I_{oq}$ for a large set of $X/R$ ratios (from purely $X$ to purely $R$).

### C. Virtual impedance design

The virtual impedances in the proposed control loop are used to generate the direct and quadrature voltage deviations by multiplying the direct or quadrature currents separately. The direct and quadrature voltage deviations are used to automatically adjust the amplitude and phase angular of inverter output voltage. Given that virtual impedances induce output voltage and frequency deviation, they should be chosen to ensure that the voltage and frequency deviations are in the permissible range. For example, the maximum voltage deviation ($\Delta V_{max}$) is 10%, while the maximum frequency deviation ($\Delta f_{max}$) is 0.5 Hz in a low voltage network.

The relationship between the maximum voltage magnitude deviation $\Delta V_{dmax}$ and $I_{od}$ can be derived as follows:

$$\Delta V_{d\max} = R_{vird} \cdot I_{od} \tag{14}$$

In an extreme case, the inverter is assumed to supply only active current. (1) can be presented as follows:

$$\Delta V_{\max} = R_{vird_\max} \cdot I_{od_\max} \tag{15}$$

where, $I_{od_\max}$ is the maximum $d$-axis current of the inverter.

Thus, the upper limitation of the $d$-axis virtual resistor can be described as follows:

$$R_{vird_\max} = \Delta V_{\max} \big/ I_{o_rate} \tag{16}$$

Similarly, in an extreme case, the inverter is assumed to supply only reactive current. The relationship between the maximum angular frequency $\omega_{\max}$, quadrature output current $I_{oq}$ and $R_{virq}$ can be derived from (11), as expressed in (17):

$$R_{virq_\max} = \frac{num}{den} \tag{17}$$

being:

$$num = V_{ref}\omega_{\max}(\omega_{\max}{}^2 - \omega_o{}^2)[K_{iv}(1 + C_f L_f \omega_{\max}{}^2) + C_f K_{pv}(K_{pi}K_{PWM} + r)(\omega_{\max}{}^2 - \omega_o{}^2)]$$

$$den = I_{oq_\max} K_{pi} K_{PWM}[\omega_{\max}{}^2(K_{iv}{}^2 + K_{pv}{}^2\omega_{\max}{}^2) + K_{pv}{}^2\omega_o{}^2(\omega_o{}^2 - 2\omega_{\max}{}^2)],$$

where $V_{ref}$ is the voltage reference magnitude, $\omega_o$ is the fundamental frequency, $K_{PWM}$ is the gain of three-phase inverter, and $I_{od_\max}$ is the maximum $d$-axis current output of the inverter.

This relationship is more complex than the relationship of $\Delta V_{dmax}$, $I_{od_max}$ and $R_{vird_max}$ because the frequency of the proposed system is affected not only by the virtual resistance and quadrature current but also by the PR voltage control loop. Based on (17), the maximum $q$-axis virtual resistance can be calculated.

On the other hand, another functionality of the virtual

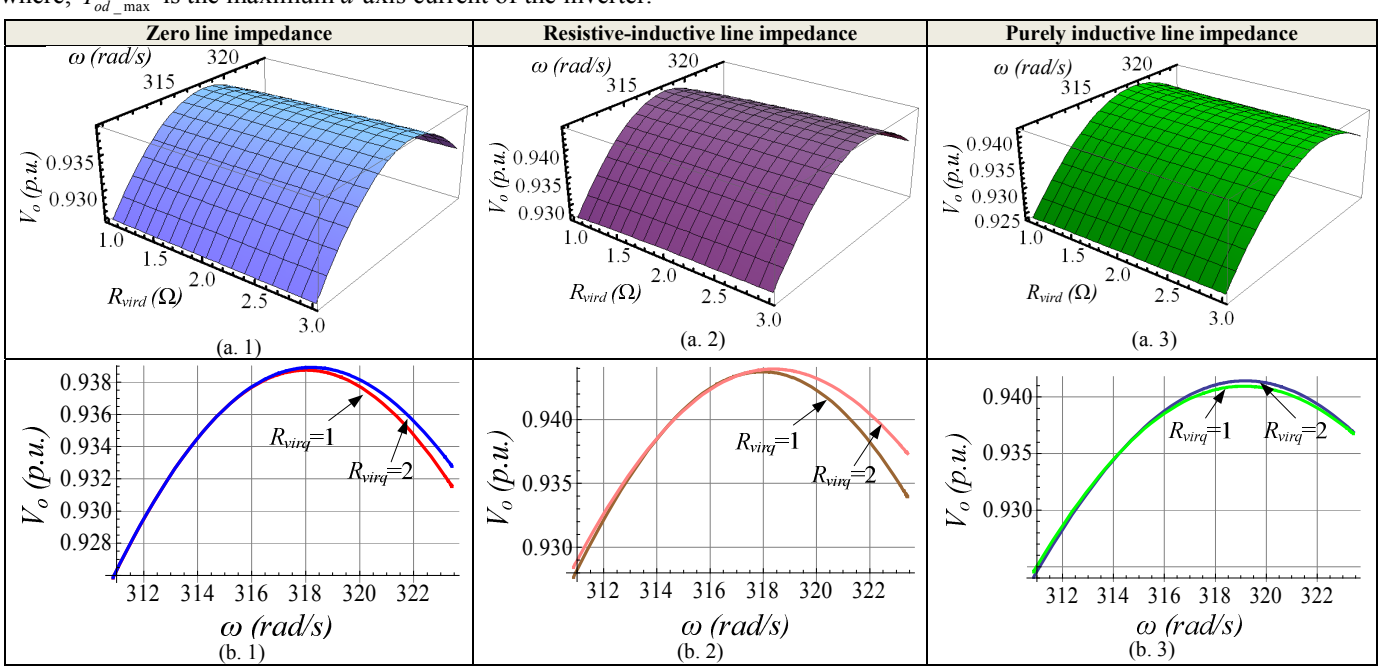



Fig. 11. The relationship of $R_{virq}$, $\omega$ and $V_o$ with different line impedances. (a) The relationship of $R_{virq}$, $\omega$ and $V_o$ with different line impedances, (b) The relationship of $\omega$ and $V_o$ when $R_{virq}$=1Ω/2Ω with different line impedances respectively.

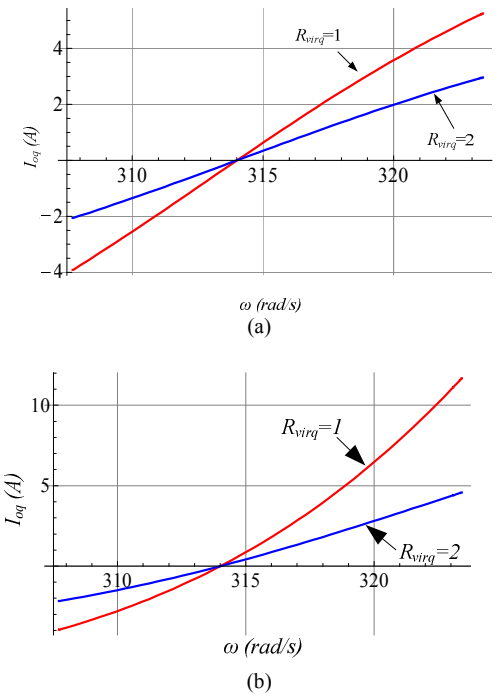



Fig. 12. The relationship of $I_{oq}$ and $\omega$ when the line impedances are equal to the maximum values. (a) $L_{line}$ is equal to 6 mH, (b) $R_{line}$ is equal to 15 Ω.

resistance is to compensate the effects of line inductance. Thus, the virtual resistor should not too small to predominate over the output impedance of the converter.

### *D. The limitations of the line impedance*

The limitations of the line impedance depend on the control loop parameters, the virtual impedance and electrical parameters. In this case, if the $R_{vird}$ and $R_{virq}$ are both equal to 2 Ω, the maximum inductive line impedance and the maximum resistive line impedance that are able to maintain the steady state operation of the proposed parallel-inverter based system can be calculated by (11). The maximum inductive line impedance and the maximum resistive line impedance are approximately 6 mH and 15 Ω respectively. The proposed $I_{od}-V_o$ and $I_{oq}-\omega$ droop characteristics will present non-linear when the line impedance over the limitations, as illustrated in Fig. 12.

In general, the proposed control strategy can provide good control performance over a wide range of line impedance which is hard to achieve by previously developed control strategies.

## VI. Experimental Results

An islanded experimental MG setup, which consists of three Danfoss 2.2 kW inverters, a real-time dSPACE1006 platform, *LC* filters, line impedance, resistive load and resistance -inductance load has been built according to Fig.1, as shown in Fig. 13. The switching frequency is set to 10 kHz. The electrical setup and control system parameters are listed in Table I. Different scenarios have been considered to test the performances of the proposed controller. In addition, a two parallel-inverters system has been used to compare and evaluate the performance of the proposed control approach

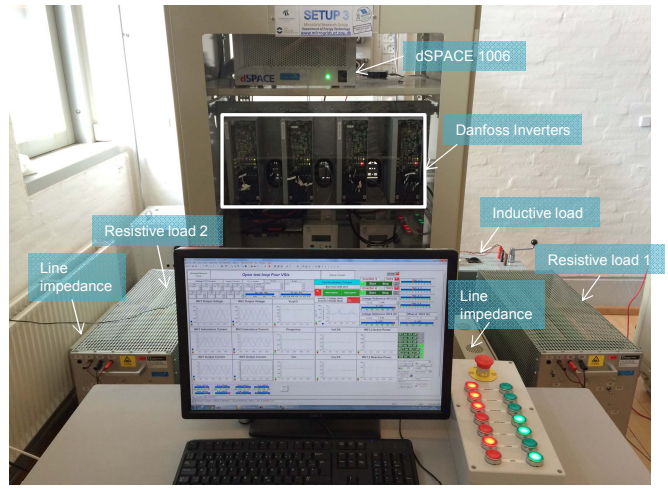



Fig. 13. Experimental setup.

TABLE I
Power Stage and Control System Parameters

| | Parameters | | Value |
|---|---|---|---|
| | | Description | |
| DG Inverter and output filter | $V_{dc}$ | DC voltage | 650 V |
| | $V_{MG}$ | MG voltage | 311 V |
| | $f$ | MG frequency | 50 Hz |
| | $f_s$ | Switching frequency | 10 kHz |
| | $L_f$ | Filter inductance | 1.8 mH |
| | $C_f$ | Filter capacitance | 25 μF |
| | $L_{line_1}$ | Resistive – inductive line | 1 Ω + 1.7 mH |
| | $L_{line_2}$ | Inductive line | 1.8 mH |
| Loads (Figs. 16 and 17) | $Z_{load1}$ | Local load 1 | 57+j2.83 Ω |
| | $Z_{load2}$ | Local load 2 | 57 Ω |
| Inner Loop | $k_{pi}$ | Current proportional term | 0.07 |
| | $K_{ii}$ | Current integral term | 0 |
| | $K_{pv}$ | Voltage proportional term | 0.04 |
| | $K_{iv}$ | Voltage integral term | 94 |
| Droop Control | $k_{pP}$ | Active power droop proportional coefficient | 5e-7 |
| | $k_{iP}$ | Active power droop integral coefficient | 6e-6 |
| | $k_{pQ}$ | Reactive power droop proportional coefficient | 1e-5 |
| | $k_{iQ}$ | Reactive power droop integral coefficient | 0 |
| | $R_v$ | Virtual resistance | 2 Ω |
| | $L_v$ | Virtual inductance | 8 mH |
| Proposed Control | $K_{p_PLL}$ | PLL proportional term | 1.4 |
| | $K_{i_PLL}$ | PLL integral coefficient | 1000 |
| | $R_{vird1}$ | d-axis virtual resistance (inverter 1) | 2 Ω |
| | $R_{virq1}$ | q-axis virtual resistance (inverter 1) | 2 Ω |
| | $R_{vird2}$ | d-axis virtual resistance (inverter 2) | 2 Ω |
| | $R_{virq2}$ | q-axis virtual resistance (inverter 2) | 2 Ω |
| Loads (Figs. 14 and 15) | $Z_{load}$ | Local load 1 | 230+ j2.83 Ω |
| | $Z_{test}$ | Step up load | 460 Ω |

with the conventional droop control. In this comparison, the parameters of electrical and inner voltage and current loops are all the same for both control methods.

### *A. Comparison experiment with inductive line impedance*

Fig. 14 shows the experimental results to compare the control performance of the conventional droop control and the proposed control with purely inductive line impedance which is equal to 1.8 mH in three different scenarios. Figs. 14 (a.1) to 14 (a.6) shows the transient response when VCI #2 is connected to VCI #1 with the conventional droop controller and the proposed controller separately. As seen in Figs. 14 (a.1) to 14 (a.4), VCI #1 is connected to a resistive-inductive load feeding around (1.16+j 0.4) A, while VCI #2 is disconnected. At 2.3 s, VCI #2 is connected to VCI #1, operating in parallel supplying a common load. The direct and quadrature currents output of VCI #2 are increased by 0.58 A and 0.2 A respectively, whereas the output direct and quadrature currents of the VCI #1 are decreased also by 0.58 A and 0.2 A respectively. The settling time is approximately 5.2 s with the conventional droop control, whereas the settling time is approximately 1s with the proposed control strategy. Notice that a small overshoot occurs due to small voltage error between inverters at the moment of connection, as shown in Fig. 14 (a.3). An offset approximately 0.03 A of reactive current when using the droop control can be found in Fig. 14 (a.3) due to the unbalance between line impedances, which is well suppressed when using the proposed controller as shown in Fig. 14 (a.4). Fig. 14 (a.5) shows that after 1.2 s the system frequency at 49.992 Hz was restored closely to 49.996 Hz because of the decrease of the output currents with conventional droop control. As can be observed in Fig. 14 (a.6), the system frequency at 50.035 Hz was restored to50.018 Hz. All these deviations in both cases are maintained within the acceptable range, e.g., ±0.5 Hz.

Fig. 14 (b.1) to 14 (b.6) shows the transient response during load step changes in the AC common bus. At the beginning, the parallel VCIs operate with same power rates. At 1.3 s, an extra 460 Ω resistive load is connected to the common bus. The direct currents output of VCI #1 and VCI #2 both increase by 0.31 A immediately to supply the needed current with conventional droop control and the proposed controller as shown in Figs. 14 (b.1) and 14 (b.2). The quadrature currents output of VCI #1 and VCI #2 with the conventional droop control deviate by approximately 0.03 A because of the coupling between direct and quadrature currents as shown in Figs. 14 (b.3). However, by using the proposed method the quadrature currents output of VCI #1 and VCI #2 can maintain their original values, being barely affected by the direct output current disturbances as shown in Figs. 14 (b.4). The frequency response to load disturbances for both VCI units is depicted in Figs. 14 (b.5) and 14 (b.6).

The transient response for sudden direct currents sharing ratio changes between the parallel VCIs is illustrated in Figs. 14 (c.1) to 14 (c.6). At the beginning, the VCI units parallel operate with a common *RL* load. Both the VCI #1 and VCI #2 feeds are approximately 0.58 A of direct current and 0.2 A of quadrature current. At 2.3 s, the direct current sharing ratio between the parallel VCIs with the conventional droop control has been suddenly changed from 1:1 to 1:2 and then changed back to 1:1 at 10.6 s. As it can be seen in Fig. 14 (c.1), after about maximum 6 s, the output currents of the parallel VCIs are changed according to the new sharing ratio. Meanwhile, the quadrature current sharing has been affected by the changes on direct current sharing ratio as shown in Fig. 14 (c.3). By contrast, the direct current sharing ratio between the parallel VCIs with the proposed control approach has also been suddenly changed from 1:1 to 1:2 at 1.6 s and then changed back to 1:1 at 3.5 s. Fig. 14 (c.2) shows that the direct current outputs of VCIs increase immediately according to the sharing ratio changes and the transient response only lasts 0.2 s. Meanwhile, the quadrature current sharing ratio is kept constant via the decoupling control of the proposed controller.

### *B. Comparison experiment with resistive-inductive line impedance*

Fig. 15 shows the experimental results in order to compare the conventional droop control and the proposed control, with resistive-inductive line impedance which is equal to 1 Ω plus 1.7 mH in three different scenarios. Similarly Figs. 15 (a.1) to 15 (a.6) show the transient response of direct currents, quadrature currents and frequency when the VCI #2 is connected to VCI #1 with the conventional droop controller and the proposed controller separately. Figs. 15 (b.1) to 15 (b.6) illustrate the transient response for load step-up changes on AC common bus. Figs. 15 (c.1) to 15 (c.6) present the transient response during sudden direct currents sharing ratio changes between the parallel VCIs. Both the conventional droop control and the proposed controller can achieve stable operation. By contrast, the proposed approach can endow the system with faster response speed, smaller overshoot and decoupling control. Oscillation appears in the output current and system frequency with the conventional droop control due to the resistive-inductive line impedance and the coupling between $I_{od}$ and $I_{oq}$.

When having almost zero line impedance, or highly resistive, the parallel VCIs cannot operate by using the conventional droop control. In contrast, excellent performance can be obtained by using the proposed control as shown below.

For the rest of the tests, three parallel inverters have been considered to test the performances of the proposed controller with zero line impedance in the following scenarios.

### *C. Hot-swap operation (zero line impedance)*

A three-parallel VCIs system sharing a linear load ($R_{load1}$=57+j2.83 Ω) tests have been done to test individually the effects of DG units connecting and disconnecting. The transient response of the instantaneous currents, direct and quadrature output currents and frequency with the proposed control are illustrated in Fig. 16 (a), (b) and (c), respectively. As it can be observed, at the beginning, the three VCI units are on parallel operation with same power rates. At $t_2$ and $t_3$, VCI #2 and VCI #3 are disconnected from VCI #1 separately, whereas VCI #1 is responsible for supplying the total current. Fig. 16 indicates that the output currents of VCI #2 and VCI #3 decrease to zero, meanwhile, the output currents of VCI #1 is increased to 7.5 A immediately. After the synchronization process, VCI #2 and VCI #3 are re-connected to VCI #1 at $t_4$ and $t_5$ respectively. The transient performance is smooth and fast that the slowest settling time is about 0.8s. Furthermore, the current oscillations are well damped.

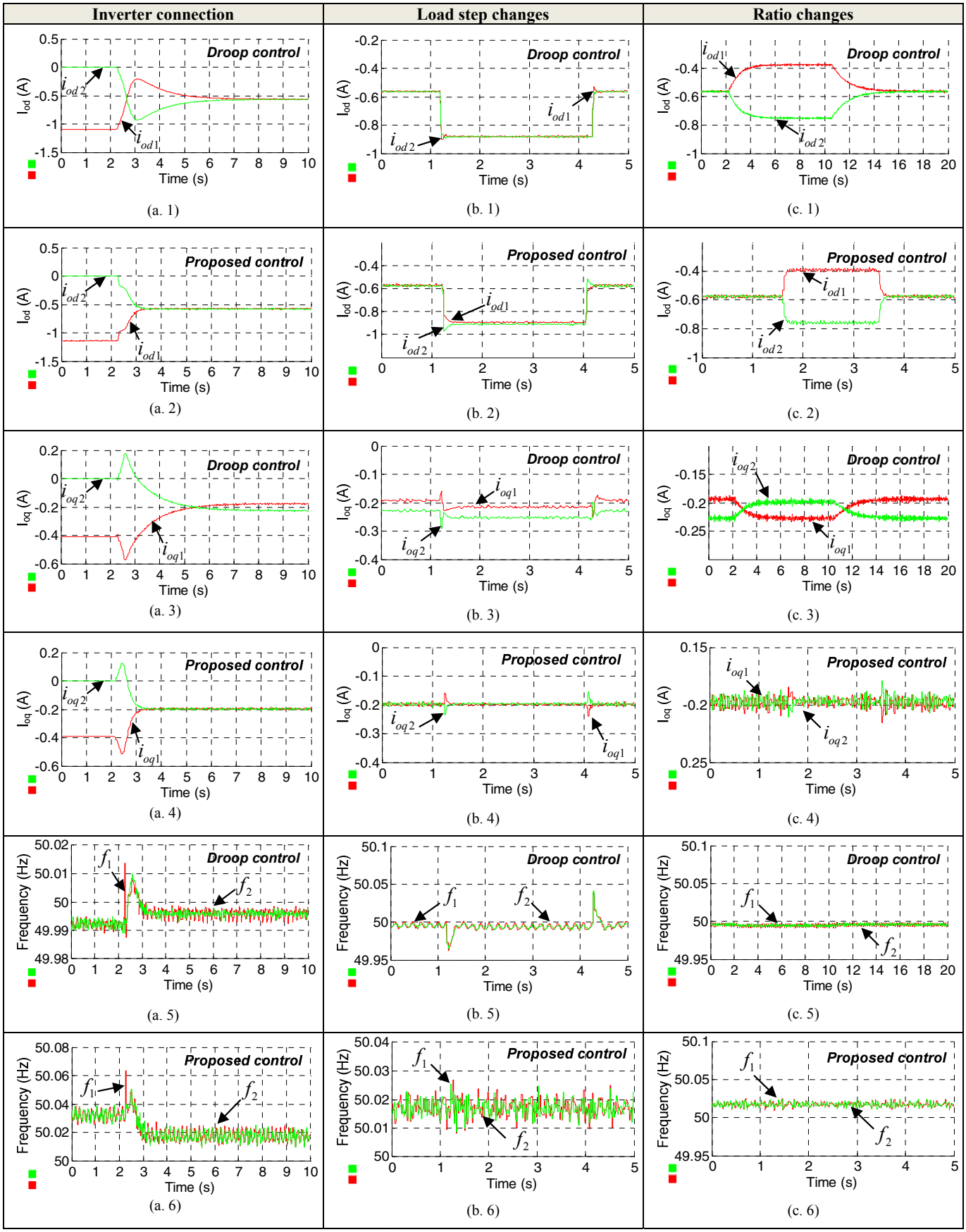



Fig. 14. Comparison experimental results with purely inductive line impedance in different scenarios.

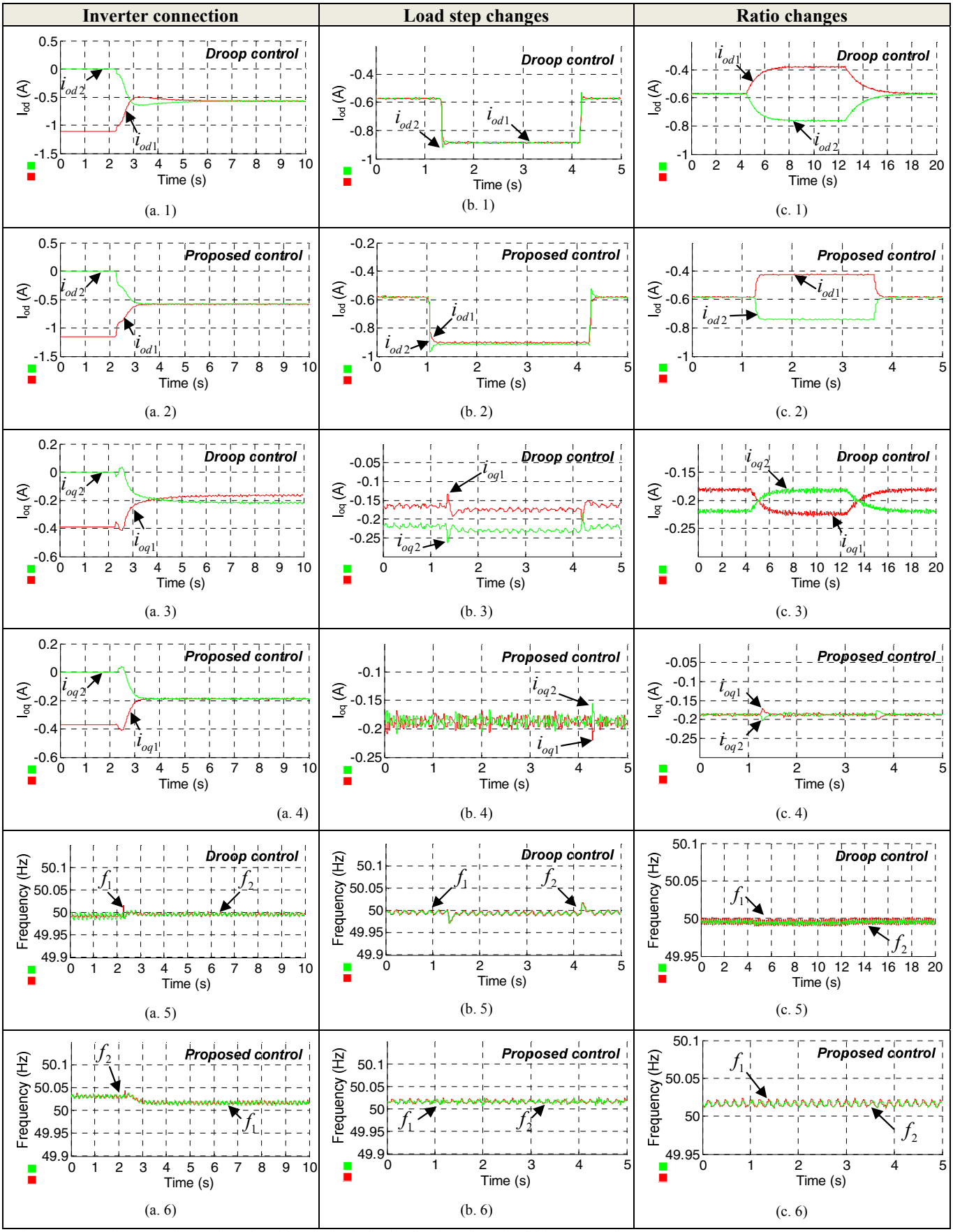
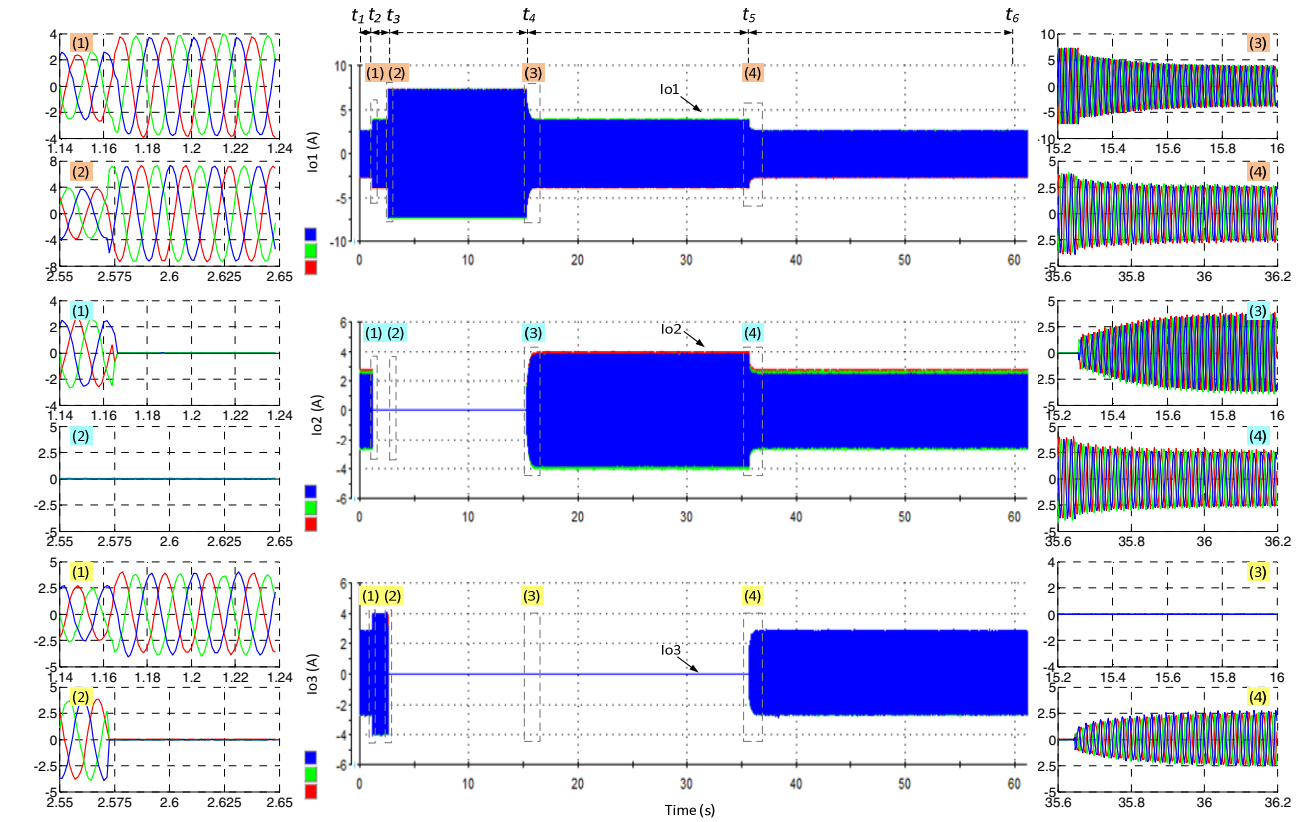
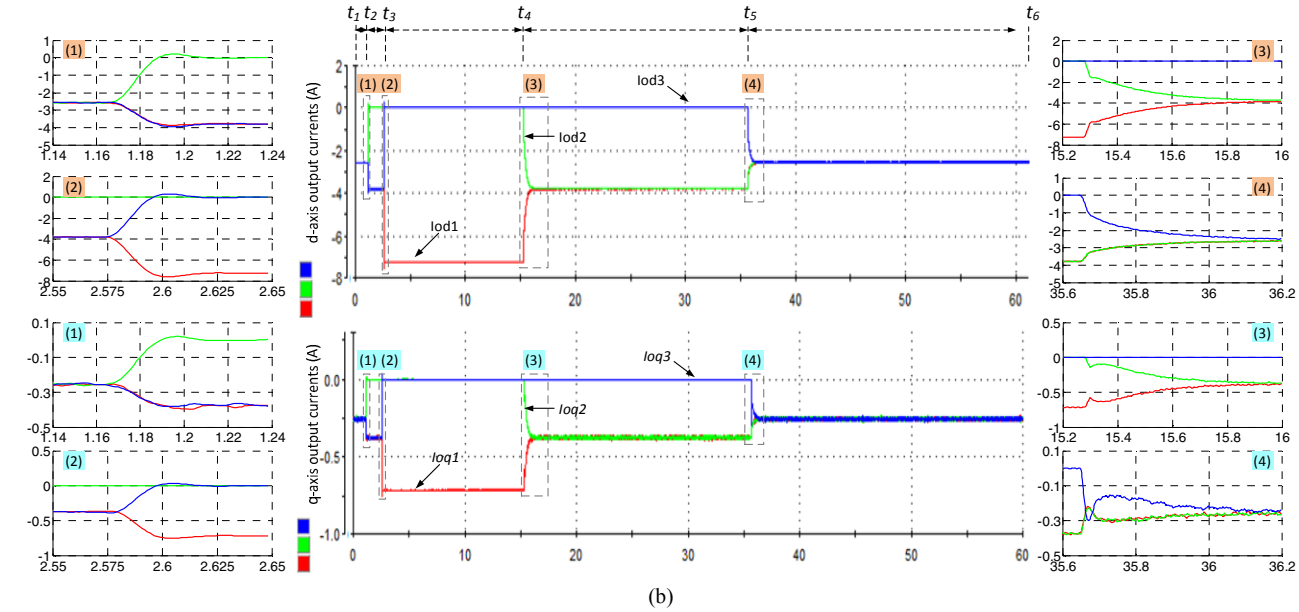


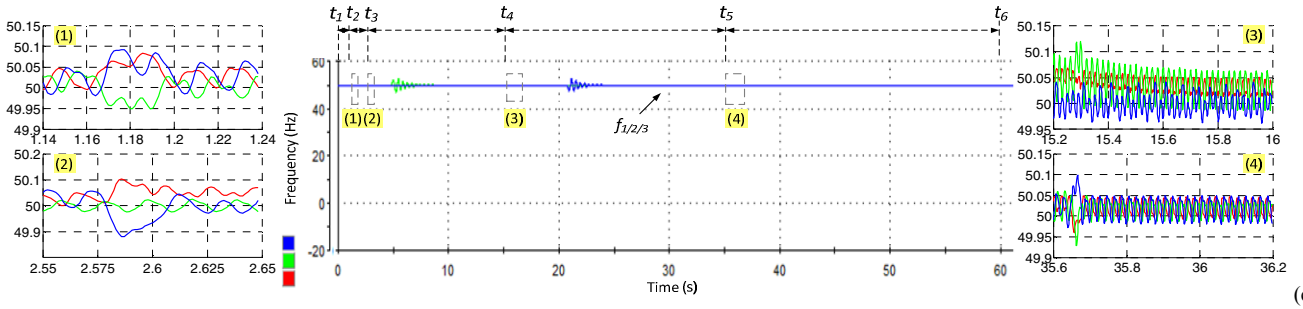

Fig. 15. Comparison experimental results with resistive-inductive line impedance in different scenarios.




(a)




(b)




(c)

Fig. 16. Transient responses of DG1, DG2, and DG3 in connection and disconnection scenario with the proposed controller. (a) Instantaneous output currents of DG1-3, (b) Direct and quadrature output currents of DG1-3, (c) Frequency of DG1-3.

### *D. Direct and quadrature currents decoupling sharing with different sharing ratio (zero line impedance)*

In some cases, the parallel connected VCIs need to supply active and reactive currents with different rates based on different power rates, requirements from EMS or other superior control loops. A three- parallel VCIs setup sharing a common distributed linear load ($R_{load1}$=57+j2.83 Ω) has been built to test the decoupling sharing performance of direct and quadrature currents with different sharing ratios. As shown in Fig. 17, the experiment can be divided nine stages. The different stages (S1 to S9) are described as follows:

S1 ($t_1$-$t_2$): The three VCIs are on parallel operation to share the common load equally due to the same virtual resistances

S2 ($t_2$-$t_3$): The *d*-axis virtual resistance ($R_{vird}$) ratio of these three paralleled VCIs is suddenly changed from 1:1:1 to 1.25:1:1 at $t_2$. Thus, the direct current output of VCI #1 is decreased immediately, whereas the direct currents output of VCI #2 and VCI #3 are all increased by the same value within 0.1s. The change on active current does not influence on the quadrature currents of these three VCIs as the theoretical analysis.

S3 ($t_3$-$t_4$): The $R_{vird}$ ratio is suddenly changed from 1.25:1:1 to 1.25:1.5:1 at $t_3$. As observed, the output direct current of VCI #2 is decreased to the desired value.

S4 ($t_4$-$t_5$): At $t_4$, the paralleled system is subjected to a 50% step up in the *q*-axis virtual resistance ($R_{virq}$) of VCI #2. Thus, the $R_{virq}$ ratio of these three VCIs is suddenly changed from 1:1:1 to 1:1.5:1. As observed, the output quadrature current ratio becomes 1.5:1:1.5 which is the inverse proportion of the virtual resistance ratio as the theoretical analysis. In addition, the change on reactive current also does not affect the direct currents.

S5 ($t_5$-$t_6$): The $R_{virq}$ ratio suddenly changes from 1:1.5:1 to 1:1.5:1.75 at $t_5$.

S6 ($t_6$-$t_7$): At $t_6$, the $R_{vird}$ of VCI #1 reduces back to 2 Ω. Thus the output direct current sharing ratio becomes 1.5:1:1.5.

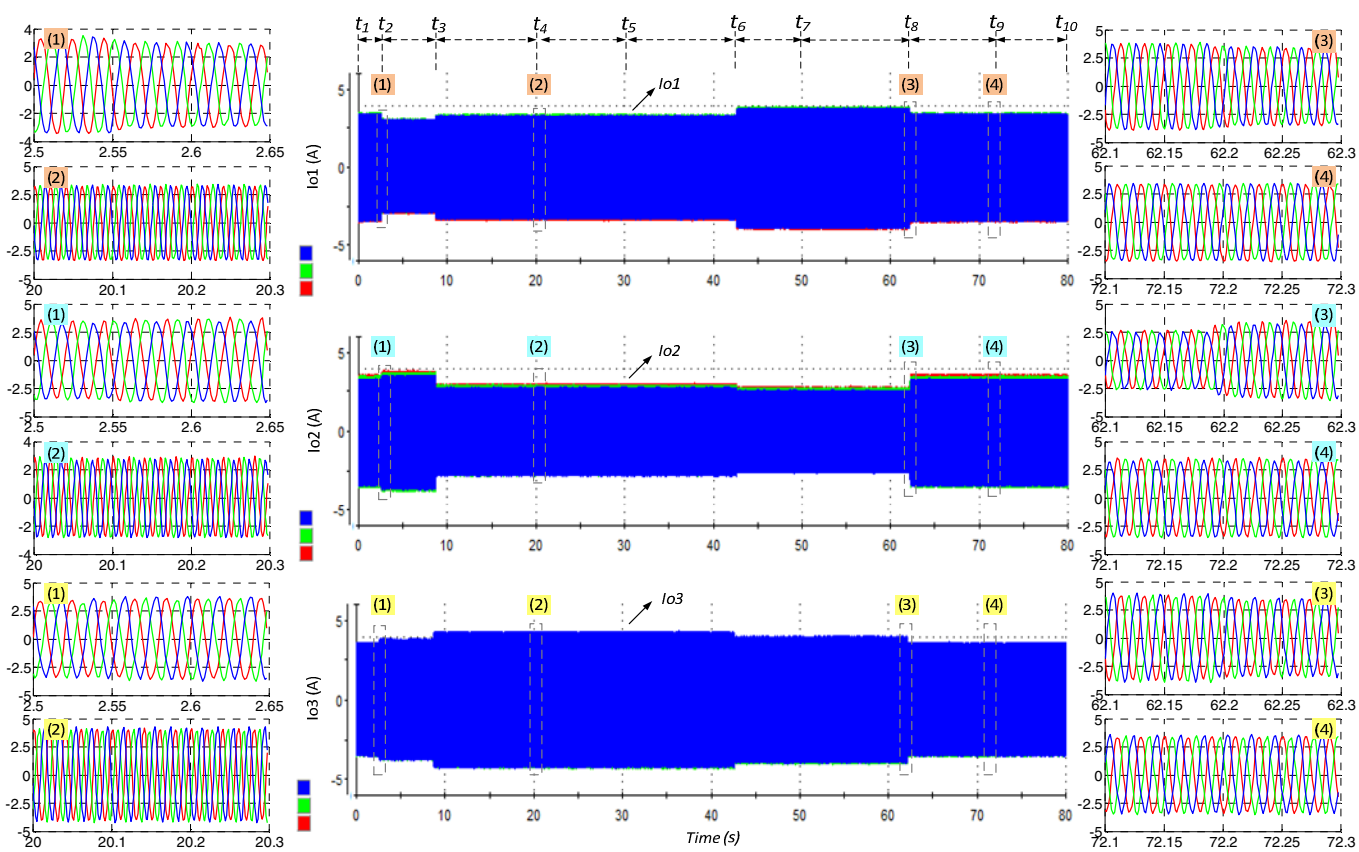
S7 ($t_7$-$t_8$): At $t_7$, the $R_{virq}$ of VCI #2 reduces back to 2 Ω. Hence the direct current sharing ratio becomes 1.75: 1.75:1.

S8 ($t_8$-$t_9$): The $R_{vird}$ ratio changes from 1:1.5:1 to 1:1:1 at $t_8$.

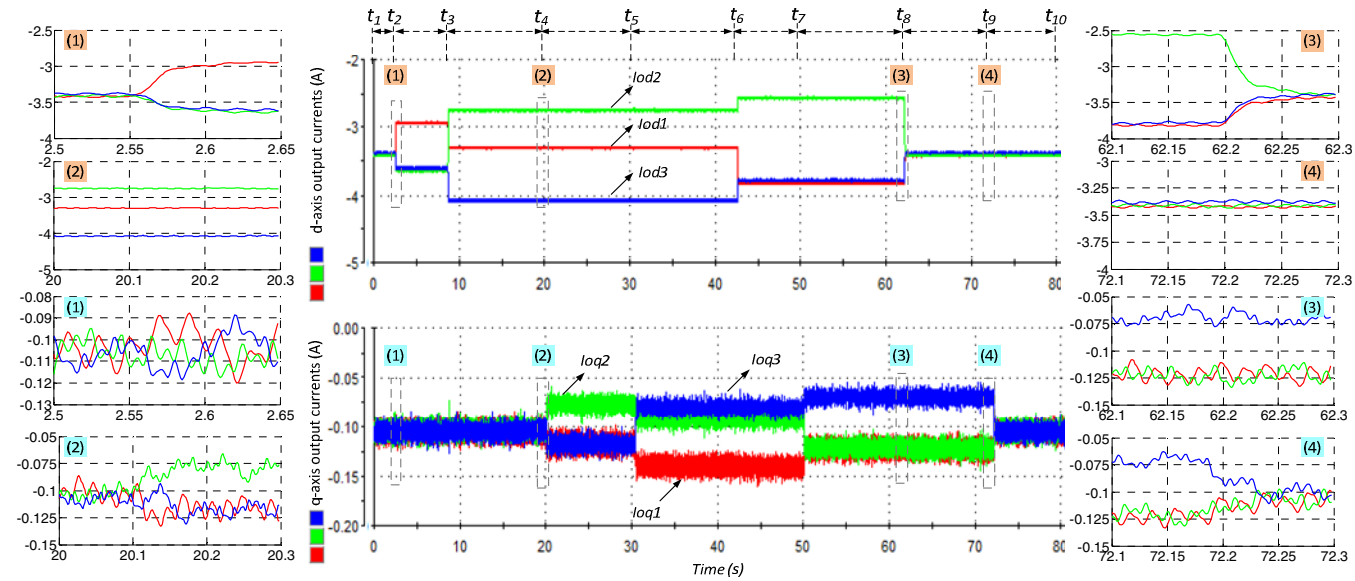
S9 ($t_9$-$t_{10}$): The $R_{virq}$ ratio changes from 1:1:1.75 to 1:1:1 at $t_9$. Therefore, the output direct and quadrature currents of three VCIs are equal again.

The proposed controller successfully regulates the output currents of paralleled VCIs to the desired value. As can be observed, even with different power rates, the VCI units with the proposed control strategy will still maintain stable operation and achieve the online sharing ratio change. The proposed controller presents large stability margin to the control variables $R_{vird}$ and $R_{virq}$.

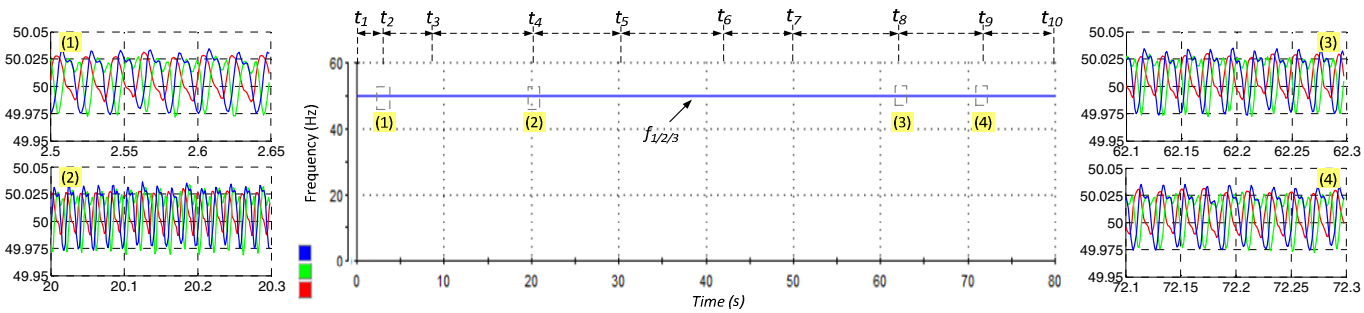
In summary, the experimental results reveal that the proposed control strategy does apply to low-voltage parallel-VCI-based system where the line impedance usually presents high ratio of *R/X* and short length because of its faster response speed, online sharing ratio change function, larger stability margin, smaller overshoot, plug'n'play operation and decoupling control. In addition, the proposed control strategy also works well with inductive-resistive line impedance and small purely inductive line impedance by means of virtual




(a)




(b)




(c)

Fig. 17. Transient responses of DG1, DG2, and DG3 with different sharing ratio. (a) Instantaneous output currents of DG1-3, (b) Direct and quadrature output currents of DG1-3, (c) Frequency of DG1-3

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resistor. The proposed $I_{od}-V_o$ and $I_{oq}-\omega$ droop characteristics will present non-linear when the line impedance over the limitations. Thus, the droop control strategy should be applied to the high inductive system. In other cases, the proposed control strategy can provide superior performances. The prominent features of the proposed strategy compared with the conventional droop control are summarized in Table II.

## VII. Conclusion and Future Work

A simpler and faster controller that comprises a PLL, a virtual resistance loop and a PR controller in inner voltage loop for controlling direct and quadrature load currents separately among parallel three-phase inverters is developed. Based on the steady state characteristic analysis, by adjusting the *d*-axis virtual resistance ratio between the parallel inverters, the direct load current sharing can be achieved. Whereas by modifying the *q*-axis virtual resistance ratio between parallel inverters, the quadrature load current provided will be changed proportionally. The proposed control strategy does apply to low-voltage microgrids and islanded minigrids. In addition, it can also works well with inductive-resistive line impedance and even small purely inductive or resistive line impedance thanks to the use of virtual resistance. Compared with conventional droop control, the described method does not need to calculate active and reactive powers. Thus, the method exhibits faster transient response and better precision. Experimental results are included to show the excellent behaviour of the proposed controller. The small signal model and stability analysis will be presented in Part II of this paper.

## Appendix

The detailed derivative process of (10) in Section IV is shown as follows.

As indicated in Fig. 5, the closed loop includes three-leg three-phase inverter, $L_f$-$C_f$ filter, line impedance, inner voltage and current control, and virtual resistance loop.

The block diagram of the inner current and voltage loops as well as the *LC* filter is shown in Fig. A.1.

Based on the diagram, the closed-loop transfer function can be written as follows:

$$v_o(s) = G(s)v'_{ref}(s) - Z_o(s)i_o(s) \tag{A.1}$$

being

$$G(s) = \frac{G_v(s)G_i(s)K_{PWM}}{L_fC_fs^2 + (rC_f + G_i(s)K_{PWM}C_f)s + 1 + G_v(s)G_i(s)K_{PWM}} \tag{A.2}$$

TABLE II
PERFORMANCE COMPARISON

| | Purely inductive line impedance | | Resistive-inductive line impedance | | Zero or resistive line impedance | |
|---|---|---|---|---|---|---|
| | ***P-V/Q-f* droop** | **Proposed control** | ***P-V/Q-f* droop** | **Proposed control** | ***P-V/Q-f* droop** | **Proposed control** |
| Control capability | Yes | Yes, but cannot work with large inductive line impedance | Yes | Yes | No, need change to *P-f/Q-V* droop | Yes |
| Transient response | Slow | fast | Slow | fast | Slow | fast |
| Control performance | Good | Good, but cannot work with large inductive line impedance | Oscillations | Good | Good (if with *P-f/Q-V* droop) | Very well |
| Robustness | Poor | Good | Poor | Good | Poor | Good |
| Control parameters | $m$, $n$, $Z_{vir}$ | $R_{vird}$, $R_{virq}$ | $m$, $n$, $Z_{vir}$ | $R_{vird}$, $R_{virq}$ | $m$, $n$, $Z_{vir}$ | $R_{vird}$, $R_{virq}$ |

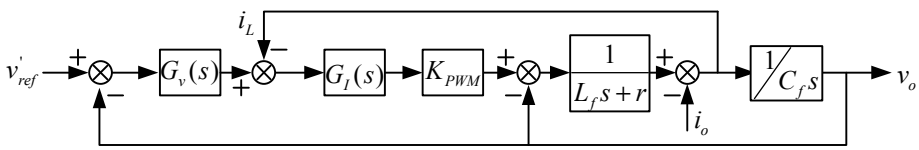


Fig. A.1 Block diagram of the dual-loop control

$$Z_o(s) = \frac{sL_f + r}{L_f C_f s^2 + (rC_f + G_i(s)K_{PWM}C_f)s + 1 + G_v(s)G_i(s)K_{PWM}} \tag{A.3}$$

$$G_v(s) = K_{pv} + \frac{K_{iv}s}{s^2 + \omega_c^2} \tag{A.4}$$

$$G_i(s) = K_{pi} \tag{A.5}$$

where *G(s)* presents the tracking performance of the output voltage following the voltage reference, $Z_o(s)$ is the equivalent output impedance of the inverter, $v_o(s)$ is the output voltage, $v'_{ref}(s)$ is the reference voltage of inner voltage loop, $i_o(s)$ is the output current, $G_v(s)$ is the PR voltage control loop, $G_i(s)$ is the proportional current control loop, $K_{PWM}$ is the gain of three phase inverter, $L_f$, $C_f$ and *r* are the inductor, capacitor, and inductor ESR of the *LC* filter respectively, $K_{pv}$ and $K_{iv}$ are the proportional and integral coefficients of voltage control loop, $\omega_c$ is the resonant frequency of the PR regulator in voltage control loop, and $K_{pi}$ is the proportional coefficients of current control loop.

To obtain the direct and quadrature load currents, the equivalent parallel connected resistive-inductive load can be represented as follows:

$$G_{Lequ}(s) = \frac{1}{R_{Lequ}} + \frac{1}{sL_{Lequ}} \tag{A.6}$$

where $G_{Lequ}(s)$ is the equivalent load admittance, $R_{Lequ}$ is the equivalent resistor, and $L_{Lequ}$ is the equivalent inductance.

The line impedance can be expressed as follows:

$$Z_{line}(s) = R_{line} + sL_{line} \tag{A.7}$$

where $Z_{line}(s)$ is the line impedance, $R_{line}$ is the line resistor, and $L_{line}$ is the line inductance.

Hence, the closed loop transfer function $T_{plant}(s)$ can be derived based on Fig. 5.

$$T_{plant}(s) = \frac{v_o(s)}{v_{ref}(s)} = \frac{G(s)\left[1 + G_{Lequ}(s)Z_{line}(s)\right]}{1 + G_{Lequ}(s)Z_{line}(s) + G_{vir}(s)G(s) + G_{Lequ}(s)Z_o(s)} \tag{A.8}$$

being $G_{vir}(s) = \frac{R_{vird}}{R_{Lequ}} + \frac{R_{virq}}{sL_{Lequ}}$

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