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Analysis of Phase-Locked Loop Influence on the Stability of Single-phase Grid-Connected Inverter

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***Abstract*-- A controlled power inverter can cause instability at the point of common coupling (PCC) with its output filter and the grid. This paper analyzes the influence of the Phase-Locked Loop (PLL) on the output admittance of single-phase current-controlled inverters with different grid stiffness. It shows that the PLL introduces a paralleled admittance into the output admittance of the inverter, which may lead to unintentional low-order harmonic oscillation in a weak grid. Moreover, the Second Order Generalized Integrator PLL (SOGI-PLL) is also modeled. It is found that the quadrature signal generator of SOGI plays a stabilizing role in grid-inverter interactions, which thus provides a promising candidate for avoiding the PLL-induced instability in single-phase inverters. Simulation results are presented for verifying the theoretical analysis. The possible instability due to different PLL bandwidth is also demonstrated.**

***Index Terms*--Phase-Locked Loop (PLL), small-signal model, single-phase inverter, stability.**

I. INTRODUCTION

Most renewable energy sources have to be converted from dc to ac in grid-connected applications. The phase angle and frequency of the injected current have to be synchronized with the grid voltage in order to flexibly control the active power and reactive power injected into the power grid. This has typically been accomplished by using a Phase-Locked Loop (PLL) [1].

It has been reported the power quality of grid tends to be degraded as the increased penetration level of inverter-interfaced renewable energy sources. For example, it is shown in [1] that even though some commercial photovoltaic inverters fulfilled the requirements imposed by the grid standards, their output currents still exceed the harmonic limits in weak grids with high grid inductance.

In these cases, harmonic emissions of inverters are likely induced by the interaction between the inverter control system, e.g. PLL and current control, and grid impedance [2]. A well-established technique to analyze such interconnected systems is the impedance-based stability analysis with Nyquist stability criterion [6], [10], which predicts the system stability based on the ratio between the grid impedance and inverter output admittance. This method has widely been used to study the stability of a hybrid ac/dc system [7], and the stability of grid-connected and islanded micro-grids [8]. It is shown in [3] that the harmonic content in the injected current increased in the case of using a wide-bandwidth PLL in a weak grid, which may further lead to instability when grid impedance changes, as shown in [5]. It is demonstrated in [4] that how this instability can be avoided by actively shaping the output admittance of inverter. However, the previous research works focused on the stability influence of conventional Synchronous Reference Frame-PLL (SRF-PLL), while the dynamic of the Quadrature Signal Generator (QSG) used in single-phase systems is overlooked, which is a critical component for grid-synchronization of single-phase grid-connected inverters.

This paper thus addresses the influence of PLL on the stability of a single-phase grid-connected, LCL-filtered inverter with a stationary frame current control, and a particular attention is given to the effect of Second-Order Generalized Integrator (SOGI) in using SOGI-PLL. First, the impedance models of the single-phase inverter with the basic T/4 delayed PLL and SOGI-PLL are developed. Then, the influence of these PLLs on the stability of inverter is analyzed by means of impedance-based stability analysis method. It is shown in stiff grids the inverter is stable when the PLL itself and current control loop are stable. In contrast, the system stability in a weak grid is not only affected by the stability of PLL itself and current control, but affected also by the PLL bandwidth through the current reference generation, which may introduce a negative real-part in the output admittance of inverter. Moreover, with the use of SOGI and its low-pass filtering nature of generating quadrature signal, the inverter can still be stabilized even with a wide-bandwidth SRF-PLL design. It thus provides a promising grid synchronization technique for avoiding the PLL-induced instability.

The rest of the paper is organized as follows: Section II presents a small-signal model of the single-phase grid-connected inverter with PLL. Section III shows how the bandwidth of PLL influences on the stability of the inverter under a weak grid, and the resulting resonance frequency is predicted by means of the impedance-based stability analysis. Simulation results are presented in Section IV, which validates the effectiveness of theoretical analysis. Section V concludes the paper.

II. Impedance-based Model of Inverter with PLL

A. Inverter Model

Fig. 1 shows a diagram of a single-phase grid-connected inverter with an *LCL*-filter, where L_1, C_f and L_2 constitute the *LCL*-filter; Z_g is the grid impedance; U_{in} is the input dc voltage; u_{inv} is the output voltage of the inverter bridge; u_g is the grid voltage; u_{PCC} is the voltage of PCC point. The reference current i_{ref} is obtained by using a phase-locked loop which will be synchronized with the power grid voltage. $G_i(s)$ is the grid current controller transfer function which adopts the proportional resonant (PR) controller. In order to accurately reflect the characteristics of the digital control, the zero order hold (ZOH) is adopted in the model and its transfer function is $G_h(s)=1-e^{-sT_s}/s\approx T_s e^{-0.5sT_s}$.

According to Fig. 1, a small signal model of the grid-connected inverter in s-domain can be obtained as shown in Fig. 2. Here $1/T_s$ is the sampling time, K_{PWM} is the transfer function from modulation wave to u_{inv}, $G_{PLL}(s)$ is the phase locked loop transfer function. As shown in Fig. 2, the inverter model can be divided into two parts: the first part is the phase-locked control loop, which is from the grid reference current i_{ref} to the voltage of PCC u_{PCC} through phase-locked loop; the other part is the grid current control loop, which is from the grid current i_g to the grid reference current i_{ref} through the grid current closed loop.

The control model of Fig. 2 can be simplified to Fig. 3,

$$G_{X1}=\frac{K_{PWM}G_iG_ZZ_C}{Z_{L1}+Z_C} \tag{1}$$

$$G_{X2}=\frac{Z_{L1}+Z_C}{Z_{L1}Z_{L2}+Z_{L1}Z_C+Z_{L2}Z_C} \tag{2}$$

$$G_Z=e^{-sTs}\bullet G_h(s)\approx 1/(1.5T_s s+1) \tag{3}$$

where, $Z_{L1}=sL_1, Z_{L2}=sL_2, Z_C=1/sC_f, G_i(s)=K_{pcon}+\frac{K_{rcon}s}{s^2+\omega^2}$.

From Fig. 3 the grid current i_g can be obtained as

$$i_g=\frac{T_{ig}}{1+T_{ig}}i_{ref}-\frac{G_{X2}}{1+T_{ig}}u_{PCC} \tag{4}$$

where $T_{ig}=G_{X1}G_{X2}$ is the gain of the current control loop. However, the reference current i_{ref} is not an independent variable, when considering the PLL. The grid current i_g can be rewritten as

$$i_g=\frac{T_{ig}}{1+T_{ig}}I_mG_{PLL}u_{PCC}-\frac{G_{X2}}{1+T_{ig}}u_{PCC} \tag{5}$$

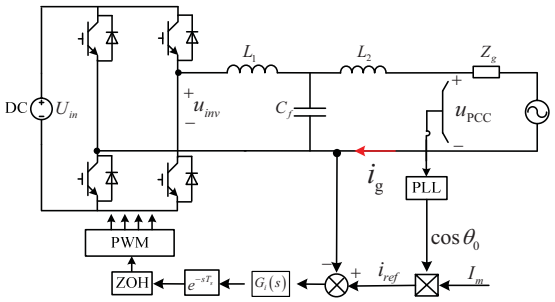

Fig. 1. Basic diagram of a single-phase inverter with LCL-filter.

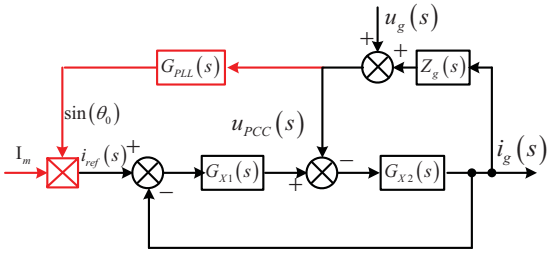

Fig. 3. Simplified block diagram of inverter in the s-domain.

B. The Small Signal Model of T/4 Delayed PLL

In order to analyze the influence of the PLL on the stability of the grid-connected inverter, the mathematic model of the PLL should be established at first. This paper analyzes the influence of the PLL on the system stability by adopting the *T/4* delayed PLL as the synchronous method for simple, and the analysis method can be extended into other PLLs. The block diagram of *T/4* delayed PLL is shown in Fig. 4.

From Fig.4, the small-signal model of the inverter can be derived as (6) in the time-domain. In terms of notation, bold fonts are used to represent vector and matrix quantities. Where ω_0 is the fundamental angular frequency, θ_0 is the corresponding angle, i_{ref} is the reference grid current, I_m is the amplitude of the reference current.

$$\begin{cases}\boldsymbol{\mu}_{\alpha\beta}=T_{\alpha\beta/dq}\boldsymbol{\mu}_{dq}=e^{j\omega_0 t}\boldsymbol{\mu}_{dq}\triangleq\mu_\alpha+j\mu_\beta\\ \omega_0=\left(K_p+\int K_i\right)\mu_q\\ \theta_0=\int\omega_0 dt\\ i_{ref}=I_m\cos(\theta_0)\end{cases} \tag{6}$$

Since the PLL is a nonlinear system, linearization must be made to allow transfer function to be derived. For this sake, Equation (6) can be rewritten by the sum of the steady state variable and disturbance variable as

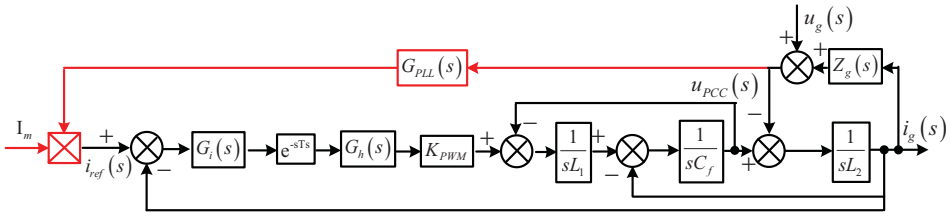

Fig. 2. Block diagram of grid-connected inverter in s-domain.

$$\begin{cases} \boldsymbol{\mu}_{dq} = \boldsymbol{U}_{dq} + \hat{\boldsymbol{\mu}}_{dq} \\ \theta = \theta_0 + \hat{\theta}_0 = \omega_0 t + \hat{\theta}_0 \\ i_{ref} = I_{ref} + \hat{i}_{ref} \end{cases} \tag{7}$$

where, ω_0 is the fundamental angular frequency, $\hat{\theta}_0$ is the disturbance angular, $\boldsymbol{U}_{dq}$ and $\hat{\boldsymbol{\mu}}_{dq}$ are the synchronous frame voltage and disturbance variable of the PCC, respectively. After the Park transformation, the voltage of PCC in stationary frame can be obtained as

$$\boldsymbol{\mu}_{\alpha\beta} = \boldsymbol{U}_{\alpha\beta} + \hat{\boldsymbol{\mu}}_{\alpha\beta} = e^{j\omega_0 t + \hat{\theta}_0} \boldsymbol{\mu}_{dq} \tag{8}$$

The relation can be linearized by approximating $\cos\hat{\theta}_0 \approx 1$, $\sin\hat{\theta}_0 \approx \hat{\theta}_0$ and by neglecting cross terms between the perturbation quantities, yields:

$$\boldsymbol{\mu}_{dq} = U_m + \hat{\boldsymbol{\mu}}_{dq} - jU_m\hat{\theta}_0 \tag{9}$$

The relation between the disturbance voltage of PCC in stationary frame $\hat{\boldsymbol{\mu}}_{\alpha\beta}$ and the disturbance voltage of PCC in synchronous frame $\hat{\boldsymbol{\mu}}_{dq}$ can be derived as

$$\hat{\boldsymbol{\mu}}_{\alpha\beta} \approx e^{j\omega_0 t}\left[jU_m\hat{\theta}_0 + \hat{\boldsymbol{\mu}}_{dq} \right] \tag{10}$$

Then, substitute (7) and (9) to (6), and after the Laplace transformation, the result can be obtained as

$$\hat{\theta}_0(s) = T_{PLL}(s)\,\mathrm{Im}\left\{\hat{\boldsymbol{\mu}}_{dq}\right\} \tag{11}$$

where $T_{PLL}(s) = \dfrac{K_p s + K_i}{s^2 + U_m\left(K_p s + K_i\right)}$.

For the stationary frame current control, the reference current can be obtained as

$$i_{ref} = I_{ref} + \hat{i}_{ref} = I_m\cos(\omega_0 t) + I_m\sin(\omega_0 t)\hat{\theta}_0 \tag{12}$$

where

$$\hat{i}_{ref} = I_m\sin(\omega_0 t)\hat{\theta}_0 \tag{13}$$

Then, equation (13) can be transformed to s-domain by the Laplace transformation as

$$\hat{i}_{ref}(s) = \frac{-I_m}{2j}\left[\hat{\theta}(s - j\omega) - \hat{\theta}(s + j\omega)\right] \tag{14}$$

Neglecting the PD dynamic characteristics of the PLL, i.e. $\hat{u}_{PCC} = \hat{u}_\alpha$, and considering $\hat{\mu}_\beta$ lagging $\hat{\mu}_\alpha$ 90°, Substitution of (10-11) in (13), the transfer function from the reference current to the voltage of the PCC and PLL transfer function can be obtained as (15) and (16).

$$\frac{\hat{i}_{ref}(s)}{\hat{\mu}_{\mathrm{PCC}}(s)} = \frac{I_m}{2}\frac{K_p(s - j\omega_0) + K_i}{(s - j\omega_0)^2 + U_m\left[K_p(s - j\omega_0) + K_i\right]} \tag{15}$$

$$G_{PLL}(s) = \frac{1}{2}T_{PLL}(s - j\omega_0) \tag{16}$$

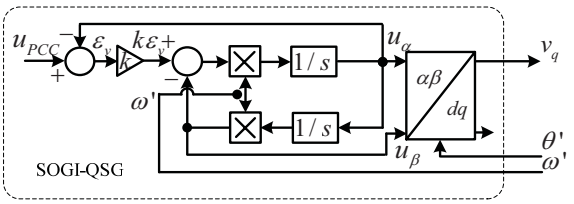

Fig. 5. Phase Detector of SOGI-PLL

C. The Small Signal Model of SOGI-PLL

As discussed in the previous part, the transfer function of PLL from the reference current to the voltage of the PCC to can be obtained by neglecting the PD block dynamics, however, in the practice, there always exists a PD in the advanced PLL, i.e. Enhanced PLL, SOGI-PLL and Inverse Park transformation PLL [13], which are common used in the single-phase inverter, because the information of the single-phase system is less than three-phase system. The characteristics of the QSG has not discussed in the published papers that concerned the PLL influence on the impedance of the inverter. In this part, the dynamics of the QSG in an advanced PLL (SOGI-PLL) will be considered when modeled the admittance of the inverter with PLL.

An adaptive filtering based PLL solution is using second order generalized integrator (SOGI) to create the QSG system, commonly known as SOGI-PLL [13]. The structure of SOGI-QSG is depicted in Fig. 5, in which ω' is the estimated frequency of the input signal, the proportionality factor k is the control parameter of the adaptive filter.

If two-weight adaptive filters are adopted in single-phase applications, it will present a better performance and it behaves like a "sinusoidal integrator" [13-15]. The transfer function of such kind of adaptive filter can be expressed as,

$$G_{AF} = \frac{s}{s^2 + \omega'^2} \tag{17}$$

Multiplied by ω', it shares the transfer function of a second order generalized integrator in common [14], [15].

Thus, referring to Fig. 5, the characteristic transfer functions of the SOGI block can be derived as

$$\begin{cases} D(\mathrm{s}) = \dfrac{u_\alpha}{u_{PCC}}(\mathrm{s}) = \dfrac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \\ Q(\mathrm{s}) = \dfrac{u_\beta}{u_{PCC}}(\mathrm{s}) = \dfrac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \end{cases} \tag{18}$$

When considering the QSG dynamics, equation (15) cannot be used for the transfer function of PLL from the

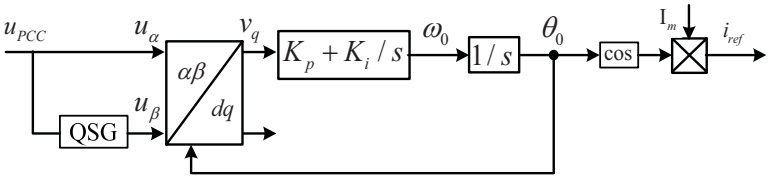

Fig. 4. Block diagram of synchronous reference frame PLL.

reference current to the voltage of the PCC. It will be only the transfer function of PLL from the reference current $\hat{i}_{ref}(s)$ to one of the outputs of QSG $\hat{u}_\alpha$. However, the other output of the QSG $\hat{u}_\beta$ in the SOGI-PLL also has the effect on the characteristics of the PLL. As shown in equation (18), *D(s)* is a band-pass filter and *Q(s)* is a low-pass filter, when analyze the influence of PLL on the admittance of the inverter, both of the two characteristics has to be considered.

From equation (10), the disturbance of the QSG output can be obtained as (19) and (20), separately.

$$\begin{aligned}\hat{\mu}_\alpha \approx & -U_m \sin(\theta_0)\hat{\theta}_0 - \mathrm{Im}\{\hat{\boldsymbol{\mu}}_{dq}\}\sin(\theta_0) \\ & + \mathrm{Re}\{\hat{\boldsymbol{\mu}}_{dq}\}\cos(\theta_0)\end{aligned} \tag{19}$$

$$\begin{aligned}\hat{\mu}_\beta \approx & U_m \cos(\theta_0)\hat{\theta}_0 + \mathrm{Im}\{\hat{\boldsymbol{\mu}}_{dq}\}\cos(\theta_0) \\ & - \mathrm{Re}\{\hat{\boldsymbol{\mu}}_{dq}\}\sin(\theta_0)\end{aligned} \tag{20}$$

For the disturbance $\mathrm{Re}\{\hat{\boldsymbol{\mu}}_{dq}\}$ in synchronization frame is not used in the PLL structure, so the third term in right side of equation (19) and (20) can be neglected. Equation (19) and (20) can be simplified transformed to s-domain by Laplace transformation as

$$\hat{\mu}_\alpha(s) = \frac{-1}{2j}\left[\frac{1}{T_{PLL}(s-j\omega)}\hat{\theta}(s-j\omega) - \frac{1}{T_{PLL}(s+j\omega)}\hat{\theta}(s+j\omega)\right] \tag{21}$$

$$\hat{\mu}_\beta(s) = \frac{1}{2}\left[\frac{1}{T_{PLL}(s-j\omega)}\hat{\theta}(s-j\omega) + \frac{1}{T_{PLL}(s+j\omega)}\hat{\theta}(s+j\omega)\right] \tag{22}$$

Substitute (21) and (22) in (14), the transfer function from the reference current to the output voltage of the SOGI-QSG can be obtained as (23).

$$\begin{aligned}\hat{i}_{ref}(s) = & \frac{I_m}{2}\left[T_{PLL}(s-j\omega) + T_{PLL}(s+j\omega)\right]\hat{\mu}_\alpha(s) \\ & + j\frac{I_m}{2}\left[T_{PLL}(s-j\omega) - T_{PLL}(s+j\omega)\right]\hat{\mu}_\beta(s)\end{aligned} \tag{23}$$

Considering the dynamics of the SOGI-QSG, the transfer function from the reference current $\hat{i}_{ref}(s)$ to the voltage of PCC $\hat{\mu}_{\mathrm{PCC}}(s)$ and SOGI-PLL transfer function can be derived as (24) and (25).

$$\begin{aligned}\frac{\hat{i}_{ref}(s)}{\hat{u}_{PCC}(s)} = & \frac{I_m}{2}\left[T_{PLL}(s-j\omega) + T_{PLL}(s+j\omega)\right]D(s) \\ & + j\frac{I_m}{2}\left[T_{PLL}(s-j\omega) - T_{PLL}(s+j\omega)\right]Q(s)\end{aligned} \tag{24}$$

$$\begin{aligned}G_{SOGI-PLL}(s) = & \frac{1}{2}\left[T_{PLL}(s-j\omega) + T_{PLL}(s+j\omega)\right]D(s) \\ & + j\frac{1}{2}\left[T_{PLL}(s-j\omega) - T_{PLL}(s+j\omega)\right]Q(s)\end{aligned} \tag{25}$$

From equation (25), the current reference $\hat{i}_{ref}(s)$ is not only effected by $\hat{u}_\alpha$, but also influenced by the orthogonal signal $\hat{u}_\beta$, both of the two characteristics of *D(s)* and *Q(s)* influenced the admittance of the inverter by effected the transfer function of PLL.

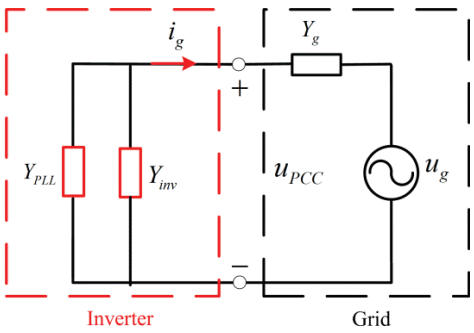

Fig. 6. Equivalent circuit of grid-connected inverter with PLL.

III. Impact to System Stability due to PLL Effects

The main focus in this section is to analyze how the amplitude of the reference current, the PLL bandwidth and SOGI-PLL effect on the stability of the single-phase inverter system. Impedance-based stability criterion will be derived to verify the accuracy of the inverter model with PLL has established in section II.

A. Impedance-Based Stability Analysis

A method to determine inverter-grid system stability only using the inverter output admittance and the grid impedance is developed in [9]. It has been shown that a grid-connected inverter will remain stable, if the ratio of the inverter output admittance to the grid admittance and satisfied the Nyquist stability criterion. But in [9] the inverter model does not consider the influence of the PLL on the stability of the inverter. The impedance-based stability criterion of considering the influence of the PLL on the inverter will be derived in this paper.

Equation (5) can be rewritten as

$$i_g = -\left(Y_{PLL}u_{PCC} + Y_{inv}u_{PCC}\right) \tag{26}$$

where, $Y_{PLL} = -\dfrac{I_m G_{PLL} T_{ig}}{1+T_{ig}}$, $Y_{inv} = \dfrac{G_{X2}}{1+T_{ig}}$, $G_{PLL}(s)$ can be replaced by $G_{SOGI-PLL}(s)$ if the synchronization method is SOGI-PLL.

From equation (26), the equivalent circuit of the grid-connected inverter is shown in Fig. 6. As shown in Fig. 6, considering the PLL, the grid inverter admittance can be equivalent to a model of the current loop admittance Y_{inv} in parallel with the negative admittance Y_{PLL}. The output admittance of the grid-inverter can be obtained as:

$$Y_o = -\frac{i_g}{u_{PCC}} = Y_{PLL} + Y_{inv} \tag{27}$$

According to Fig. 6, the following can be obtained,

$$\frac{i_g}{u_g} = -\frac{1}{1/Y_0 + 1/Y_g} = -Y_0\frac{1}{1+Y_o/Y_g} \tag{28}$$

where $Y_g = 1/L_g s$ is the output admittance of the grid, L_g is the grid inductance.

The following is to analyze how the grid admittance affected the stability criterion of the system when the grid is changed from a strong grid to a weak grid.

1) Strong grid.

As shown in the Fig. 6, Y_0 is equivalent to Y_{PLL} in parallel with Y_{inv}.

$$Y_0 = Y_{PLL} + Y_{inv} \tag{29}$$

From equation (29), the poles of Y_0 are the poles of Y_{PLL} add the poles of Y_{inv}, therefore, in order to guarantee Y_0 stable, Y_{PLL} and Y_{inv} must be stable.

Form (26) and (5), the admittance of the inverter can be obtained as $Y_{inv} = 1/Z_{inv} = G_{X2}/\left(1+T_{ig}\right)$, and the closed transfer function of the current control loop can be written as $\Phi_{inv} = T_{ig}/\left(1+T_{ig}\right)$, so both of them have the same poles. As a consequence, to guarantee all poles of Y_{inv} in the left half plane of s-domain, the parameters of the closed loop must be designed reasonable to ensure the current control loop is stable.

The paralleled admittance of PLL can be derived as $Y_{PLL} = -I_m G_{PLL} T_{ig}/\left(1+T_{ig}\right)$ from (26), and the closed loop transfer function of PLL is $\Phi_{PLL} = I_m G_{PLL}$. The poles of Y_{PLL} equal to the poles of Φ_{PLL} add the poles of Φ_{inv}. If the current control loop and PLL are stable, all the poles of Y_{PLL} in the left half plan, which means Y_{PLL} is stable.

Under a strong grid, the admittance of the grid can be neglected because its value is very small, i.e. $Y_g = \infty$. If the current control loop and PLL are stable, Y_{inv} and Y_{PLL} can be guaranteed stable, which provides Y_0 is stable. Therefore, in this situation, the stability of the system depends on the stability of current control loop and PLL. The condition of guarantee the system stable is ensure the current control loop and PLL is stable respectively.

2) Weak Grid

The admittance of the gird can't be neglected in a weak grid. For system stability analysis, it can be assumed that the admittance of the inverter with PLLY_0 is stable. In this situation, the stability of the current depends on the stability of the second term on the right-hand side of (28), define $H(s)$ as

$$H(s) = \frac{1}{1+Y_0/Y_g} \tag{30}$$

The impedance-based stability criterion is based on the observation that $H(s)$ resembles the close-loop transfer function of a negative feedback control system where the forward gain is unity and the feedback gain is Y_o/Y_g; that is, the ratio of the inverter output admittance to the grid output admittance. By linear control theory, *H(s)* is stable if and only if Y_o/Y_g satisfies the Nyquist stability criterion [8].

From the analysis in these two situations, the conclusion can be obtained as: If the system is stable, two conditions must be satisfied: 1) the output admittance of the grid-inverter Y_0 is stable; 2) Y_o/Y_g satisfied the Nyquist stability criterion.

B. Influence of PLL on the Stability of Inverter

From (26), it can be observed that the PLL introduced a negative admittance Y_{PLL} to the output admittance Y_o of the grid-connected inverter, which will reduce the amplitude and phase angle of Y_o, and reduces the stability margin of the system. It may even cause system instability. However, in the factor of Y_{PLL}, T_{ig} is determined by the grid current closed loop design, thus only I_m and G_{PLL} affect Z_{PLL}. The following is analyzes the effect of these two variables on the admittance of the inverter with PLL Y_o.

1) Reference current amplitude I_m.

The larger I_m leads the amplitude of Y_{PLL} larger, and Y_o is in the form of Y_{PLL} in parallel with Y_{inv}. And the admittance of the inverter with PLL Y_o mainly depends on a larger parallel admittance. Therefore, the phase margin and stability of the system can be decreased by a larger amplitude of the reference current I_m, which has a large impact on the admittance of PLL Y_{PLL}.

2) G_{PLL}.

The transfer function of PLL G_{PLL} takes on the characteristics of the low pass filter above the fundamental frequency f_0 and assumes its bandwidth is f_{BW}. Therefore, when $f > f_{BW}$, the amplitude of G_{PLL} decreases when the frequency increases. At the same time when $f > f_0$, the phase frequency curve of G_{PLL} has a $0° \sim 90°$ phase shift. The amplitude and phase angle of $1/G_{PLL}$ is lower at the high frequency with a larger bandwidth of the G_{PLL}, thus result in the amplitude and phase angle of Y_{PLL} is smaller, which reduces the amplitude and phase of Y_o, so the phase margin and the stability of the system is decreased.

As the amplitude of the reference current I_m is the given parameter in the system; thus, in order to get a stable system, the bandwidth of the PLL should be set at a low frequency. As a consequence, a compromise exists between PLL response speed and the stability of the system.

To apply the impedance-based stability criterion presented in the aforementioned section, the output admittance of the inverter and the grid admittance were simulated. System circuit diagram and control schemes used as shown in Fig. 1, the system and inverter control parameters are given in Table I. There are three cases will be demonstrated in this part: 1) *T/4* delayed PLL with different bandwidths as 100Hz and 200Hz are used in a weak grid for demonstration how the stability of the system is influenced by the PLL bandwidth. 2) The bandwidth of *T/4* delayed PLL is changed under the condition of half of the power rating, which will be demonstrated that the reference current smaller will be good at the stability of the system with the same PLL bandwidth. 3) The *T/4* transport delayed PLL is replaced by the SOGI-PLL with the same PLL bandwidth 200 Hz to demonstrate how the SOGI-QSG impacts the stability of the system.

1) T/4 delayed PLL.

Fig. 7 shows the bode diagram of the grid-connected inverter output admittance and the grid admittance for the two PLL bandwidths in a weak grid as the inductance of

TABLE. I. PARAMETERS OF A SINGLE-PHASE GRID-CONNECTED INVERTER.

Prameters/Compensator	Symbol	Value
Dc Bus Voltage	U_{in}	400 V
Peak Grid Voltage	U_g	325 V
Fundamental Frequency	f	50 Hz
LCL Filter	L_1	0.36 mH
	C_f	4.7 uF
	L_2	0.2 mH
Sampling Frequency	f_s	10 kHz
Grid Inductance	L_g	7 mH
Current Controller	K_{pcon}	8
	K_{rcon}	800
Peak of the rated Current	I_{ref}	40 A
Different PLL bandwidths	f_{BW1}	100 Hz
	f_{BW2}	200 Hz
SOGI-PLL	k	1.414
	f_{BW}	200 Hz

the grid is 7 mH. With the bandwidths of PLL are 100 Hz and 200 Hz, the grid admittance intersects with the grid-connected inverter output admittance at two different frequencies (180 Hz and 210 Hz) where the phase difference is 154 deg and 192 deg, respectively, indicating that in the first case the design of the PLL bandwidth is 100 Hz has sufficient phase margin exists for the system stability and it is stable, but in the second case with the PLL bandwidth is 200 Hz, the system is unstable.

2) Reducing the power rating.

Fig. 8 shows the bode diagram of the grid-connected inverter output admittance and the grid admittance for these two PLL bandwidths under half of the rated current as 20 A in a weak grid. In this situation the two unstable conditions with PLL bandwidth as 200 Hz becomes stable for their phase margin sufficient the impedance-based stability criterion. This can be matched with the results that the amplitude of the reference current decreased could improve the stability of the system which has discussed in the theoretical analysis.

3) SOGI-PLL

Fig. 9 shows the bode diagram of the grid-connected inverter output admittance and the grid admittance with a T/4 delay and SOGI-PLL with the same bandwidth as 200 Hz in a weak grid. In this situation the unstable conditions with PLL bandwidth as 200 Hz becomes stable by using the SOGI-PLL for their phase margin sufficient the impedance-based stability criterion. This is owe to the low pass filter and band pass filter characteristics of the SOGI-QSG, which can improve the stability of the system by suppressing harmonics pass from the voltage of PCC to the current of the grid.

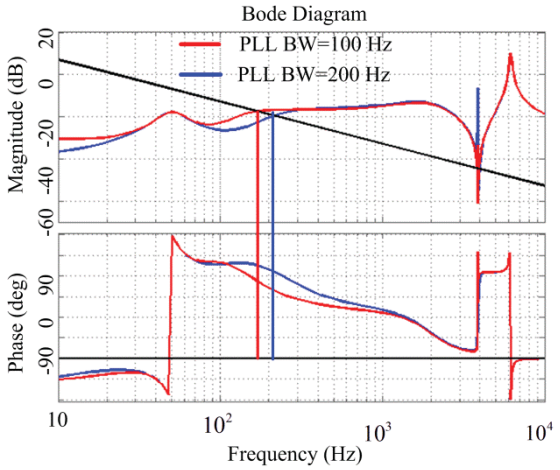

Fig. 7. Bode diagram of grid inverter admmitance with PLL of different bandwidth in a weak grid as the inductance of the grid is 7mH.

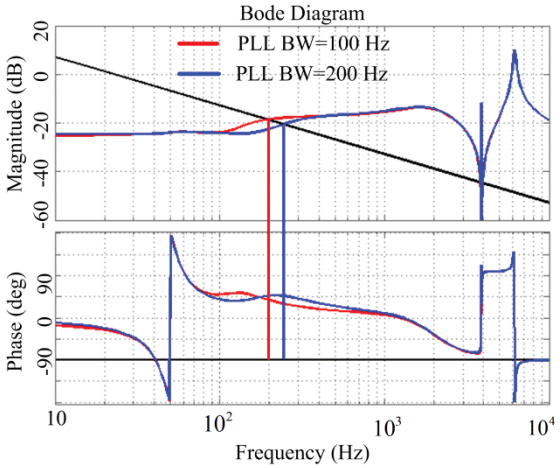

Fig. 8. Bode diagram of grid inverter admittance with PLL of different bandwidth under half of the rated current in a weak grid as the inductance of the grid is 7mH.

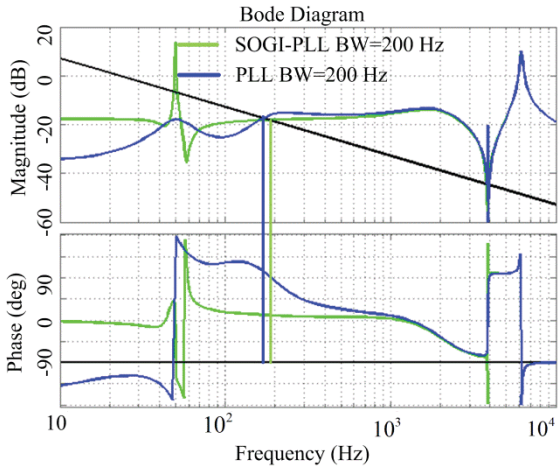

Fig. 9. Bode diagram of grid inverter admittance with different PLL of same bandwidth as 200 Hz in a weak grid as the inductance of the grid is 7mH.

IV. VERIFICATION

The impedance-based stability analysis shown in previous sections indicates that different amplitudes of the reference current and PLL bandwidths will change the output admittance of the inverter. This paper also explores that changing PLL bandwidth will cause instability in the whole system. The advanced PLL as SOGI-PLL will improve the admittance of the inverter by using the SOGI-QSG for its low pass filter and band pass filter characteristics.

To verify the stability analysis in the previous section, a 6 kW single-phase grid-connected inverter has been studied, where the bandwidth of PLL and power rating can be varied. The parameters are set to be the same as given in Table. I. An additional inductor was inserted to increase the grid admittance and emulated as a weak grid.

Fig. 10 demonstrates the steady-state voltage and current waveforms with PLL bandwidth is 100 Hz under a weak power grid (L_g=7 mH). From Fig.10, It can be shown that the system is stable for it has the sufficient phase margin from the analysis of previous section.

Fig. 11 and Fig. 14 present the steady-state voltage and current waveforms as well as the current spectrum with PLL bandwidth is 200 Hz under a weak power grid (L_g=7 mH) and the rated current 40 A. From Fig. 14, it is indicated that a significant 3rd and 5th harmonic existed in the current. The dominant harmonic frequencies are separated by 100 Hz and their center frequency is 200 Hz, which is approximately the same as the frequency at which the admittance overlap exist in Fig. 7 (210 Hz), when the PLL bandwidth was set to 200 Hz and validates the theory. This leads to an under-damped resonance and explains the observed strong 3rd and 5th harmonics. Thus, the harmonic frequency in the system will be predicted by the stability criterion.

Fig. 12 shows the voltage and current waveforms of the inverter with PLL bandwidth 200 Hz under a weak power grid when the current decrease to half of the rated 20 A. As long as the amplitude of reference current decrease, the phase margin of the system will be bigger and the system is more stable. As a consequence, from Fig. 12, it is shown that when the current decreased to half of the rated value with the same high bandwidth of PLL, the system becomes stable.

Fig. 13 and Fig. 14 demonstrate the steady-state voltage and current waveforms as well as the current spectrum with SOGI-PLL bandwidth is 200 Hz under a weak power grid (L_g=7 mH). From Fig.13, It can be shown that the system is stable, there is no significant harmonics in the grid current which can be matched with the bode diagram in Fig. 9.

V. CONCLUSION

This paper discusses the impact of a conventional PLL on the output admittance of a photovoltaic single-phase inverter. The analysis demonstrates that the PLL introduces a parallel admittance to the output admittance of the inverter. A wide bandwidth PLL will decrease the stability margins at the grid-inverter interface which can lead to instability of the inverter, when the grid is weak,

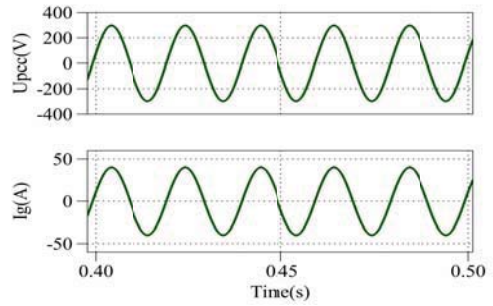

Fig. 10. Inverter terminal voltage and output current with PLL bandwidth 100 Hz in a weak grid (L_g=7 mH).

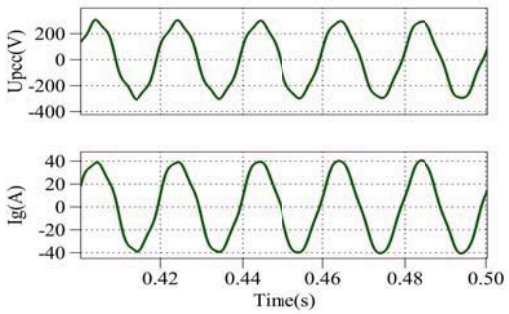

Fig. 11. Inverter terminal voltage and output current with PLL bandwidth 200 Hz in a weak grid (L_g=7 mH).

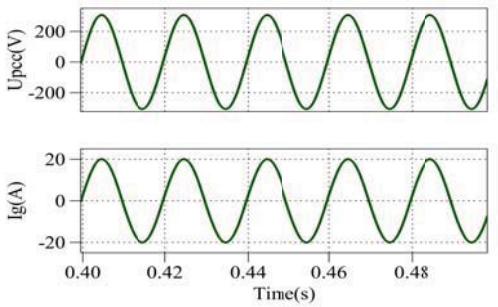

Fig. 12. Inverter terminal voltage and output current with PLL bandwidth as 200 Hz under half of the rated current in a weak grid (L_g=7 mH).

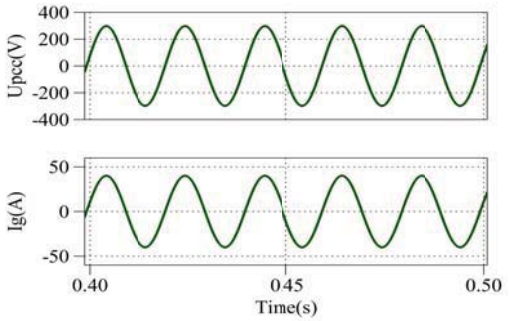

Fig. 13. Inverter terminal voltage and output current with SOGI-PLL bandwidth as 200 Hz in a weak grid (L_g=7 mH)

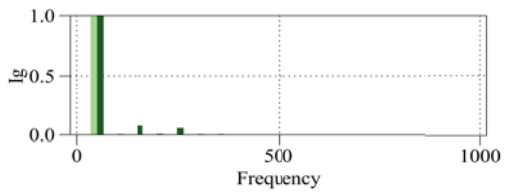

Fig. 14. Inverter terminal current spectrum with T/4 delay PLL and SOGI-PLL bandwidth is 200 Hz in a weak grid (L_g=7 mH). The light green is SOGI-PLL and the dark green is T/4 delay PLL.

i.e., it has a high inductance. The Second Order Generalized Integrator PLL (SOGI-PLL) is also modeled. It is found that the quadrature signal generator of SOGI plays a stabilizing role in grid-inverter interactions, which thus provides a promising candidate for avoiding the PLL-induced instability in single-phase inverters. Moreover, simulation results demonstrate how the inverter becomes unstable, when the PLL bandwidth increases. The Nyquist stability criterion is applied in both the stable and unstable cases, and system stability conditions and the resonant frequencies can be predicted by this method.

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