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A 0.76-pJ/Pulse 0.1-1 Gpps Microwatt IR-UWB CMOS Pulse Generator with Adaptive PSD Control Using A Limited Monocycle Pre-Charge Technique

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Abstract—This paper presents an ultra wideband pulse generator topology featuring adaptive control of power spectral density for a broad range of applications with different data rate requirements. The adaptivity is accomplished by employing a limited monocycle pre-charge approach to control the energy used for pulse generation at different desired data rates. By doing so the need for tuning circuits is eliminated and the radiated power is maintained at the highest level allowed by FCC. A prototype pulse generator has been implemented using the UMC 180 nm CMOS process for validation. The measured results show that the pulse generator can be used for a wide pulse repetition rate range from 100 Mpps to 1 Gpps. In addition, the pulse generator consumes 0.76 pJ/pulse at 1 Gpps, equivalent to 760 μ W, and has a compact size of 0.09 mm².

Index Terms—adaptive PSD control, IR-UWB, pulse generator.

I. INTRODUCTION

IMPULSE radio ultra wideband (IR-UWB) is a wireless technology featuring the unique potential of low power dissipation, robustness against multi-path fading, and feasibility in localization. For those reasons it has been considered a promising technology for various short range applications, such as wireless sensor networks (WSNs) [1], body area networks [2, 3], and medical electronic devices [4, 5]. In order for UWB to co-exist with narrow band communication technologies, FCC has allocated the UWB band mainly in 3-10 GHz with a stringent equivalent isotropically radiated power (EIRP) limit of -41.3 dBm/MHz [6]. One of the most important concerns in IR-UWB design is to fulfill these regulations. Hence significant attention has been devoted to the design of the UWB pulse generator which is the key block in determining the power spectral density (PSD) of the IR-UWB signal [7–11]. To obtain optimum system performance

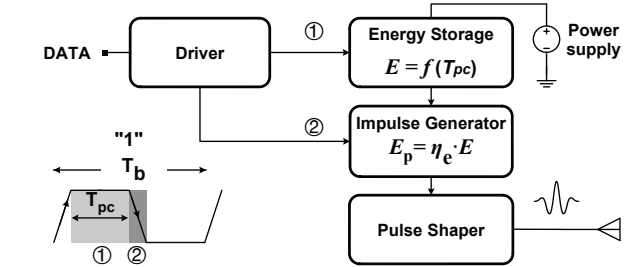


Fig. 1. The proposed IR-UWB pulse generator topology.

it is usually preferred to keep the radiated power of the UWB pulse generator closely below the EIRP limit. As a result, the UWB pulse is transmitted with the maximum energy allowed by the regulation of FCC at the specific data rate. This is done to achieve the lowest possible BER or longest possible communication distance.

However, the applications targeted by IR-UWB require different data rates, typically ranging from tens of kpps to several hundreds of Mpps. Previously reported UWB pulse generators usually offer fixed pulse amplitudes and thus for each specific application a specific design is preferred for optimum performance [7]. Furthermore, several short range wireless applications, such as wireless ultrasound video streaming, prefer adaptively adjustable data rate and signal strength to maintain the communication quality while the communication distance is varying due to the movements of the ultrasound probe or the body of the patient [12]. Therefore, the focus has been drawn to designs with tunable amplitudes in recent years [13, 14]. But tuning circuits are mandatory in these topologies, which increases the circuit complexity as well as power consumption and limits their feasibilities.

This paper proposes a circuit topology for the implementation of UWB pulse generators with adaptive PSDs. By adopting a new limited monocycle pre-charge (LMPC) technique, the energy used for the generation of each single pulse is controlled by the active period of the data signal, which eliminates the need for tuning circuits.

II. THE PROPOSED UWB PULSE GENERATOR

The proposed topology is shown in Fig. 1. It consists of a driver, an energy storage block, an impulse generator and a pulse shaper. This topology is suitable for on-off keying (OOK) with return-to-zero coding (as shown in the embedded

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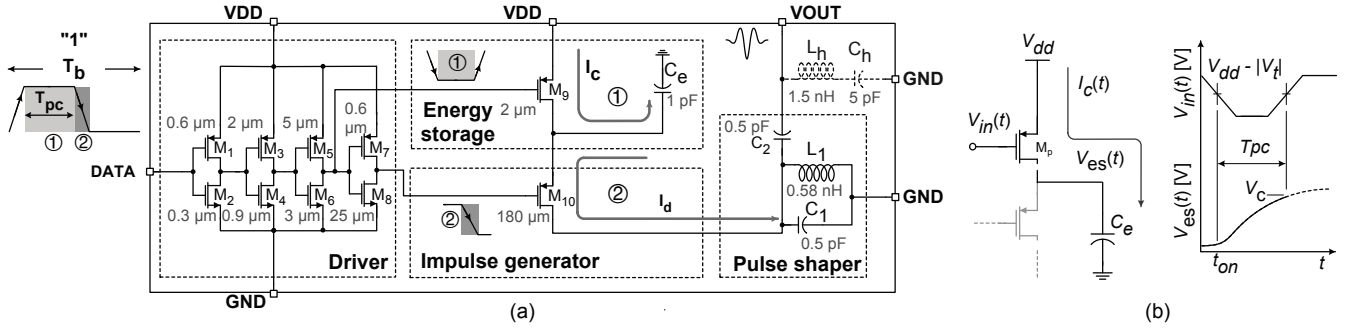


Fig. 2. (a) CMOS implementation of the proposed IR-UWB pulse generator topology in Fig. 1, and (b) charging mechanism of a PMOS transistor with a capacitance load.

figure in Fig. 1). For every bit "1", with a bit period of T_b , the energy storage block is enabled to store energy when the input data voltage becomes high (phase ①). The energy storage takes place during a period of T_{pc} , which is the active period of the monocycle with the duty cycle of $D = T_{pc}/T_b$ (the stored energy is denoted as E). At the falling edge of the input data (phase ②) the stored energy is provided as a power supply for the impulse generator to generate a single impulse with energy of $E_p = \eta_e E$, where η_e denotes the energy conversion efficiency of the impulse generator. Then the pulse shaper ensures the pulse's compatibility with FCC's UWB mask. The key idea here is that the energy storage block should be designed such that the stored energy E is a function of T_{pc} , e.g. $f(T_{pc})$. Thus for different data rates and T_{pc} the energy used for pulse generation varies accordingly. This technique, here called limited monocycle pre-charge (LMPC), provides the adaptive control of the impulse amplitude and eliminates the need for tuning circuits [14]. In order to find a suitable $f(T_{pc})$, a study on the dependence of the UWB PSD on the pulse repetition rate (PRR) is necessary.

Assuming the UWB system is using OOK then the PSD of the IR-UWB signal can be expressed as [15]

$$S(\omega) = \frac{|G(\omega)|^2}{T_b} (p-p^2) + \frac{|G(\omega)|^2 p^2}{T_b^2} \sum_{n=-\infty}^{+\infty} \delta(\omega - \frac{2\pi n}{T_b}), \quad (1)$$

where T_b is the bit period and $G(\omega)$ is the Fourier Transform of the monocycle UWB pulse. p and $(1-p)$ represent the probabilities of bit "1" and bit "0", respectively. It should be noted that the first and the second term in (1) denote the continuous part, $S_c(\omega)$, and the discrete part, $S_d(\omega)$, of the PSD, respectively. Hence for a UWB transmitter using a fixed p and the same monocycle UWB pulse waveform

$$S_c(\omega) \propto \frac{1}{T_b}, \quad (2)$$

and

$$S_d(\omega) \propto \frac{1}{T_b^2}. \quad (3)$$

Therefore, when the pulse rate varies by a factor of ten $S_c(\omega)$ and $S_d(\omega)$ vary by 10 and 20 dB, respectively [7]. Since it is preferred to have the PSD be independent of the pulse rate, either the energy of the UWB pulse signal or the probability of bit "1" must be reduced reversely. This paper only consider

the possibility of changing the energy of the UWB pulse signal as a varying bit probability, p , will increase difficulties of data recovery at the receiver. Hence the desired dependence of the pulse energy on T_b for a constant discrete PSD, $S_d(\omega)$ is

$$|G(\omega)|^2 \propto \eta_e E \propto T_b^2. \quad (4)$$

If the duty cycle, D , and energy conversion efficiency, η_e , are kept as constants, (4) can be expressed as

$$E \propto T_{pc}^2. \quad (5)$$

It is also easy to derive that for a constant continuous PSD, $S_c(\omega)$, the desired pulse energy to T_{pc} dependence is

$$E \propto T_{pc}. \quad (6)$$

A. CMOS Implementation of the UWB Pulse Generator

In this paper, the proposed topology is implemented using the UMC 0.18 μm CMOS technology to prove the concept. The design is aiming at RZ coded OOK with a bandwidth broader than 1 GHz, a p of 0.5, a D of 25%, a PSD peak of -41.3 dBm/MHz, scalable PRRs from 100 Mpps to 1 Gpps, a power dissipation as low as possible and a compact chip size. As can be seen in (1) the power magnitude of $S_d(\omega)$ and that of $S_c(\omega)$ have a ratio of $p/(T_b(1-p))$, therefore the PSD of the OOK UWB pulse signal will be dominated by $S_d(\omega)$ as p and T_b in this aimed design are 0.5 and less than 10 ns, respectively [15]. Hence the energy storage circuit only needs to fulfill the dependence described in (5).

The circuit implementation is shown in Fig. 2(a). The driver is implemented as a 4-stage inverter chain (M_1 - M_8). The energy storage is realized by a PMOS switch, M_9 , and an energy storage capacitor, C_e . At each rising edge of the input data signal, M_9 is turned on and starts charging the energy storage capacitor C_e (Fig. 2(b)). The energy stored on C_e is given by

$$E = \frac{1}{2} C_e \cdot V_{es}(T_{pc})^2, \quad (7)$$

where $V_{es}(T_{pc})$ is the voltage to which the capacitor is charged during T_{pc} . The stored energy should be sufficient for the most energy demanding operation case with the aimed low data rate of 100 Mpps. Since an output bandwidth of 1 GHz and a PSD magnitude of -41.3 dBm/MHz are aimed for, the average output power at 100 Mpps is about -11.3 dBm (74

μW). It means that the energy carried by each generated pulse should be 0.74 pJ. Thus a C_e with a value of at least 0.46 pF should be chosen when $V_{es} = V_{dd} = 1.8\text{V}$. To have some design margin to cover the energy loss in the impulse generator a C_e of 1 pF is chosen. At the falling edge of the input data signal, the impulse generator, M_{10} , discharges the stored energy, generating a current impulse I_d . Then the bandpass pulse shaper (C_1 , C_2 and L_1) suppresses the impulse's spectrum components outside the 3-10 GHz UWB band to fulfill FCC's mask. The PSD of the UWB pulse is determined by the duration of discharge through M_{10} , the pulse shaper and the load at VOUT (usually 50 Ohm). Thus a relatively big M_{10} (180 μm) is chosen to make sure that the current impulse is short enough to cover a bandwidth wider than 1 GHz. The values of $C_1 = 0.5$ pF, $C_2 = 0.5$ pF and $L_1 = 0.58$ nH are chosen so that the pulse shaper forms a -3 dB passband from about 5.5 GHz to 15 GHz, aiming for a UWB PSD located in the middle of the UWB band at 6.85 GHz.

It is no trivial task to derive the closed form solution for $V_{es}(t)$ in Fig. 2(b) for deep sub-micron CMOS transistors. However a simplified transient analysis on the capacitively loaded PMOS transistor can be done using its low order RC model, and

$$V_{es}(t) = V_{dd}(1 - \exp(-t/\tau_p)), \quad (8)$$

where $\tau_p = R_p C_e$, and [16]

$$R_p = \frac{1}{\mu_p C_{oxp} \frac{W}{L} (V_{dd} - |V_{tp}|)}. \quad (9)$$

When the charging is over the voltage on the capacitor is

$$V_{es}(T_{pc}) = V_{dd}(1 - \exp(-T_{pc}/\tau_p)). \quad (10)$$

It is easy to see that if T_{pc} is long enough, $V_{es}(T_{pc})$ can be very close to V_{dd} . But if the value of τ_p is big compared to T_{pc} , $V_{es}(T_{pc})$ only reaches a value lower than V_{dd} (here denoted as V_c). Therefore the energy stored on C_e is calculated as

$$E = \frac{1}{2} C_e \cdot V_{dd}^2 (1 - \exp(-T_{pc}/\tau_p))^2. \quad (11)$$

For the case where τ_p is much larger than T_{pc} , meaning a relatively small sized PMOS and a large C_e , then

$$1 - \exp(-T_{pc}/\tau_p) \sim \frac{T_{pc}}{\tau_p}, \quad (12)$$

and hence

$$E = \frac{1}{2} C_e \cdot V_{dd}^2 (T_{pc}/\tau_p)^2. \quad (13)$$

Considering $T_{pc} = DT_b$, thus

$$E = \frac{1}{2} C_e \cdot V_{dd}^2 \frac{D^2 T_b^2}{\tau_p^2}, \quad (14)$$

and hence

$$E \propto D^2 T_b^2 \propto T_{pc}^2. \quad (15)$$

Therefore the desired dependence of the stored energy on the pulse rate in (5) is achieved. A small size for M_9 (2 μm) is chosen so that (12) is valid and the voltage on C_e reaches 80% of the supply voltage during 2.5 ns at 100 Mpps ($T_{pc} = 25\% T_b$). For data rates higher than 100 Mpps, T_{pc} becomes shorter. Consequently the stored energy for pulse generation is reduced (Fig. 2(b)), which results in a desired constant PSD.

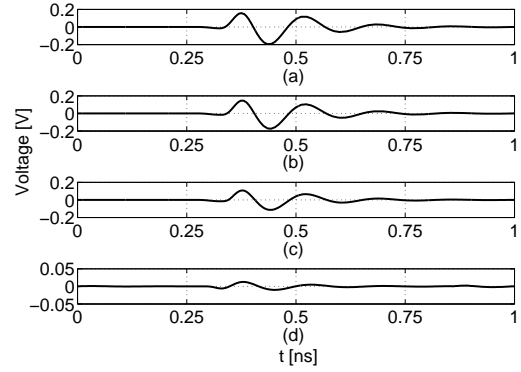


Fig. 3. Simulated pulse waveforms with PRR of (a) 10 Mpps, (b) 50 Mpps, (c) 100 Mpps and (d) 1 Gpps. The duty cycle is kept at 25% for all cases.

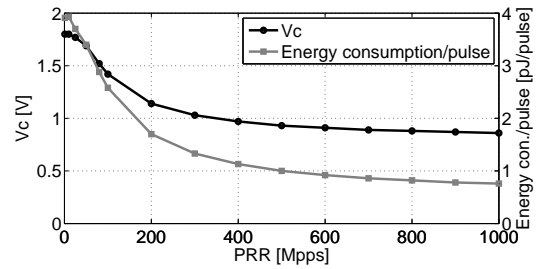


Fig. 4. The simulated voltage on the energy storage capacitor C_e and energy consumption per pulse versus pulse repetition rate.

B. Simulation validation

The simulated waveforms of the generated UWB pulses at four different pulse repetition rates and a fixed duty cycle of 25% are shown in Fig. 3. For easy comparison, the time axes are shifted. It can be seen that the waveforms have an almost consistent shape. The amplitudes for the pulse rate of 10 Mpps and 50 Mpps are close to each other because the energy stored for pulse generation is similar due to the long T_{pc} in the two cases and the proposed LMPC technique is not activated yet. However, from 100 Mpps to 1 Gpps a clear decrease in the amplitude can be seen as the proposed LMPC technique is activated by a T_{pc} shorter than 2.5 ns. The simulated voltages on the energy storage capacitor C_e versus pulse repetition rate is shown in Fig. 4. When the pulse rate is low, e.g. 1 Mpps, C_e can be charged to 1.8 V. As the pulse rate increases, the capacitor voltage drops due to the decreased T_{pc} . The simulated total energy consumption for generating one pulse is also shown in Fig. 4. The energy consumption decreases as the pulse rate increases since less energy is stored for pulse generation. For high pulse rates the energy consumption becomes flat with a value below 1 pJ. This is because the total energy consumption for high pulse rates is dominated by the energy consumption in the driver, which is independent of the pulse rate. Furthermore, the proposed technique does not use oscillators ([1–3]), output driving amplifiers ([8]) or tuning circuits ([13, 14]) and therefore can achieve significantly low power consumption.

The simulated PSDs of the UWB pulse signals at different pulse rates fulfill FCC's UWB mask well with the exception of a small violation at 1 GHz - 2 GHz (Fig. 5). As the UWB antenna usually can add more out-band suppression

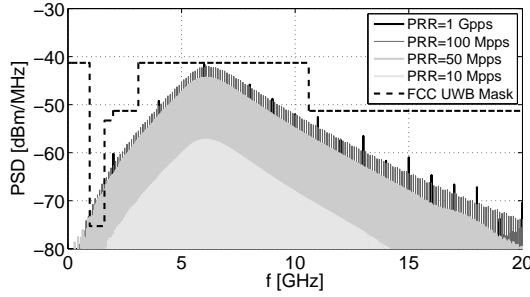


Fig. 5. Simulated PSDs of the UWB pulse signals with pulse repetition rate of 10 Mpps, 50 Mpps, 100 Mpps and 1 Gpps.

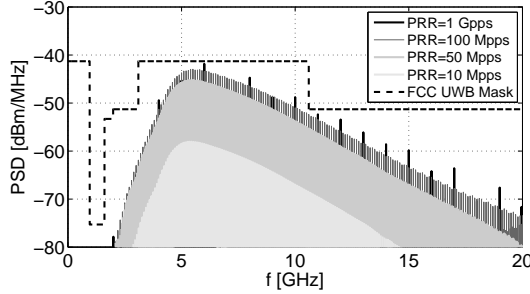


Fig. 6. Simulated PSDs of the UWB pulse signals with the extra series LC resonator (L_h and C_h in Fig. 2(a)) at output for higher suppression at 2 GHz.

to the PSD, the violation here is not a severe issue. But a series LC resonator (L_h and C_h in Fig. 2(a)) can be added at the output of the pulse generator to introduce a transmission zero at 2 GHz (Fig. 6) for applications requiring much higher suppression to cope with PVT variations. Moreover, it is clear that the PSD peaks (the highest PSD magnitude) for 100 Mpps and 1 Gpps in Fig. 5 are close to each other, while the PSD peaks increase significantly as the pulse rate increases from 10 Mpps to 50 Mpps. This is more clearly demonstrated in Fig. 7 that shows the PSD peaks of the UWB pulse signals with a pulse rate ranging from 1 Mpps to 1 Gpps at different corners. It can be seen that the PSD peaks are flat for pulse rates above 80 Mpps, and the variation is less than 1.2 dB for all the cases. Please note that the case with the typical process corner at +27°C with 1.8 V supply (black solid) matches FCC's limit well. Please also note that PSD peaks without the proposed LMPC technique (dashed) will violate FCC's EIRP limit for high pulse rates.

III. EXPERIMENTAL VALIDATION

The prototype chip fabricated using the UMC 180 nm CMOS technology is shown in Fig. 8. The size of the design without measurement pads is $0.3 \times 0.3 \text{ mm}^2$. The PSD of the UWB pulse signal was measured on wafer (without packaging and wire bonding) using a Rohde and SchwarzTM FSQ26 signal analyzer and a probe from Cascade MicrotechTM (Model ACP40-GSG-150). A pattern generator from PicosecondTM (Model 12020) was used as the RZ OOK data source. The UWB pulse generator is working with a supply voltage of 1.8 V and a duty cycle of 25% for the input data signal at all pulse rates ranging from 1 Mpps to 1 Gpps. As shown in Fig. 9, a consistency in the spectrum shapes and PSD magnitudes can

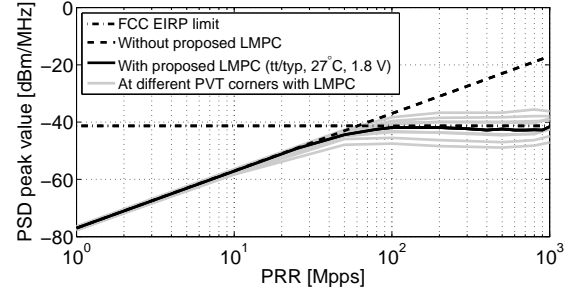


Fig. 7. Simulated PSD peak values versus PRR with corner analysis (process: ff, tt, ss; temperature: -40°C, +27°C, +85°C; voltage: 1.8 V).

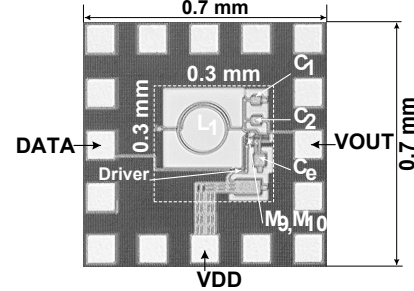


Fig. 8. Microphotograph of the fabricated test chip.

be clearly observed with pulse rates of 100 Mpps, 500 Mpps, and 1 Gpps. The PSDs fulfill FCC's UWB mask well with the exception of a violation of 6.5 dB at about 1 GHz - 2 GHz for the case of 100 Mpps and 500 Mpps. Moreover, comparing to simulation, higher attenuation on the falling side of the PSDs is observed and this might be explained by the parasitic components in the probes and cables. In Fig. 10 the measured variation of the PSD magnitudes from 80 Mpps to 1 Gpps is $< 2.2 \text{ dB}$, which matches the simulation well. Fig. 10 also shows the impact of supply variation on the performance. The deviations in the PSD peak value from the case of $V_{DD} = 1.80 \text{ V}$ are within +2.7 dB and -4.8 dB for the case of $V_{DD} = 1.98 \text{ V}$ and $V_{DD} = 1.62 \text{ V}$, respectively. And the magnitude variations from 80 Mpps to 1 Gpps are well less than 2.6 dB and 1.7 dB for the case of 1.98 V and 1.62 V, respectively. The performance of the implemented UWB pulse generator at three typical pulse rates in the designed pulse rate range is summarized in Table I. By comparison to the latest and best designs it is clear that the proposed design features the lowest energy consumption per pulse, scalable pulse rate, microwatt power consumption, and compact size (no RZ coding/controlling circuits included).

The design specifications in this paper were chosen for the proof of concept. However, the proposed technique can potentially be used for pulse rates lower than 100 Mpps. In that case bigger energy storage capacitor, smaller M_9 and bigger M_{10} should be used to obtain higher pulse energy. By changing the size of M_9 different duty cycles are also achievable. For $> 50\%$ "1" probabilities, smaller C_e should be used to reduce the pulse energy to avoid violating the FCC radiation limit (1). In addition, to avoid violation of the FCC limit due to supply variations, lower pulse energy and smaller C_e should be used to have more PSD magnitude margin to the limit.

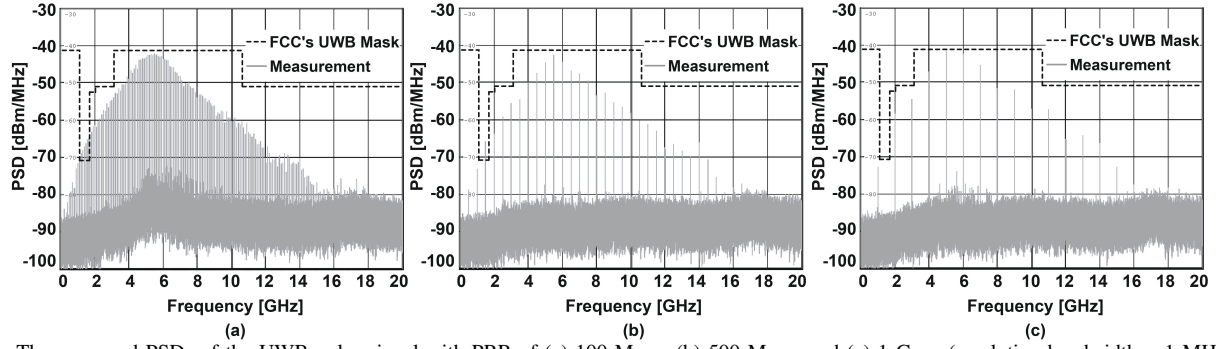


Fig. 9. The measured PSDs of the UWB pulse signal with PRR of (a) 100 Mpps, (b) 500 Mpps, and (c) 1 Gpps (resolution bandwidth = 1 MHz).

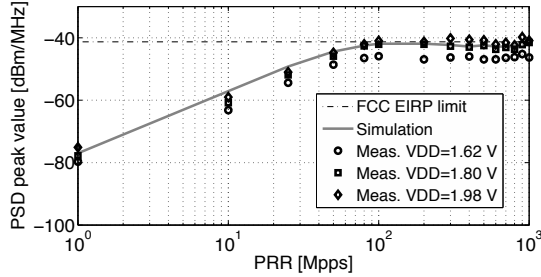


Fig. 10. The simulated and measured PSD peak values versus pulse rate.

IV. CONCLUSION

A UWB pulse generator topology applicable for a broad range of pulse rates is presented in this brief. It is achieved by using a limited monocycle pre-charge technique to enable adaptive PSD control, and the controlling circuits needed for pulse amplitude tuning in conventional designs are eliminated. The proposed topology has been validated by a prototype UWB pulse generator fabricated using the UMC 180 nm CMOS process. Measurements show that the pulse generator can be used for pulse repetition rates from 100 Mpps to 1 Gpps, while maintaining the PSD peak value closely below FCC's EIRP limit. The proposed design consumes only 0.76 pJ/pulse at 1 Gpps, and the chip size is only 0.09 mm². It is suitable for applications requiring different pulse rates or applications where adaptive PSD is desired.

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TABLE I
COMPARISON OF MEASURED PERFORMANCE

Work	CMOS MOD. [μm]	PRR [Mpps]	EP pJ/pulse	BW [GHz]	Power Con. [mW]	Area [mm ²]
[1]	0.18	OOK 2	118	3.3–5.3	0.236	0.188
[2]	0.18	OOK 20	671	1.36	129	4.4
[3]	0.13	BPSK 50	48	3.1–4.8	2.4	0.11
[4]	0.18	OOK 120	9.2	6–10	1.1	1.37
[5]	0.18	OOK 250	20	3–5	5.0	0.08
[7]	0.13	OOK 10	25.6	1.8	0.265	0.1
[8]	0.18	OOK 5	35	0.4	0.175	0.009
[9]	0.09	BPSK 860	14.4	2.4–4.6	12.13	0.18
[10]	0.13	OOK 100	9	6.8	3.84	0.54
[11]	0.09	BPSK 400	65	5.5	26.4	1.9
[13]	0.13	OOK 100	44.4	3–5	4.44	0.168
[14]	0.18	OOK 250	14.6	6.75	3.65	0.16
This work	0.18	OOK	100 2.6 500 1.0 1000 0.76*	3.2–8.2 4–8.5 4–9	0.26 0.5 0.76*	0.09

*: Simulation

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