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Control Architecture for Parallel Inverter in Uninterruptible Power Systems

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***Abstract*— In this paper, a control strategy for the parallel operation of three-phase inverters forming an online uninterruptible power system (UPS) is presented. The UPS system consists of a cluster of paralleled inverters with *LC* filters directly connected to an AC critical bus and an AC/DC forming a DC bus. The proposed control scheme comprises two layers: (i) a local layer that contains a "*reactive power-to-phase droop*" in order to synchronize the phase angle of each inverter and a virtual resistance loop that guarantees equal power sharing among inverters; and (ii) a central controller that guarantees synchronization with an external real/fictitious utility, and critical bus voltage amplitude restoration. Improved transient and steady-state frequency, active, reactive and harmonic power sharing, and global phase-locked loop resynchronization capability are achieved. Detailed system topology and control architecture are presented in this paper. Further, a mathematical model was derived in order to analyze critical parameters effects on system stability. The proposed control approach has been validated by means of experimental results obtained for several case-study scenarios.**

***Index Terms*— UPS system; parallel inverters; voltage restoration; droop control; virtual impedance**

I. Introduction

With the active technological development of modern communication systems, advanced medical equipment, advanced living facilities and emergency systems that requires high quality energy are more and more widespread used in everyday life, which require more reliable, efficient and uninterrupted electricity supply [1]. A large number of such kinds of loads bring an imposing challenge to the existing electricity supply system. Increasing concerns about the reliability and power quality of the utility lead to a growing demand for emergency electricity supply system [2]. Consequently, uninterruptable power systems (UPS) are receiving more and more attention from both engineers and researchers.

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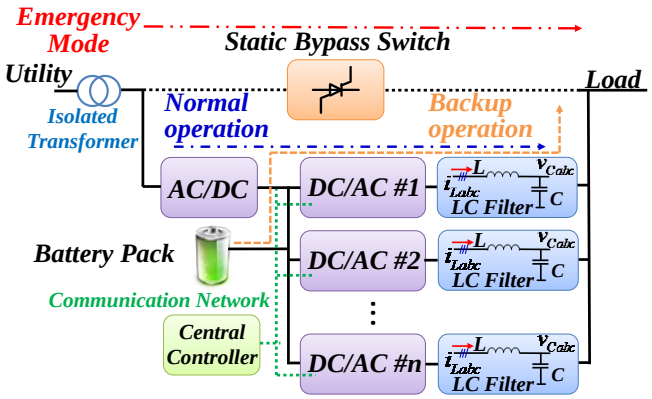

Fig. 1. Proposed Online UPS Structure.

According to the International Electrotechnical Commission Standard IEC62040-3, a UPS system can be divided into three categories, namely offline UPS [3], [4], line interactive UPS [5]-[8] and online UPS [9], [10] according to the energy flow direction under normal utility condition. Due to its outstanding capability of suppressing the utility distortion and interferences, online UPS systems are rapidly proliferating for both high power and voltage application scenarios [11]-[20].

Normally, an online UPS system is composed of an AC/DC (controlled rectifier), an inverter (DC/AC), a battery pack, a static bypass switch and isolating transformers as shown in Fig. 1. The AC/DC power stage takes the responsibility of regulating DC bus and acts as battery-pack charger at the same time under normal condition (*normal operation*). Otherwise, the online UPS system switches to backup mode and battery pack will regulate DC bus voltage instead of AC/DC (*backup operation*). On the other hand, the static bypass switch connects the load to the AC input directly in case of power conditioner failure or overload [9] (*emergency mode*).

In order to achieve high reliability and flexibility, a cluster of parallel DC/AC modules are employed to work together as the inverter stage in the online UPS system. As a result, a number of control schemes for the parallel operation of inverters are proposed in [21]-[35]. Until now, multiple control solutions can be found in the literatures, namely centralized control [21]-[23], master-slave control [24]-[27], averaged load sharing [28]-[31], wired distributed control [32], [33], and circular chain control [34], [35]. Nevertheless, by using the aforementioned techniques, critical intercommunication systems are necessary, thus decreasing the parallel operation

reliability and increasing system complexity. Consequently, a number of communication-less droop control methods [36]-[40] were proposed in order to avoid critical intercommunication. Hence, only local information of each DC/AC module, namely active and reactive powers, is used to regulate DC/AC output voltage amplitude and frequency, which contributes to power sharing among modules. However, their output voltage becomes load dependent, and as a result, secondary controllers are designated to compensate voltage deviations and enhance the parallel operation performance [41], [42]. Information, such as references and local data of each module, can be exchanged through the communications network since mature digital signal processer (DSP) technologies have contributed to a smaller communication delay for instance with the controller area network (CAN) bus [43].

On the other hand, output filter structure of DC/AC also has effects on system stability performance. Usually, *LCL* filter is employed in grid-connected current controlled inverters [44], [45]. In this case, since UPS inverters are voltage sources with *LC* filters, an additional *L* can be used in order to reduce circulating current among modules [52]. However, since *LCL* filter is a third-order system, inherent resonance may occur for certain control parameters, sampling frequency or other undesired disturbances [46]-[48]. Furthermore, adding an output inductor increases the weight, cost and volume of the UPS systems, and, when supplying nonlinear loads, the voltage Total Harmonic Distortion (THD) will increase considerably and complex control techniques should be implemented to reduce it [53]. Therefore, *LC*-type filter is preferred due to its simplicity and reliability compared to *LCL* filter.

In this paper, a parallel control approach for online UPS systems is proposed. DC/AC module is directly connected to AC critical bus with *LC*-type filter, as shown in Fig. 1. Here, only inductor current and capacitor voltage are measured, thus resulting in a cost-effective solution if one current sensor is removed. By calculating reactive power, phase angle is regulated (here named "*reactive power–to–phase droop*" or *Q–ϕ droop*), which aims at achieving reactive power sharing. Consequently, in contrast of using conventional frequency droop methods, system frequency can be locked at 50Hz all the time for different load conditions, which implies a much simpler bypass connection process. At the same time, a virtual impedance loop [39] is inserted into the control loop in order to achieve active power sharing performance by considering the inductor current. Moreover, a central controller is employed in order to compensate voltage sags and phase drift due to *reactive power-to-phase droop or Q–ϕ droop* and the virtual impedance loop. Through communication network (CAN bus), a central controller is used to generate voltage references that needs to be broadcasted to each DC/AC module. After acquiring system references information, local controller of each module uses them to control its own voltage. With central and local control, output voltage amplitude and phase are kept in line with the utility voltage.

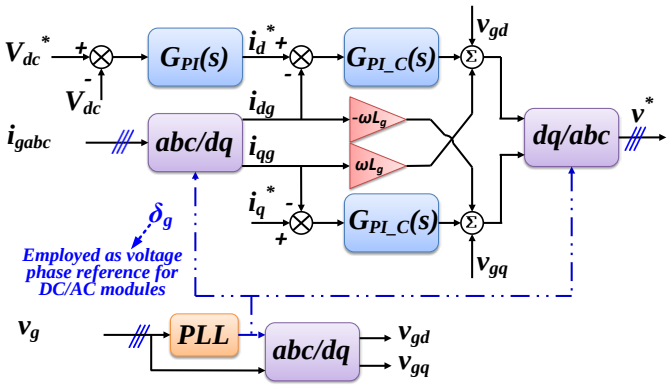

Fig. 2. Control diagram for AC/DC.

This paper is organized as follows. Section II discusses the UPS topologies that are being used and presents the proposed control structure. In order to analyze system stability, a mathematical model is presented and analyzed in Section III. Experimental results are presented in Section IV to prove the proposed control approach feasibility. Finally, conclusions are given in Section V.

II. Proposed Control Scheme for Online UPS System

Compared with offline and line-interactive UPS, online UPS, also named inverter preferred UPS or double conversion UPS, mainly aims at high power and voltage application due to the full controllability of its output voltage and decoupling capability of the utility and the load under power outage [9], [10]. For those aforementioned reasons, it is becoming the most commercialized UPS system in industrial applications. Based on typical online UPS system, a cluster of improved online UPS systems has been proposed, which are more robust at regulating active power to achieve unity power factor [11]-[19]. Additional DC/DC converters [11]-[15], high frequency galvanic isolation [16]-[19] and modular structure are three main issues that are chosen to achieve a cost-effective, volume-effective, and more reliable online UPS system [20].

The modular online UPS system used in this paper, shown in Fig. 1, uses a conventional three-phase controlled AC/DC, and the control diagram is shown in Fig. 2 [49]. Furthermore, the phase information measured by the AC/DC is also employed as the phase reference for the DC/AC modules.

A. Inner Control Loops for DC/AC Modules

Voltage and current control loop in stationary-reference frame are considered in this paper (see Fig. 3), by using proportional resonant (PR) controllers with harmonic compensation capability [50], [51] expressed as follows:

$$G_v(s) = k_{pv} + \frac{k_{rv}s}{s^2+\omega_o^2} + \sum_{h=5,7} \frac{k_{hrv}s}{s^2+(\omega_o h)^2} \quad (1)$$

$$G_c(s) = k_{pc} + \frac{k_{rc}s}{s^2+\omega_o^2} + \sum_{h=5,7} \frac{k_{hrc}s}{s^2+(\omega_o h)^2} \quad (2)$$

being k_{pv} the voltage proportional term, k_{rv} the fundamental frequency voltage resonant term, ω_o the fundamental

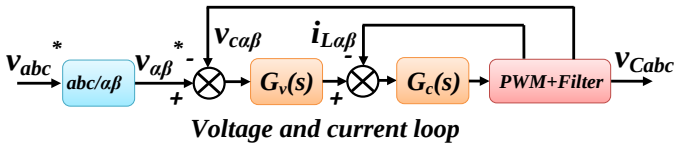

Fig. 3. DC/AC module inner loop control diagram in αβ frame.

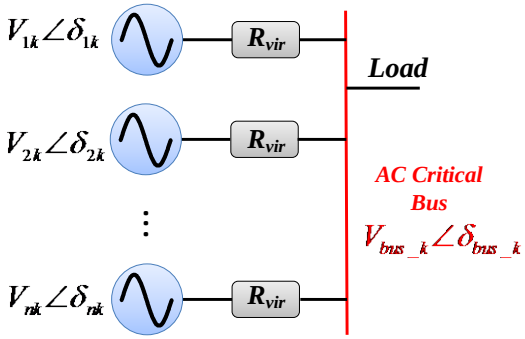

Fig. 4. Simplified parallel DC/ACs system diagram.

frequency, k_{hrv} the h^{th} harmonic voltage compensation term, h the harmonic order, k_{pc} the current proportional term, k_{rc} the fundamental frequency current resonant term, and k_{hrc} the h^{th} harmonic current compensation term. Hereby, only 5^{th} and 7^{th} harmonics have been taken into consideration.

B. *Current-Sharing Loops for DC/AC Modules*

The simplified equivalent circuit of the parallel DC/AC modules is presented in Fig. 4. As a result, if the output impedance of the inverters is enforced to be resistive (R_{vir}) the active power and reactive power that are injected to the AC critical bus can be expressed as follows [38]

$$P_{nk} = \frac{V_{nk}V_{bus\_k}}{R_{vir}}\cos(\delta_{nk} - \delta_{bus\_k}) - \frac{V_{bus\_k}^{\ 2}}{R_{vir}} \tag{3}$$

$$Q_{nk} = -\frac{V_{nk}V_{bus\_k}}{R_{vir}}\sin(\delta_{nk} - \delta_{bus\_k}) \tag{4}$$

being P_{nk} and Q_{nk} the active and reactive power injected by the module n at k-phase, V_{nk} the voltage amplitude of the module n at k-phase, δ_{nk} the angle of the module n at k-phase, V_{bus_k} the voltage amplitude, and δ_{bus_k} the phase angle of the critical bus at k-phase.

By considering that the well-known small power angle (δ_{nk}-δ_{bus_k}) consideration, the approximations ($cos(\delta_{nk}$-$\delta_{bus\_k})=1$, $sin(\delta_{nk}$-$\delta_{bus\_k})=$ δ_{nk}-δ_{bus_k}) are often used to decouple respectively active and reactive power as follows:

$$P_{nk} \approx \frac{V_{bus\_k}}{R_{vir}}\left(V_{nk} - V_{bus\_k}\right) \tag{5}$$

$$Q_{nk} \approx -\frac{V_{nk}V_{bus\_k}}{R_{vir}}(\delta_{nk} - \delta_{bus\_k}) \tag{6}$$

Consequently, the active power of each module can be regulated by output voltage amplitude, while reactive power can be controlled by regulating the phase angle. In this sense, a virtual impedance loop is proposed to share the active power

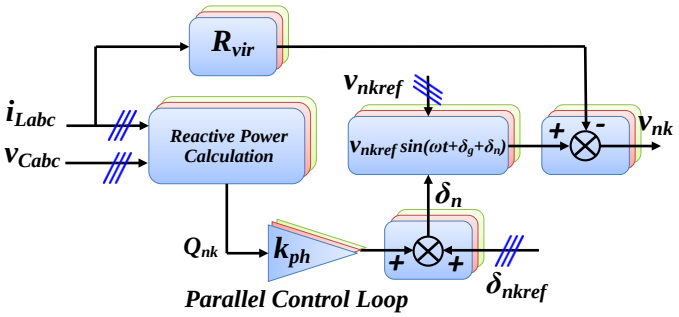

Fig. 5. Virtual impedance and "reactive power to phase droop" control diagram.

and a *Q–ϕ droop* is proposed to share reactive power. These loops are embedded into the control scheme to achieve parallel operation and power sharing, as shown in Fig. 5:

$$V_{nk} = V_{nkref}\sin\left(\omega t + \delta_g + \delta_n\right) - R_{vir}i_{nLabc} \tag{7}$$

$$\delta_n = \delta_{nkref} + k_{ph}Q_{nk} \tag{8}$$

where n is the number of DC/AC module ($1, 2, 3…N$), k is the phase order (a, b, c), V_{nkref} the nominal voltage reference, R_{vir} the virtual resistor, δ_g is the utility phase angle, δ_{nkref} the nominal phase reference, k_{ph} the phase regulating coefficients, and Q_{nk} the reactive power of each phase of each DC/AC module. Note that δ_{nkref} is equal to δ_g in Fig. 2.

Simulations were carried out by using the power electronics simulation software PLECS in order to illustrate the detailed process originated by the virtual impedance loop (7) and the *Q–ϕ droop* controller (8). Two DC/AC modules are given a phase error.

In order to analyze the active power sharing performance, virtual impedance loop is enabled while *Q–ϕ droop* control is disabled, ie k_{ph} is 0. At t_1 module #2 is ordered to connect with module #1. Although virtual impedance (7) is trying to regulate the voltage amplitude to the same value, the active power is not shared precisely due to the phase difference between two modules. Module #1 bears more load power than module #2, which means that voltage amplitude of module #2 is higher than module #1 based on (7). As a result, the reactive power of module #1 keeps being reduced until it reached a random steady state as shown in Fig. 6(a). Thus the *Q–ϕ droop* control is enabled and the result is shown in Fig. 6(c). When module #2 is ordered to connect with module #1 at t_3, module #2 phase will be advanced while module #1 phase will be delayed based on (8), which will indirectly decrease voltage amplitude of module #2 and increase the voltage amplitude of module #1. Thus the active power of module #1 is reduced further and the active power of module #2 is increased further until it reaches the same value. At the same time, (8) regulates two modules phase angle to the same value. Thus with same phase angle and voltage amplitude, the active and reactive power is precisely balanced between the two modules as shown in Fig. 6(c).

As for the reactive power balancing, a similar procedure is used, i.e. the virtual impedance is disabled (R_{vir} = 0) and the result is shown in Fig. 6(b). It can be observed that the reactive power is not precisely shared with only *Q–ϕ droop*

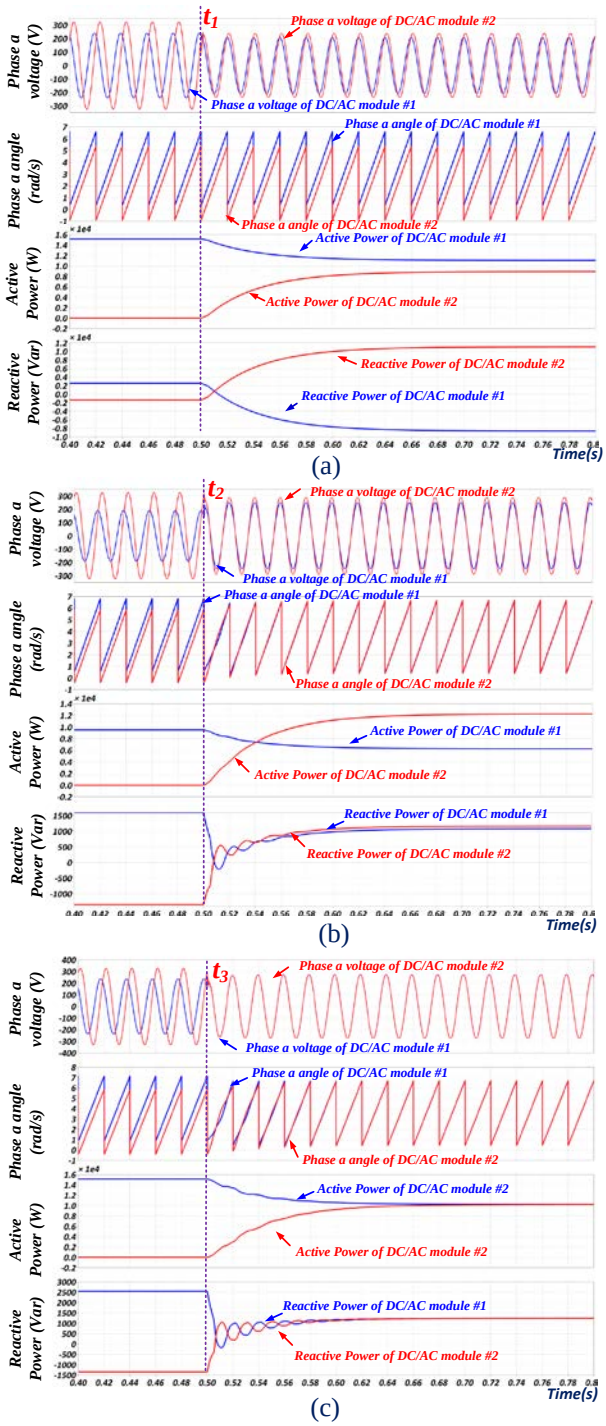

Fig. 6. Active and reactive power sharing transient process: (a) using only virtual impedance (k_{ph}=0); (b) using only *Q–ϕ droop* loops (R_{vir}=0); (c) using both virtual impedance and *Q–ϕ droop* loops.

control. Since reactive power of module #2 is higher than module #1, which means that the phase angle of module #2 is advanced compared with module #1 according to (8), which will result in a higher active power and output current of module #2. Also, the voltage amplitude of module #2 is also higher than module #1 as shown in Fig. 6(b). By applying (7), the voltage amplitude of module #2 will be decreased further due to its higher output current. Consequently, both its reactive and active power is reduced at the same time. Finally,

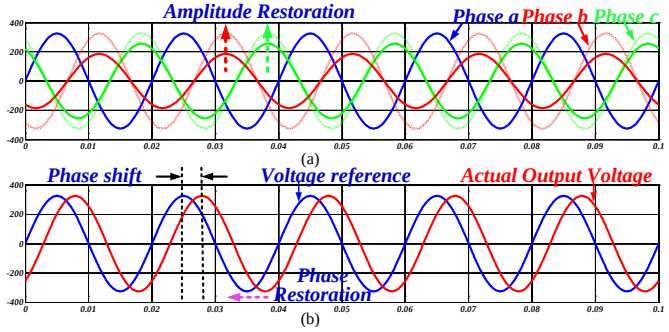

Fig. 7. Voltage and phase deviations. (a) Voltage deviations due to unbalance load. (b) Phase deviations due to "*reactive power–to–phase droop*" or *Q–ϕ droop*.

the power is precisely shared between the two modules as shown in Fig. 6(c).

Here, parameters are chosen to be large in order to show the whole process clearly, so that there are some oscillations during the transient process. It can be concluded that (7) and (8) are required to work together in order to achieve a precise power sharing performance.

In order to avoid voltage unbalances when supplying single-phase loads, each phase voltage references are calculated and modified as follows (Note that each phase reactive power is calculated respectively):

$$v_a = V_{aref} \cdot \sin(\omega t + \delta_g + k_{ph} Q_a) - R_{vir} i_{La} \quad (9)$$

$$v_b = V_{bref} \cdot \sin(\omega t + \delta_g + k_{ph} Q_b) - R_{vir} i_{Lb} \quad (10)$$

$$v_c = V_{cref} \cdot \sin(\omega t + \delta_g + k_{ph} Q_c) - R_{vir} i_{Lc} \quad (11)$$

C. UPS System Central Control

According to the aforementioned analysis, due to virtual impedance action, each phase voltage of DC/AC module will have different deviations in case of unbalanced load condition. Thus, voltage amplitude must be restored as shown in Fig. 7(a). On the other hand, phase shift caused by the *Q–ϕ droop* control should be reduced by the central controller, as shown in Fig. 7(b). According to the aforementioned analysis, since the utility phase information is employed as the phase reference, there may exist a phase difference between the utility voltage and UPS output voltage, which is an undesired condition for an online UPS system. Hence a central controller that deals with voltage amplitude and phase restoration is implemented. Considering that each phase voltage may experience different load conditions, references are generated and modified respectively.

Each DC/AC sends its own RMS value of capacitor voltage to the central controller through the communication network. Central controller obtains the average of RMS values of each phase voltage respectively, shown in Fig. 8. For instance, average value of all DC/ACs phase *a* RMS voltage is derived,

$$V_{a\_avr} = \frac{1}{n} \sum_{i=1}^{n} (V_{ia}) \quad (12)$$

where V_{ia} is the phase *a* RMS voltage value of DC/AC #i.

Similarly, average phase angle information is also calculated in the central controller,

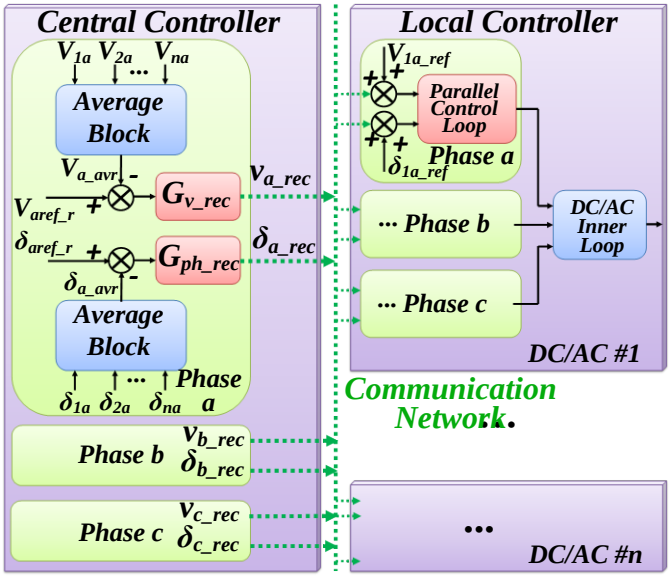

Fig. 8. Overall control diagram for the online UPS system.

$$\delta_{a\_avr} = \frac{1}{n}\sum_{i=1}^{n}(\delta_{ia}) \tag{13}$$

where δ_{ia} is the phase *a* angle of DC/AC #i. By employing the compensation block depicted in Fig. 8, the restoration signals for voltage amplitude and phase are derived as

$$v_{k\_rec} = \left(V_{kref\_r} - V_{k\_avr}\right)\cdot G_{v\_rec}(s) \tag{14}$$

$$\delta_{k\_rec} = \left(\delta_{kref\_r} - \delta_{k\_avr}\right)\cdot G_{ph\_rec}(s) \tag{15}$$

being v_{k_rec}, k, V_{kref_r}, V_{k_avr}, G_{v_rec}, δ_{k_rec}, δ_{kref_r}, δ_{k_avr} and G_{ph_rec} as restoration value of voltage amplitude, phase order (*a*, *b*, *c*), RMS voltage reference of phase *k* in central controller, average value of phase *k* RMS voltage value, voltage compensation block's transfer function, phase restoration value of phase *k*, phase reference in central controller (utility phase angle), average value of phase *k* angle and phase compensation block transfer function respectively.

In this scenario, the compensation blocks are implemented by using two typical *PI*s,

$$G_{v\_rec}(s) = k_{pv\_sec} + k_{iv\_sec}/s \tag{16}$$

$$G_{ph\_rec}(s) = k_{p\theta\_sec} + k_{i\theta\_sec}/s \tag{17}$$

being k_{pv_sec} as the voltage proportional term, k_{iv_sec} the voltage integral term, $k_{p\theta\_rec}$ the phase proportional term and $k_{i\theta\_sec}$ the phase integral term.

III. Stability Analysis

In order to analyze system stability, a mathematical model is derived in this Section. Considering that the whole system control scheme consists of three main control blocks, namely inner voltage and current loops, current sharing loops (virtual impedance and *Q–ϕ droop*) and central control (voltage amplitude and phase restoration), the system design model is divided into three parts, which are illustrated in detail in the following subsections.

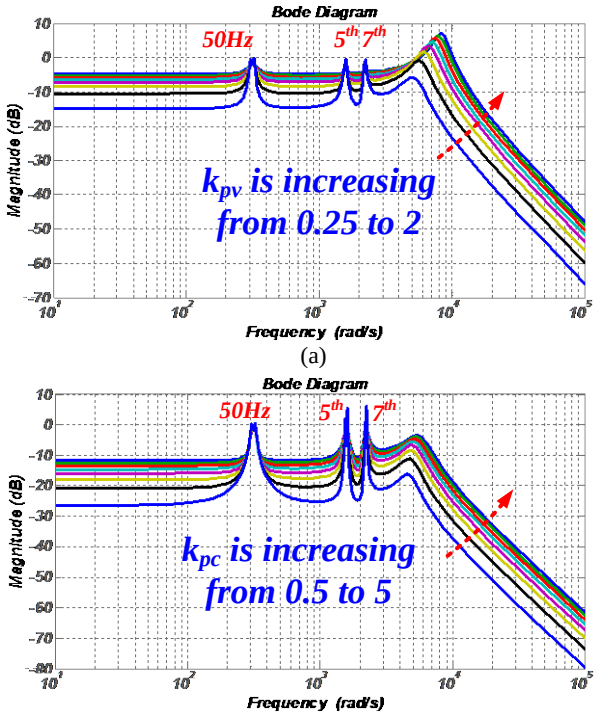

Fig. 9. Bode diagram of inner loop. (a) Bode diagram with variable k_{pv}. (b) Bode diagram with variable k_{pc}.

A. Modeling of Inner Voltage and Current Loop

According to Fig. 3, by combining (1) and (2), the transfer function from reference voltage to output capacitor voltage is derived as follows

$$G(s) = \frac{v_{cabc}}{v_{nkref}} = \frac{d}{as^2 + bs + c} \tag{18}$$

with $a = LZ_{Load}C$, $b = L + G_c(s)G_{PWM}Z_{Load}C$, $c = Z_{Load} + G_c(s)G_{PWM} + G_v(s)G_c(s)G_{PWM}Z_{Load}$, $d = Z_{Load}G_v(s)G_c(s)G_{PWM}$ where L, C, Z_{Load}, $G_v(s)$ and $G_c(s)$ are filter inductance, filter capacitance, load, inner voltage loop and inner current loop respectively; whereas the PWM delay is expressed as

$$G_{PWM}(s) = \frac{1}{1.5T_s s + 1} \tag{19}$$

where T_s is the PWM period.

By plotting the bode diagram of (18), the influence of control parameters on the fundamental frequency and 5th, 7th harmonic frequency is analyzed through plotting Bode diagram of the system is presented in Fig. 9. The bandwidth of the controller is designed to be 1/6 of the switch frequency (10kHz), which is around 1.5kHz. At the same time, a band-pass filter closed loop control behavior, with 0dB gain at specific frequencies (50Hz, 5th harmonic, 7th harmonic) must be guaranteed as shown in Fig. 9. With k_{pv} moving from 0.25 to 2, the bandwidth of the controller is increasing around 1.5kHz and 0dB gain is achieved at specific frequencies. Also a similar performance is observed while changing k_{pc}.

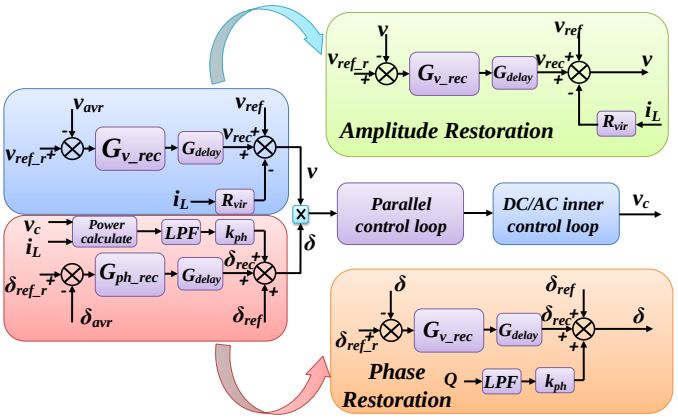

Fig. 10. Control loops for voltage restoration and phase restoration.

B. Virtual Impedance and Phase Droop Loops

According to the IEC 62040-3, voltage variation should be limited to 10%, maximum 48% for IT loads. If the virtual impedance value is constant, the output voltage amplitude will be decreased proportionally to the inductor current. So that the virtual impedance value is chosen as,

$$\left|\frac{i_L R_{vir}}{V_{\max}}\right| \le 0.1 \tag{20}$$

being i_L the inductor current under full load condition and V_{max} the nominal output voltage amplitude. As for the phase droop loop, it is analyzed together with the phase restoration loop since it is tightly related with output voltage phase angle.

C. Central Controller

According to the aforementioned analysis, since the central controller corresponds with UPS output voltage amplitude and phase, its mathematical model can be divided into two parts. In Fig. 10, voltage and phase restoration control (shown in Fig. 8) is simplified and presented with G_{delay} being the delay function caused by communication network. Because each DC/AC module capacitors are connected to the same AC critical bus, v_{avr} is equal to v_c (output voltage of each DC/AC), referring to (12). On the other hand, v_c is tightly controlled by inner loops from the view of communication frequency since dynamics of the local inner loop is much faster than communication. As a result, v_c is treated as the modified voltage reference v. So the model for voltage restoration is able to be simplified as shown in Fig. 10 (Amplitude Restoration). For given G_{delay} similar pattern as G_{PWM} except for a bigger T_c, the model can be derived,

$$v = \frac{G_{v\_rec} G_{delay} v_{ref\_r} + v_{ref} - R_{vir} i_L}{1 + G_{v\_rec} G_{delay}} \tag{21}$$

Considering the dynamic performance of the system, the closed loop function is expressed as follows,

$$G_v(s) = -\frac{1.5 R_{vir} T_c s^2 + s}{1.5 T_c s^2 + (1 + k_{pv\_sec}) s + k_{iv\_sec}} \tag{22}$$

Fig. 11 shows the step response in simulation under different k_{pv_sec} with load step test. For a fixed k_{iv_sec}, different k_{pv_sec} brings different dynamic process. Fig. 12 shows the

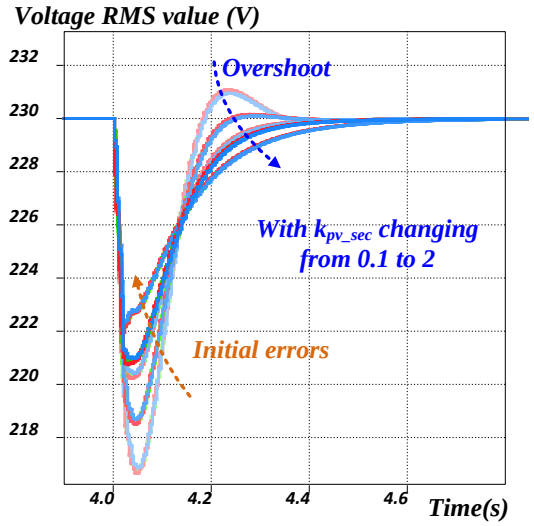

Fig. 11. Step responses of voltage restoration control with different k_{pv_sec}.

pole-zero map of voltage restoration control block. As k_{pv_sec} increasing from 0 to 2, one dominating pole moves towards the origin point, and the second one tends to move towards the stable region slowly, as shown in Fig. 12(a). Also, it can be observed that k_{iv_sec} has small effect on the dominating poles movements. Both two dominating poles almost stay in the same position with variable k_{iv_sec}. Thus mainly k_{pv_sec} determines system dominating poles position, which has crucial impact on the system performance.

Similarly, a simplified control diagram for phase restoration is derived as shown in Fig. 10 (see phase restoration block), from which a mathematical model can be derived

$$\delta = \frac{G_{ph\_rec} G_{delay} \delta_{ref\_r} + \delta_{ref} + G_{LPF} k_{ph} Q}{1 + G_{ph\_rec} G_{delay}} \tag{23}$$

Consequently, the dynamical model can be expressed as follows,

$$\delta = G_{LPF} k_{ph} Q / (1 + G_{ph\_rec} G_{delay}) \tag{24}$$

$$G_{LPF} = \omega_c / (s + \omega_c) \tag{25}$$

$$\frac{\delta}{Q} = (as^2 + bs) / (cs^3 + ds^2 + es + f) \tag{26}$$

$$G_{delay}(s) = 1 / (1.5 T_c s + 1) \tag{27}$$

with the following parameters:

$a = 1.5 T_c \omega_c k_{ph}$, $b = \omega_c k_{ph}$, $c = 1.5 T_c$,

$d = 1.5 T_c \omega_c + k_{p\theta\_sec} + 1$, $e = \omega_c + k_{i\theta\_sec} + k_{p\theta\_sec} \omega_c$,

$f = k_{i\theta\_sec} \omega_c$, where ω_c is the cut-off frequency of power calculation low-pass filter and T_c is the communication delay time. The phase regulation coefficient k_{ph} is on the numerator, which indicates that it has no effect on the system dominating poles distribution. The *pole-zero* map in *Z* domain under different control parameters for phase restoration is presented in Fig. 13. It can be observed that a similar *pole-zero* map performance is obtained, which meaning that the proportional term of phase restoration dominates the system stability.

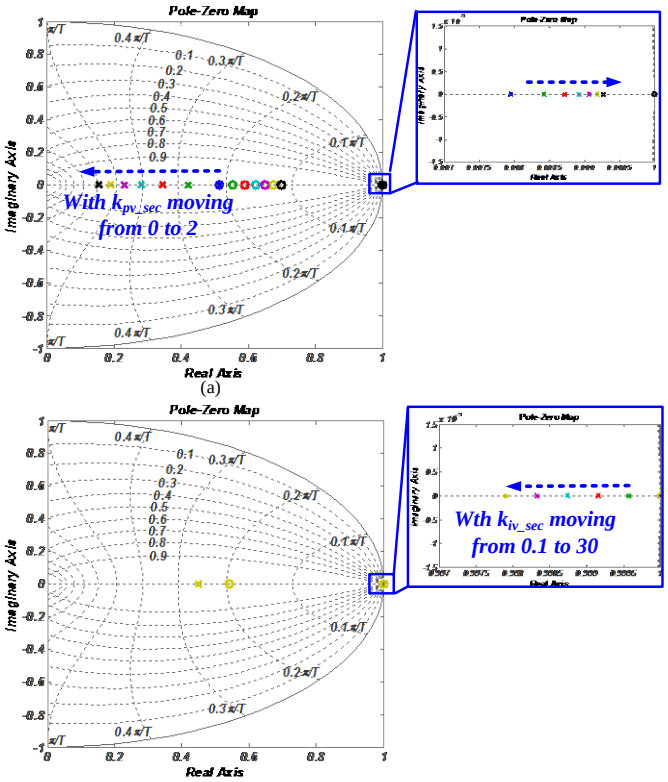

Fig. 12. *pole-zero* map of voltage amplitude restoration. (a) *pz* map with variable k_{pv_sec}. (b) *pz* map with variable k_{iv_sec}.

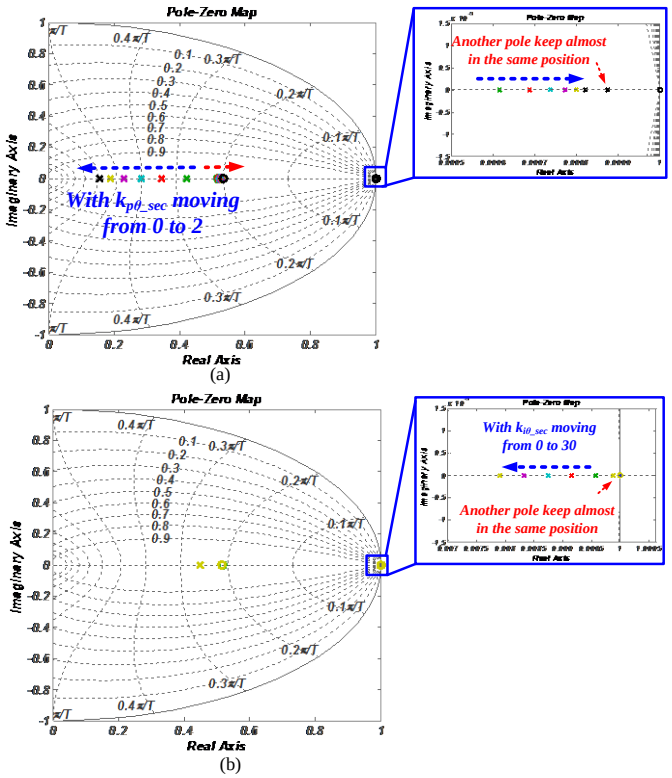

Fig. 13. *pole-zero* map for phase restoration. (a) *PZ* map with variable $k_{p\theta\_sec}$. (b) *PZ* map with variable $k_{i\theta\_sec}$.

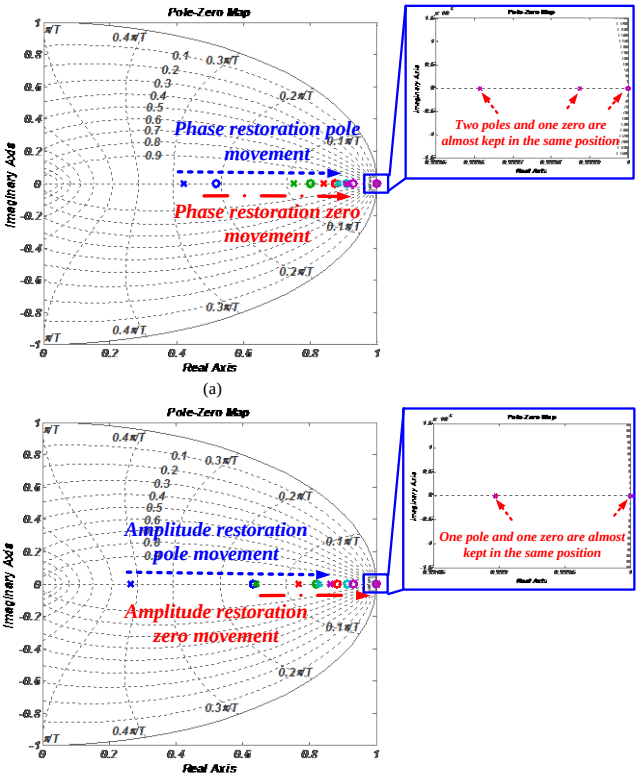

Fig. 14. Communication delay impact on voltage amplitude and phase restoration control. (a) Phase restoration. (b) Amplitude restoration.

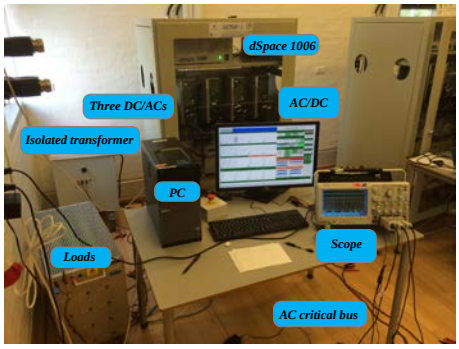

Fig. 15. Experimental setup.

Furthermore, communication delay T_c is also taken into consideration. If T_c is increased to 0.5*s*, one dominating pole of phase restoration is moving towards the boundary of stable area. On the other hand, one zero tends to move out of the unit circle, indicating a slow dynamic performance, as shown in Fig. 14(a). Fig. 14(b) presents the *pole-zero* map for voltage amplitude restoration. The same phenomenon is obtained. Normally, CAN bus have a time delay of hundreds of microseconds according to [43]. So from Fig. 14, it can be concluded that the dominating poles for both voltage amplitude and phase restoration are always kept inside the stable region.

IV. Experimental Results

In order to validate the feasibility of the proposed control, a modular online UPS system, shown in Fig. 1, was built in the laboratory. Fig. 15 shows the experimental setup, which

TABLE I. PARAMETERS FOR EXPERIMENTAL SETUP

Symbol	Parameter	Values
	Converters	
f_{sw}	Switch frequency	10kHz
L_g	Grid side inductor of AC/DC filter	1.8mH
C_1	Capacitor of AC/DC filter	27μF
L_c	Converter side inductor of AC/DC filter	1.8mH
L	Filter inductance of three AC/DCs	1.8mH
C	Filter capacitance of three AC/DCs	27μF
	AC/DC	
V_{dc}	AC/DC reference voltage	650V
P_v	Proportional voltage term	0.1
I_v	Integral voltage term	1
P_c	Proportional current term	19
I_c	Integral current term	677
	DC/AC module	
k_{pv}	Proportional voltage term	0.55
k_{rv}	Resonant voltage term	70
k_{5rv}, k_{7rv}	5^{th}, 7^{th} resonant voltage term	100,100
k_{pc}	Proportional current term	1.2
k_{rc}	Resonant current term	150
k_{5rc}, k_{7rc}	5^{th}, 7^{th} resonant current term	30,30
V_{ref_r}	Reference voltage	230V (RMS)
	Central Control	
k_{pv_sec}	Proportional voltage term	1
k_{iv_sec}	Integral voltage term	20.5
$k_{p\theta\_sec}$	Proportional phase term	0.2
$k_{i\theta\_sec}$	Integral phase term	9
k_{ph}	Phase control coefficients	0.0001rad/VAr
R_{vir}	Virtual resistor	20Ω

TABLE II. TRANSIENT DURATION TIME UNDER LINEAR AND NONINEAR LOAD

	Voltage overshoot or sag (%)	*Duration time (ms)*
Linear Load	14% (overshoot or sag)	20-40
	12% (overshoot or sag)	40-60
	11% (overshoot or sag)	60-100
	10% (overshoot or sag)	100-1000
Nonlinear Load	12% (overshoot) /27% (sag)	40-60
	11% (overshoot) /27% (sag)	60-100
	10% (overshoot) /20% (sag)	100-1000

consists of four *Danfoss* converters, one of which works as an AC/DC module to regulate the DC bus. The other three operate as DC/AC modules. The control algorithm was implemented into a dSPACE 1006 platform for real-time control of the experimental setup. A list of critical parameters that have significant effect on the system performance is presented in Table I. Experiments including both steady and transient operation were carried out to validate the proposed control strategy. And the transient duration time is tested according to the IEC 62040-3, which is shown in Table II.

A. Parallel DC/AC Transient Response

Power sharing performance among different modules is evaluated as shown in Fig. 16. In Fig. 16 (a) and (b), active and reactive power sharing performance among three modules is presented. Module #3 is started at around t_3 = 4.5s while module #1 and #2 are already working in parallel. The active power and reactive power are equally shared during the whole transient process. In Fig. 16(c), it can be observed that it requires 20*ms* to recover the voltage when module #3 starts to work.

A load step was carried out at t=1s. As it can be seen, good power sharing performance among the modules is shown in Fig. 17. Due to the low pass filter for power calculation block, power dynamic process was slower. Moreover, both proper

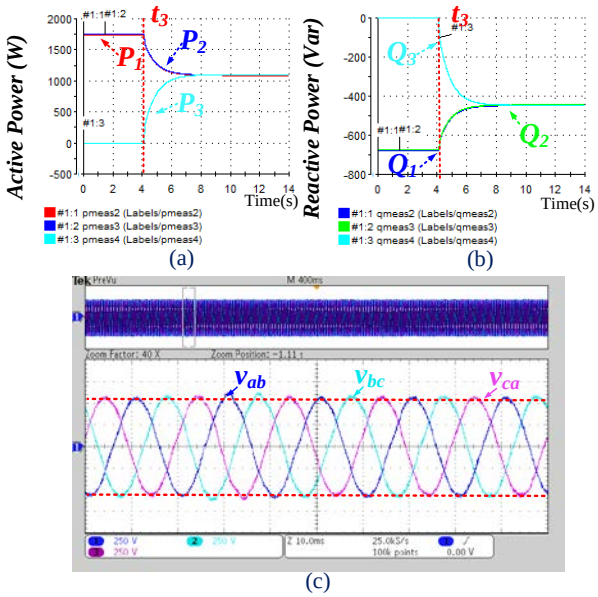

Fig. 16. DC/AC modules parallel performance. (a) Active power sharing between three modules. (b) Reactive power sharing between three modules. (c) Output voltage details.

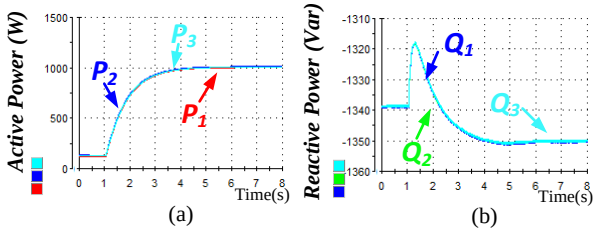

Fig. 17. Active and reactive power of 3 DC/AC modules. (a) Three DC/AC active power. (b) Three DC/AC reactive power.

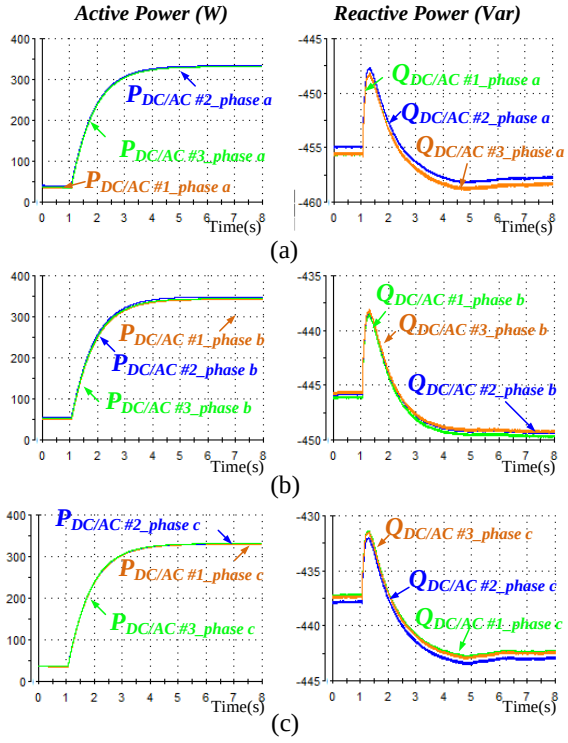

Fig. 18. Active and reactive power per phase. (a) Phase *a* active and reactive power of three DC/ACs. (b) Phase *b* active and reactive power of three DC/ACs. (c) Phase *c* active and reactive power of three DC/ACs.

active and reactive power sharing performance was also guaranteed in phase (*a*, *b* and *c*) of DC/ACs, as shown in Fig. 18. Furthermore, the control performance of the voltage restoration block is also shown in Fig. 19. Fig. 19(a) to (c) show the RMS value of each phase output voltage. A voltage sag of around 8.6%, compared to the nominal output value, has been produced. In Fig. 19(d), AC critical bus voltage was also controlled tightly during voltage sags smaller than 10%.

B. Phase Regulation Control Test

In this scenario, phase errors between the utility voltage and UPS output starting from about 51.5°, as illustrated in Fig. 7(b), was reduced to zero once starting the phase restoration control at t=0.5s, as shown in Fig. 20(a). However, it has some influence over the voltage amplitude in Fig. 20(b). A voltage overshoot of around 4V RMS occurred, which 1.74% of the nominal output voltage value. This meets the transient voltage requirement for UPS system that mentioned in the standard IEC 62040-3. Due to the voltage amplitude restoration control action, the amplitude was restored back to the nominal value few cycles later.

C. Grid Synchronization Process Tests

Considering the UPS as a whole system, both steady and dynamic performance of the system should be tested at AC critical bus of the UPS system in order to validate UPS system steady and dynamic performance. Synchronization process for

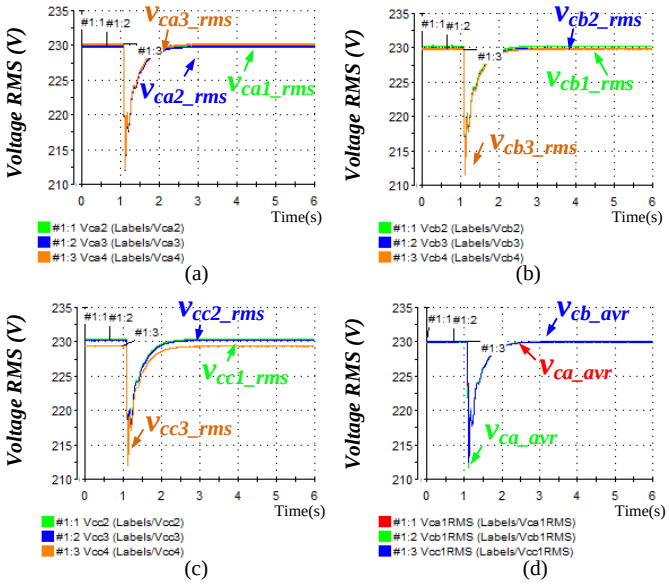

Fig. 19. RMS voltage (Three DC/ACs and AC critical bus). (a) Phase *a* voltage RMS. (b) Phase *b* voltage RMS. (c) Phase *c* voltage RMS. (d) AC critical bus voltage RMS.

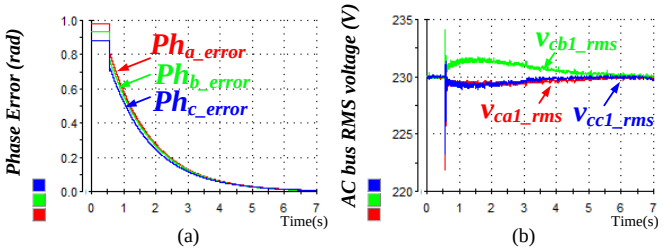

Fig. 20. Phase restoration. (a) Phase errors. (b) RMS Voltage .

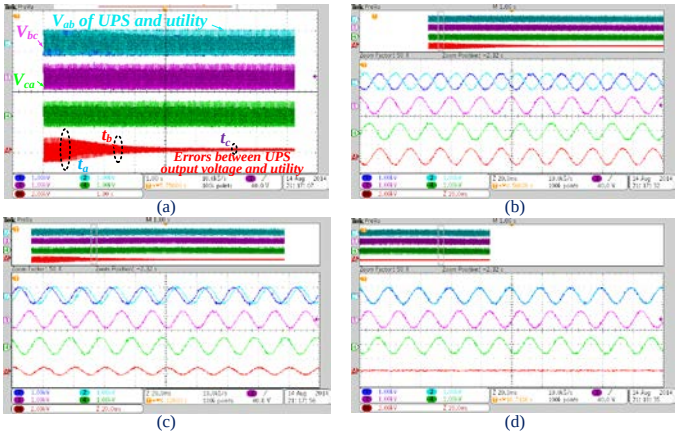

Fig. 21. Synchronization process between $v_{ab\_utility}$ and v_{ab_UPS} under linear load condition. (a) Overall process. (b) Details at t_a. (c) Details at t_b. (d) Details at t_c.

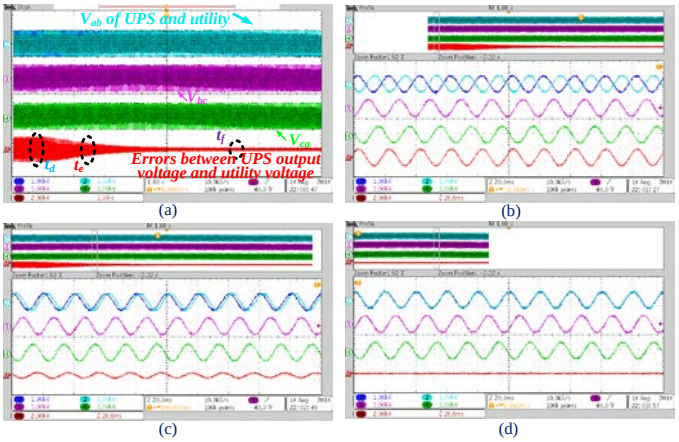

Fig. 22. Synchronization process between $v_{ab\_utility}$ and v_{ab_UPS} under nonlinear load condition. (a) Overall process. (b) Details at t_d. (c) Details at t_e. (d) Details at t_f.

the whole UPS system was tested under both linear and nonlinear load condition. The initial phase error was set to π. Fig. 21 illustrates the synchronizing process with linear load in one phase while Fig. 22 presents results when the nonlinear load is connected. It can be concluded that good synchronization performance had been obtained.

D. Linear Load Sharing Tests

Fig. 23-25 show both balanced and unbalanced load switch performance of the online UPS system. An *R* type load was connected between phases *a* and *b*, while phase *c* is disconnected. Fig. 23 shows both steady state and dynamic voltage and current in case of highly unbalanced load. It can be observed that 5 utility periods (100*ms*) are required to recover the unbalanced voltages with small voltage oscillation when it was suddenly connected.

Similarly, around 5 utility periods, which is 100*ms*, are required to restore voltage when the unbalanced load was disconnected. And this meets the requirement for linear load changing test shown in TABLE II. Additionally, an *LR* type load was connected between phases *a* and *b*, while phase *c* is disconnected. Fig. 24 presents both active power and reactive power performance. At t_g, the *LR* type load was connected and exited this state at t_h. It can be seen that active power are equally shared as shown in Fig. 24(a). At the same time,

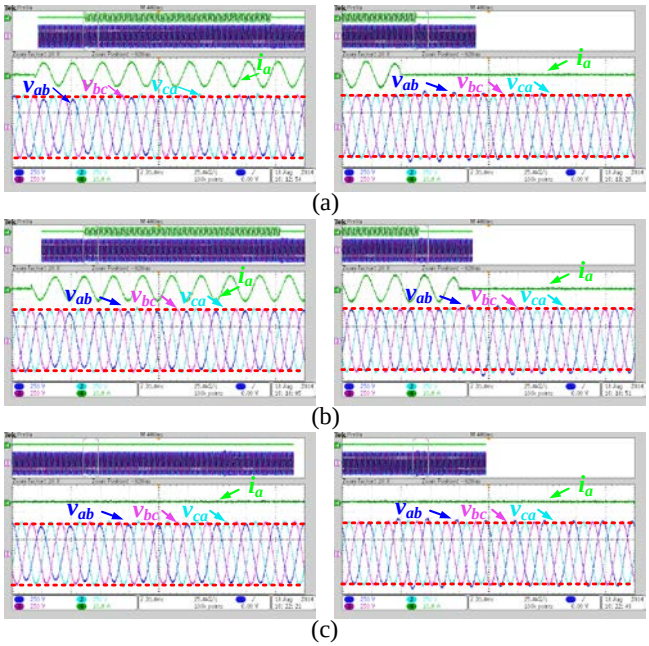

Fig. 23. Voltage and current under unbalanced linear load condition (voltage: 250V/Div, Current: 10A/Div). (a) Output voltage and phase *a* current. (b) Output voltage and phase *b* current. (c) Output voltage and phase *c* current.

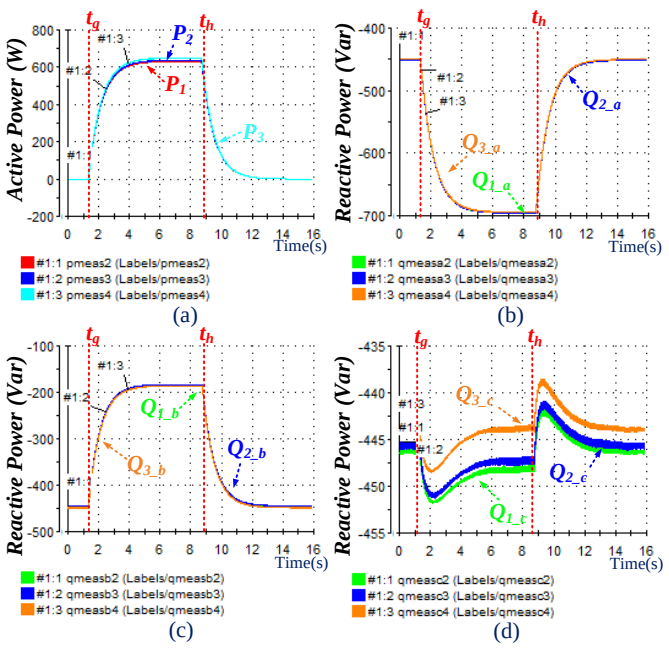

Fig. 24. Active power and reactive power sharing performance under unbalanced nonlinear load condition. (a) Active power. (b) Reactive power of phase *a*. (c) Reactive power of phase *b*. (c) Reactive power of phase *c*.

although each phase faces different reactive power, it is still equally shared among each phase among the three modules (Fig. 24(b)-(d)). And the UPS system output voltage performance is presented in Fig. 25(a) and (b). It can be observed that 1 utility period (20*ms*) are required to recover the voltage. Fig. 25 (c) and (d) depicts the voltage performance under another kind of unbalanced load condition – phase *a* and *b* are connected with *LR* type load while phase c are connected with *R* type load. It can be observed that voltage is recovered to nominal value very fast. Also balanced load test results are shown in Fig. 26. It takes around 40*ms* for the

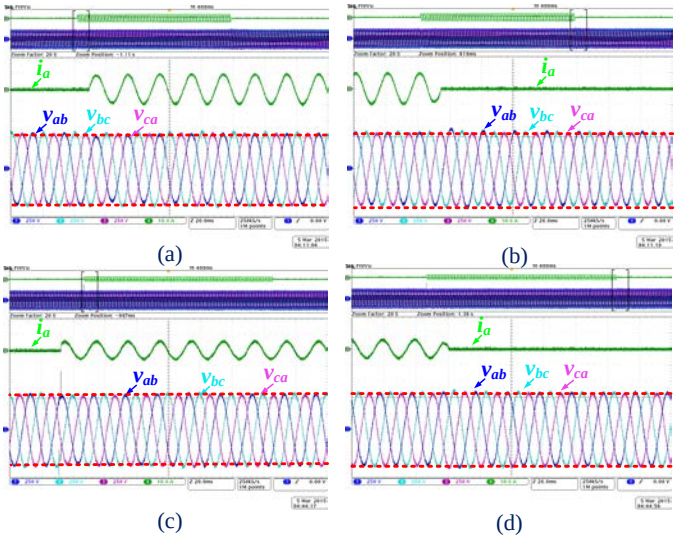

Fig. 25. Voltage and current under unbalanced load condition (Voltage: 250V/Div, Current: 10A/Div). (a) Output voltage and phase *a* current when load is turned on. (b) Output voltage and phase *a* current when load is turned off. (c) Output voltage and phase *a* current when load is turned on. (d) Output voltage and phase *a* current when load is turned off.

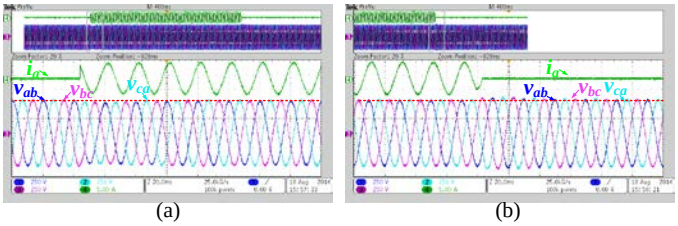

Fig. 26. UPS line to line voltage (phase *a* to *b*) and phase *a* current (Voltage: 250V/Div, Current: 5A/Div). (a) Balanced load connected. (b) Balanced load disconnected.

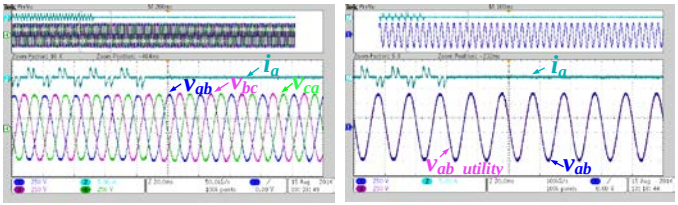

Fig. 27. UPS output voltage and current under nonlinear load condition (Voltage: 250V/Div, Current: 5A/Div). (a) Output voltage and phase *a*'s current. (b) Phase *a* voltage of UPS and the utility.

UPS to recover output voltage to nominal value when the load is suddenly switched on. Once the load is disconnected again, a similar dynamic performance is guaranteed. The recovery process takes around 30*ms*. This also meets requirement shown in Table II.

E. Nonlinear Load Sharing Tests

A diode rectifier circuit was connected to the AC critical bus. UPS line-to-line voltage and phase current were presented. From Fig. 27(a), it can be seen that a small voltage distortion had occurred when the UPS system was connected to the nonlinear load. Fig. 27(b) shows the system performance while UPS keeps synchronizing with the utility. It is noteworthy that the power quality of the UPS output voltage is still maintained while remaining synchronized with the utility when nonlinear load is suddenly connected and disconnected.

V. Conclusion

In this paper, a control strategy intended for an online UPS system was developed under a modular online UPS structure. Active and reactive power is equally shared among different DC/AC modules in linear, nonlinear, balanced and unbalanced load condition under both steady and dynamic process, which is validated through the experimental results. An improved system frequency and phase performance during the transient process is obtained due to the synchronization capability of the central control. Moreover, the total UPS system output voltage is tightly controlled and fast recovered to the nominal voltage value and it meets the UPS application standard IEC62040-3. Critical parameters impacts on the system performance are analyzed hierarchically in this paper, which is a guidance to design the system parameters. With the built modular online UPS system, experimental results are obtained to support the proposed control algorithm.

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