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Published in:
I E E E Transactions on Smart Grid

DOI (link to publication from Publisher):
10.1109/TSG.2015.2488980

Publication date:
2016

Document Version
Early version, also known as pre-print

A Control Architecture to Coordinate Distributed Generators and Active Power Filters Coexisting in a Microgrid

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***Abstract*—This paper proposes a control architecture of distributed generators (DGs) inverters and shunt active power filters (APFs) in microgrids to compensate voltage harmonics in a coordinated way. For this, a hierarchical control structure is proposed that includes two control levels. The primary (local) control consists of power controllers, selective virtual impedance loops and proportional-resonant (PR) voltage/current controllers. The secondary (central) control manages the compensation level of voltage harmonic distortion of sensitive load bus (SLB). Compensation of SLB harmonics by control of DGs may cause excessive voltage harmonics at the terminal of one or more of DGs interface inverters and/or overloading of the inverters. After occurrence of each case, active power filter (APF) participates in harmonic compensation and consequently the compensation efforts of DGs decrease to avoid excessive harmonics or overloading of interface inverters. Effectiveness of the proposed control scheme is demonstrated through simulation studies.**

***Index Terms*—Active power filter, Distributed Generator (DG), Hierarchical control, Microgrid, Voltage harmonic.**

I. Introduction

The proliferation of nonlinear loads and power electronic equipment have caused high penetration of harmonic pollution in electrical system. This might result malfunction or overheating devices and motors. These problems can be more severe if the harmonic distortion produced by Distribute Generators (DGs) converters is taken into consideration. Due to this fact, power quality has been considered as one of important issues, recently.

Micrigrids (MGs) are small electrical distribution grids that include DGs, loads and energy storage resources that can operate either connected to the main utility grid (grid-connected) or isolated from that (islanded). Usually DGs connect to electric network by power-electronic converters. The output stage of the converter is an inverter that is able to control output power, voltage and/or current. Recently, many control strategies have been proposed to compensate power quality problems in MGs [1]-[21]. Among others, one of the most important power quality issues is the voltage harmonic which is addressed in the present paper. The works of [1]-[4] are focused on voltage unbalance compensation and thus is not discussed here.

For Voltage Harmonic Compensation (VHC) of MGs, using series or shunt Active Power Filters (APFs) have been suggested [5]-[14]. Generally, APFs inject compensating harmonic current in opposite phase to cancel voltage harmonics of the APF installation point. However, depending on compensation effort of APF, voltage quality at the points other than APF installation bus might degrade [9]. In this line, [13] proposed a control strategy using Distributed APFs (DAPFs) to attenuate voltage harmonics of system. Discrete automatic VHC is proposed in [14] that individual harmonics are mitigated at APF installation point. It is demonstrated in [14] that less capacity of APF is occupied in those strategies based on selective harmonic filtering. Compensation approach of [14] is based on resistance emulation at harmonic frequencies while the same strategy is used in [15]-[21] to address VHC of MG by DGs interface inverters proper control.

In [15], a sinusoidal waveform for DG output voltage is obtained by decoupling fundamental and harmonic components of PWM current and providing controllable resistive behavior for them. Droop characteristic is used in [16] to control the resistance value according to harmonic reactive power of each unit. Voltage Control Method (VCM) and Current Control Method (CCM) are used in [17] to improve output voltage and current of DG, respectively. Furthermore, a single-phase DG is controlled in [18] as an APF to compensate voltage harmonics by injecting harmonic currents. In this method, proper supply of active and reactive power by DG might not be achieved in severe harmonic distortion condition. The methods suggested in [15]-[18] consider DGs output voltage compensation whereas compensation at point of common coupling (PCC) or sensitive load bus (SLB) is in general more important. In fact, voltage of SLB or PCC may become distorted due to the so-called "whack a mole" effect, which means that providing an appropriate voltage quality at all buses (including SLB) may not be possible while voltage compensation is carried out locally [22].

In this sense, voltage THD of PCC is chosen as voltage quality index in [19] while VHC is reduced since violation from DG rated power is occurred. In [20], an interface inverter

This work was supported by the Energy Technology Development and Demonstration Program (EUDP) through the Sino-Danish Project "Microgrid Technology Research and Demonstration" (www.meter.et.aau.dk).

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control method based on VCM is proposed. In this method, VHC of PCC and DG terminal is carried out by proper tuning of compensation gain between -1 and ∞, however, compensation of the both points (DG terminal and PCC) is not achieved simultaneously. A selective compensation approach for mitigating SLB voltage harmonic distortion is proposed in [21] for three-phase MGs. In this method, compensation effort of each DG is proportional to its rated power. Despite significant quality improvement of SLB voltage using this approach, output voltages of one or more of DGs may become too distorted; moreover, the power rating limitation of interface inverters is not taken into account.

Distortion in DGs output voltage reduces power quality in proximity of them and may cause harmful effects on the performance and life of the equipment in those areas. Furthermore, ignoring the rated power of interface inverters may cause damages due to overheating. To cope with these problems, the present paper addresses VHC of MGs considering the voltage quality at SLB as well as DGs terminal. Furthermore, limitation of inverters ratings is taken into account. In fact, the proposed method is considered VHC of SLB by coordinated control of DGs and APFs.

The idea behind the proposed control approach should be considered at the stage of planning and construction of a new MG. At this stage, the topology design criterion is to avoid dedicated power quality conditioners as much as possible and assign the distortion compensation duty to the interface converters of the DGs. This way, capital investment can be reduced. However, since the generation and consumption conditions in a MG can vary significantly, it is probable that the compensation by DGs leads to overloading of them and/or excessive voltage distortion at their terminal. In these conditions, APF(s) can be considered to be installed at SLB to address these requirements.

In a MG that is already designed and installed consisting of some APF(s) so that the compensation priority is with the APF(s) and DGs are as auxiliary compensators, imagine the APF(s) are overloaded and the cooperation of DGs is needed. In this case, there is no guarantee that the DGs can cooperate since their inverters capacity maybe be fully used due to high power generation. In fact, this can be a significant challenge which complicates the control design. Thus, it is better to evaluate the availability of the DGs for compensation and calling APFs when it is necessary as designed in the present paper.

Rest of the paper is organized as follows: in Section II, proposed hierarchical control scheme is described. The local control of APF applied in this paper is explained in Section III. Coordinated control between distributed generators and active power filters is introduced in Section IV. Section V is dedicated to the simulation results of the proposed control scheme and finally, the paper is concluded in Section VI.

II. Proposed Hierarchical Control Scheme

A hierarchical control structure is proposed in this paper. This method includes two control levels, namely primary and secondary. Primary control of each inverter consists of droop controller and virtual impedance loop to share fundamental powers and harmonic current among DGs, respectively. In addition, it contains inner voltage and current controllers. Secondary control is a centralized controller that causes reduction in voltage harmonics of SLB by sending proper control signals to each DG. In addition, this level makes APF cooperate with DGs for compensation whenever is necessary.

Fig. 1(a) shows a general structure of MG with DGs and APFs. Fig. 1(b) depicts the proposed hierarchical control system. It is possible that secondary controller is located far from DGs and SLB; thus, all the signals communicated to secondary control are sent to this level through low bandwidth communication (LBC) [3]. As it can be seen in Fig. 1(b), at first, SLB required data for evaluating SLB voltage ($v_{dq}^{h,1+}$) are measured by "Measurement Block" then they are sent to "DG(s) Compensation Rate Cal." block of secondary control. In this block, SLB voltage distortion rate is estimated. If nonlinear loads are considerable and voltage harmonic compensation of SLB is required, proper signals generated in this block (C_{dq}^{h}) are sent to primary control of each DG to improve SLB voltage by DG(s) inverter. Note that C_{dq}^{h} is the same for all DGs and sharing compensation effort between DGs is considered in "Compensation Effort Controller" block of each DG that is described in the next part. Since compensation of SLB by DG(s) results severe voltage distortion at DG(s) terminal or overloading DG(s) inverter, cooperation of APF(s) is required for compensating SLB. According to Fig. 1(b), voltage distortion rate of DG terminal and overloading DG inverter are checked in "Constraints Block" of each DG; if the cooperation is required for a DG, proper signal (G_i) is calculated in this block. G_i is send to "APF(s) Cooperation Rate" block (to make cooperation with DG(s)) and DG primary control (to reduce DG compensation effort and alleviate voltage distortion of DG terminal). Note that each DG has its own constraint block and APFs only cooperate with those which they need cooperation. In "APF(s) Cooperation Rate" block, the suitable signals (S_i) are generated and sent to control stage of each APF by LBC to share total devolved compensation rate to APFs. To briefly illustrate the proposed control scheme, Fig. 2 shows a simple structure of the proposed control in flowchart configuration. In follow, more explanations concerning different blocks represented in Fig. 1(b) are offered in detail.

A. DGs Primary (Local) Control

Fig. 3 shows block diagram of primary control. Local control contains voltage and current controllers, power droops and selective resistive-inductive virtual impedance loop. For two or more VSIs in MG, active/reactive power circulation might occur between them. To limit the circulation, voltage frequency and amplitude restoration for each VSI is required that is considerable by power droop control. In fact, droop controller regulates output active and reactive power sharing [23]. To apply power droop controller, it is needed calculation of fundamental components of active and reactive power by their instantaneous values (Eq. (1)) to use in power droop control scheme (Eq. (2)) [24].

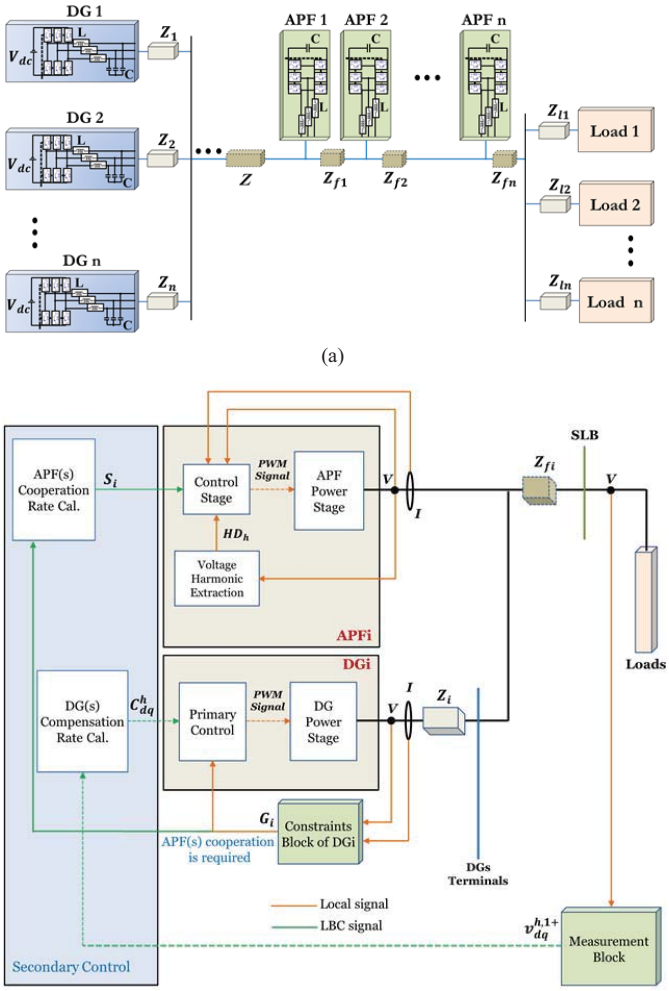


Fig. 1. General scheme of: (a) microgrid, (b) proposed control.

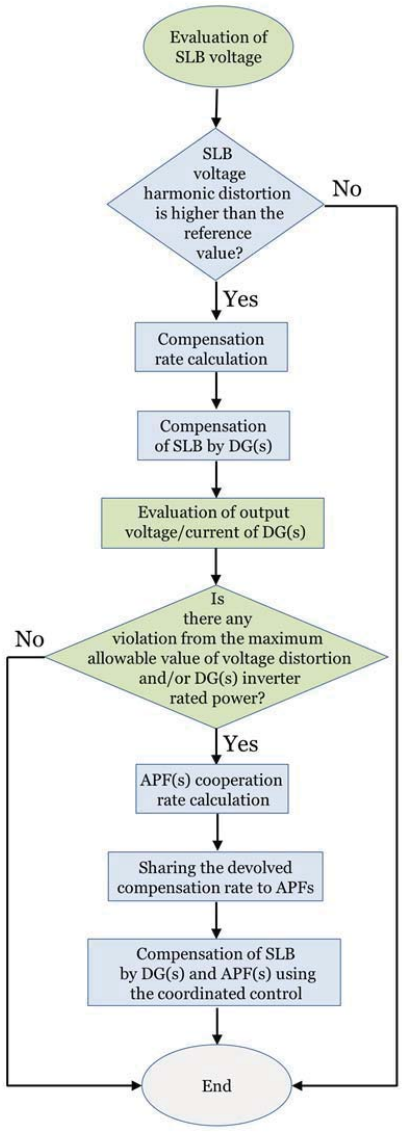


Fig. 2. Flowchart of the proposed control.

$$p = v_{o\alpha} i_{o\alpha} + v_{o\beta} i_{o\beta}\,, \quad q = v_{o\beta} i_{o\alpha} - v_{o\alpha} i_{o\beta}. \tag{1}$$

$$\varphi^* = \frac{1}{s}\omega_0 - \left(\frac{m_i}{s} + m_p\right) P_f, \quad E^* = E_0 - n_p Q_f. \tag{2}$$

where:

s : Laplace variable; E_0 : rated voltage amplitude; ω_0 : rated angular frequency; P_f : fundamental component of active power; Q_f: fundamental component of reactive power; m_p : active power proportional coefficient; m_i : active power integral coefficient; n_p: reactive power proportional coefficient; E^* : voltage amplitude reference; φ^*: voltage phase angle reference.

It is worth noting that to extract fundamental components of active and reactive power, Low Pass Filter (LPF) can be used. After determination of reference phase and amplitude of voltage, sinusoidal waveform generator is used to generate the final waveform based on the references (see Fig. 3).

One of the main drawbacks of droop control is that harmonic current sharing is not taken into consideration in droop control when there is nonlinear load in MG. To accurately share current (including fundamental and harmonic components), using selective resistive-inductive virtual impedance is recommended [23], [25]. For this aim, virtual impedance provides resistive behavior toward harmonic and resistive-inductive behavior toward fundamental components of output current as the following equation:

$$V_{vr} = V_{vr\alpha} + V_{vr\beta}. \tag{3}$$

where

$$V_{vr\alpha} = R_{vr}^{1+} i_{o\alpha}^{1+} - L_{vr}\omega_0 i_{o\beta}^{1+} + \sum_{h=5,7,\ldots} R_{vr}^{h} i_{o\alpha}^{h}. \tag{4}$$

and

$$V_{vr\beta} = R_{vr}^{1+} i_{o\beta}^{1+} + L_{vr}\omega_0 i_{o\alpha}^{1+} + \sum_{h=5,7,\ldots} R_{vr}^{h} i_{o\beta}^{h}. \tag{5}$$

that $R_{vr}^{h,1+}$ might be determined for individual DGs according to their rated power. In the above equations $i_{o\alpha}^{1+}$ and $i_{o\alpha}^{h}$ are fundamental and harmonic components of output current in α-axis while $i_{o\beta}^{1+}$ and $i_{o\beta}^{h}$ are those in β-axis, respectively. It is worth noting that MSOGI-FLL harmonic extraction method [26] is used in this paper to extract fundamental and harmonic components of voltage/current in stationary framework (αβ frame).

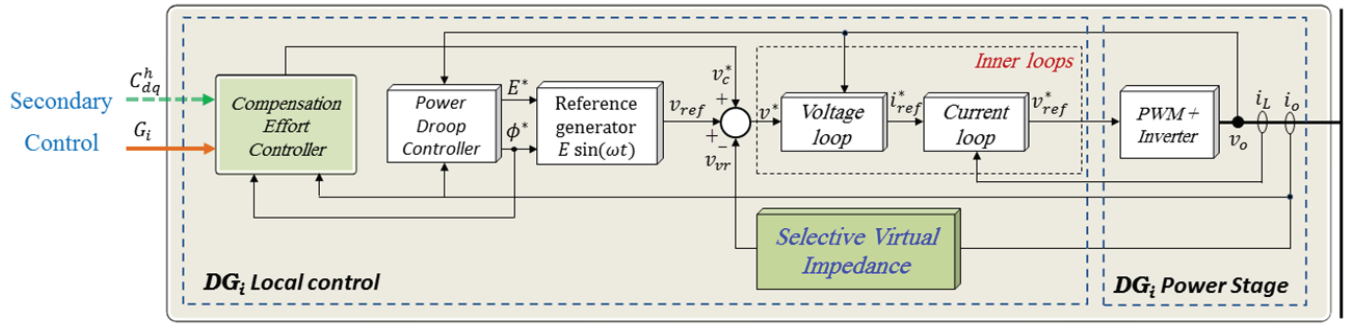


Fig. 3. Block diagram of primary control.

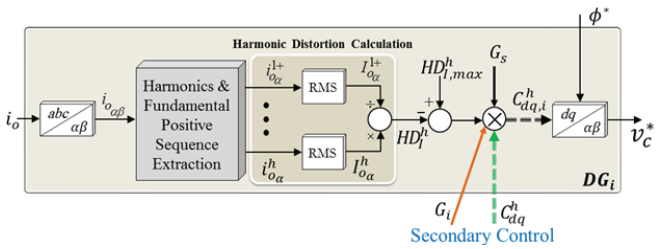


Fig 4. DGs compensation effort controller.

Fig. 4 shows block diagram of DG compensation effort controller. This controller tunes compensation effort of each DG based on its rated power and in accordance with secondary control. Because DG reduces voltage distortion by injecting harmonic current, estimating harmonic distortion of output current (HD_I^h) can be an efficient way to estimate DG effort for compensation. As can be seen in Fig. 4, at first fundamental component and the main harmonics of DG output current are extracted, then h^{th} current harmonic distortion is estimated as [9]:

$$HD_I^h = \frac{I_{rms_{O\alpha}}^h}{I_{rms_{O\alpha}}^{1+}}. \quad (6)$$

where $I_{rms_{O\alpha}}^{1+}$ and $I_{rms_{O\alpha}}^h$ are rms value of fundamental positive sequence and h^{th} harmonic component of output current in α-axis, respectively. Then, HD_I^h is subtracted from its maximum possible value ($HD_{I,max}^h$) to provide a droop characteristic. Noteworthy that $HD_{I,max}^h$ is set to 1 in this paper. It should be noted that higher values can be used for $HD_{I,max}^h$ whereas the droop scheme efficiency is decreased. Therefore, the minimum value of $HD_{I,max}^h$ can make an effective droop scheme while we are sure HD_I^h does not exceed $HD_{I,max}^h$ [21]. Note that a balanced loading is considered in the present paper; thus, β-axis current amplitudes are same as α-axis ones.

The coefficients generated by secondary control (G_i,C_{dq}^h) and DG rated power coefficient (G_s) are applied to produce the final value for compensation effort control of each harmonic that should be carried out by each DG ($C_{dq,i}^h$). These data are transformed to $\alpha\beta$-frame with phase angle deduced by droop controller and sent to voltage/current controllers (v_c^* in Figs. 3 and 4).

The way of determining G_i and C_{dq}^h are explained in the following sections, but G_s can be obtained as [21]:

$$G_s = \frac{S_{0,j}}{\sum_{i=1}^{n} S_{0,i}}. \quad (7)$$

where $S_{0,i}$ is the nominal power of i^{th} DG inverter and n is the number of DGs. It can be deduced from Eq. (7) and Fig. 4 that total compensation is shared between all DGs according to their rated power. As it is represented in Fig. 3, all the signals produced by droop controller (v_{ref}), selective virtual impedance control loop (v_{vr}) and compensation effort controller (v_c^*) are summed up to generate a reference signal for inner control loops (v^*).

Voltage and current controllers (inner controllers) provide proper signals for pulse width modulation (PWM) to generate output voltage of inverters according to the reference values. Proportional-Resonant (PR) controller is used for this purpose. Noteworthy that the design of inner controllers, virtual impedance and droop control is discussed in [21], [24] and [27]. More details concerning primary control can be found in [23]-[25] and [27].

B. Secondary (Central) Control

Secondary control is designed for improving the power quality of SLB and DG(s) terminal, if it is needed. As mentioned before and represented in Fig. 1(b) and Fig. 2, in secondary control, at first SLB compensation is carried out by DGs. SLB compensation by DGs might result severe voltage distortion of DGs terminals or overloading their inverters (as it is shown in Section V). In these situations, APFs cooperate with DGs to partially compensate SLB. The cooperation of DGs and APFs is explained in Section IV but compensation of SLB by DGs is described here.

To compensate SLB by DG, essential data of SLB (that are measured in "Measurement Block") are sent to this level by LBC (Fig. 1(b)). In measurement block, fundamental component and the main harmonics of SLB voltage in dq-frame are extracted by SRF-PLL extraction method [26]. As shown in Fig. 1(b), the data are fed to "DG compensation rate Cal." block of secondary control. Fig. 5 shows this block. Based on Fig. 5, to estimate required compensation of SLB and reduce voltage harmonic distortion to its reference value (HD_h^*), it is necessary calculation of h^{th} harmonic distortion of SLB voltage (HD_h). Like compensation effort controller block (Fig. 4), MSOGI-FLL extraction method is used to extract fundamental and harmonic components and calculateing HD_h. The difference between HD_h and HD_h^* is transferred to a proportional-integrator (PI) controller. The output of PI

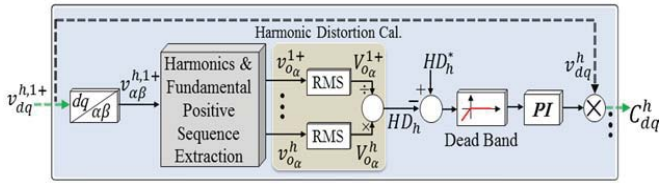


Fig 5. DGs compensation rate calculation.

controller is multiplied by h^{th} harmonic voltage of SLB (v_{dq}^{h}) to generate compensation reference (C_{dq}^{h}), which is sent to local controllers (see Fig. 1(b)). It is worth noting that, by increaseing the proportional coefficient of the PI controller, the controller response time will be reduced but instability probability will raise too. As a result, to tune the PI controller, a tradeoff between response time and stability margin should be considered. The "Dead Band" block in Fig. 5 is used before the PI controller to block secondary control in case compensation of SLB is not required.

III. Active Power Filter Local Control

The structure and local control scheme of the APF used in the present paper is shown in Fig. 6. The general approach for designing this APF is derived from [14]. In Fig. 6, a part of APF control stage is corresponding to the proposed coordinated control that is discussed in the next section.

APF compensates the selected voltage harmonics by providing proper virtual conductance at them. It can be expressed as follows:

$$i_{abc}^{*} = \sum_h G_h^{*} \cdot v_{f_{abc}}^{h}. \tag{8}$$

where h is the order of harmonic and G_h^{*} is the tuned gain that acts as conductance. Note that G_h^{*} might be different for individual harmonics. Each G_h^{*} is multiplied by relative harmonic voltage ($v_{f_{abc}}^{h}$) to compensate corresponding voltage harmonic at the bus of APF installation by injecting proper harmonic current (i_{abc}^{h*}). G_h^{*} is determined automatically based on voltage harmonic distortion rate. Since voltage harmonic distortion is more than its reference value, a PI controller is acting to determine G_h^{*} (Fig. 6). All the individual harmonic currents are summed to determine the total harmonic current that should be injected (i_{abc}^{*}). Note that "Dead Band" block is for blocking APF operation while no compensation of SLB is required. Finally, according to the reference current (i_{abc}^{*}) and voltage/current measured at the place of APF ($v_{f_{abc}}$and $i_{f_{abc}}$), voltage reference of APF ($v_{f_{abc}}^{*}$) is deduced based on the following equation:

$$v_{f_{abc}}^{*} = v_{f_{abc}} - \frac{L_f}{\Delta T}\left(i_{abc}^{*} - i_{f_{abc}}\right). \tag{9}$$

where L_f and ΔT are respectively APF inductor and sampling period. According to Eq. (9), after determination of i_{abc}^{*}, it is subtracted from $i_{f_{abc}}$. Then, based on APF inductor to sampling period ratio ($L_f/\Delta T$) and $v_{f_{abc}}$, required compensation is determined. Noteworthy that a PI controller is used for fixing the dc link of APF (see Fig. 6).

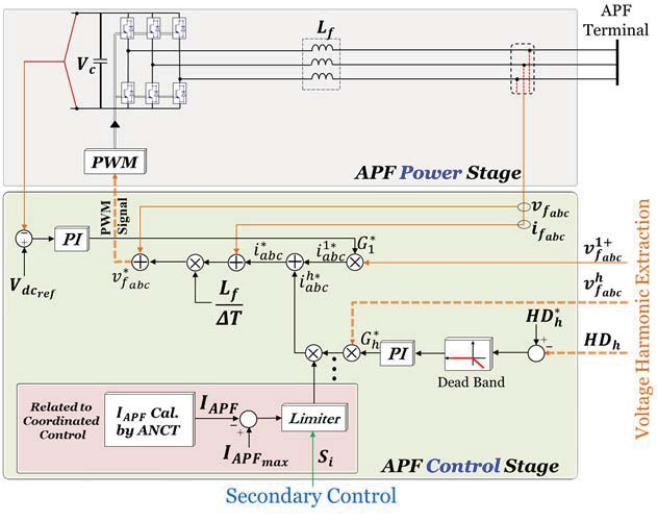


Fig. 6. APF power stage and control structure.

IV. Proposed Coordinated Control of Distributed Generators and Active Power Filters

The cooperation between DGs and APFs is built on four important rules:

1- The priority of SLB compensation is with DG(s) to utilize the available capacity of the interface inverters and to avoid applying dedicated compensation devices as much as possible while the two following rules are taken into consideration. With this rule, not only energy and equipment saving is regarded but also resonant probability is decreased.

2- During compensation of SLB by DGs, DGs output voltage distortion should not exceed from its maximum allowable value. To apply this constraint, voltage THD of DGs terminals is selected as index for evaluating voltage distortion rate and required cooperation rate of APFs.

3- Compensating SLB by DGs should not deal with overloading DGs inverters. In other words, DGs should not tolerate extra efforts for compensation. To apply this constraint, output current of DGs is selected as index.

4- The devolved compensation rate to APFs should be shared between them so that none of them are overloaded. Like DGs rated power constraint, APFs inverters output current is chosen as index for this aim.

In addition, to provide maximum compensation efficiency, APF(s) should be located as near as possible to the sensitive load (nearest electrical proximity) and preferably exactly at SLB [9].

Fig. 7 shows coordinated control process. As it can be seen, the coefficients corresponding to THD and inverter power constraints are shown by G_{di} and G_{pi}, respectively. These values are limited between zero and one. The higher the violation from each constraint is, the lower the corresponding coefficient is. Therefore, $G_{di\&pi} = 1$ represents no violation and *vice versa*. These two values are multiplied to determine a G_i which affects the compensation effort of i^{th} DG (note that $0 < G_i < 1$). Each G_i calculated in constraints block of each DG is sent to APFs cooperation rate calculation block of secondary control by LBC (see Figs. 7&1(b)). Then, these values are summed up and divided by n (number of DGs) to

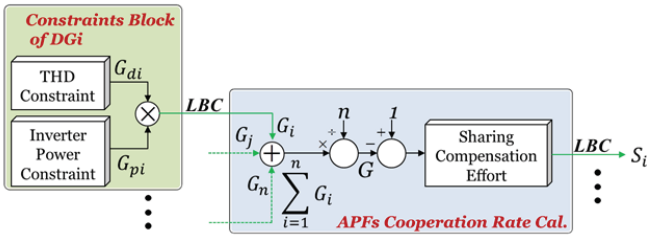


Fig. 7. Block diagram of coordination process.

generate a number between zero and one (G). In the case of complete compensation of SLB harmonics by DGs, G will be equal to one. In other words, G determines the duty of all inverters for compensation considering both constraints and $1-G$ is the compensation amount that should be carried out by APFs. It is obvious that in the case of having more than one APF, this compensation rate should be shared among APFs according to the rated power of them. On the other hand, if the compensation rate devolved to APF_i (S_i) is exceeded from the rated power of the APF, a limiter limits the cooperation of the APF by controlling S_i (see Fig. 6). As it can be seen in Fig. 6, APFs rated power is determined according to injected current magnitude. S_i is applied through multiplying by G_h^*.

Fig. 8 shows THD constraint block. Based on this figure, at first, THD of DG output voltage is measured according to Eq. (10) [9]:

$$THD = \frac{1}{V_1}\sqrt{\sum_{h=2}^{\infty} V_h^2} = \frac{1}{V_1}\sqrt{\tilde{V}_d{}^2 + \tilde{V}_q{}^2}. \quad (10)$$

where $\tilde{V}_d$ and $\tilde{V}_q$ are oscillatory components of voltage in d and q-axis in dc framework and V_1 is rms value of fundamental component of phase voltage. Then, it is compared with its maximum allowable value; if the measured value exceeds the maximum value, an integrator controller tries to reduce THD of output voltage by reducing DG compensation effort through decreasing G_d. Note that the initial condition of the integrator controller is set to 1. The integral coefficient of the integrator controller should be tuned so that the controller response is not very long and the system is able to tolerate the overshoot produced by fast response.

The coefficient corresponding to interface inverter nominal power constraint is dependent on the inverter output current amplitude which can be deduced by the following equations [28]:

$$i_o = I_1 \sin(\omega t + \theta_1) + \sum_{h=2}^{\infty} I_h \sin(h\omega t + \theta_h) = i_1(t) + i_h(t) \quad (11)$$

where $i_1(t)$ and $i_h(t)$ are fundamental and harmonic components of current, respectively. A simple and well-known method to extract the fundamental component is SRF-PLL extraction method. Then the harmonic component can be calculated by subtracting i_o from the determined fundamental component and using LPF [28]. Therefore, the amplitude of output current can be calculated as the following equation (see Fig. 9):

$$|i_o| = \sqrt{i_1{}^2 + i_h{}^2}. \quad (12)$$

It is worth noting that to measure APF output current, the above equation cannot be used since APF output current

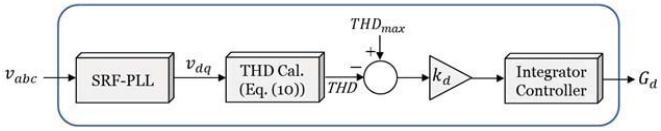


Fig. 8. Block diagram of THD constraint.

just includes harmonic components and fundamental component is not injected to MG by APF. To measure APF output current, Adaptive Noise Canceling Technology (ANCT) signal processing method [29] is used. Applying this method to the present work, APF injected harmonic current can be obtained by measuring output harmonic current reduction of DG since APF is applied.

Fig. 9 illustrates DG inverter nominal power constraint. As mentioned before, DGs inverters should not be overloaded and APFs are used for this aim. However, APFs cooperation just results harmonic current mitigation of DGs and fundamental component of DGs output current cannot be reduced by the cooperation. As a result, this point should be considered in the coordinated control that whether DGs are overloaded due to high amount of linear and/or nonlinear loads. "Comparator Block" of Fig. 9 is contrived for this point. In this block, the maximum value of output inverter current is compared with fundamental component of output current; if the fundamental component is higher than the maximum value, the fundamental component is as reference of the I-controller. It can be seen in Fig. 9 that the same strategy is used for determining THD and interface inverter nominal power constraints coefficients.

V. Simulation Results

Fig. 10 shows the three-phase test system considered for simulation. This islanded MG consists of three DGs, two APFs, a linear load and a nonlinear load (a three-phase diode rectifier) that are connected to SLB. As shown in Fig. 10, APF2 is located in an electrical distance from APF1 and SLB while APF1 is directly connected to SLB. Simulation is performed using *MATLAB/Simulink*. Nominal voltage and frequency of MG are 230 V (per-phase rms value) and 50 Hz, respectively. Switching frequency of DGs and APF inverters is 10 kHz. It is worth noting that THD_{max} is set to 5% according to IEEE Standard 519 [30]. Voltage compensation is done for 5th and 7th harmonics (main orders) of SLB voltage with the reference values of $HD_5^* = HD_7^* = 1\%$. The test system parameters are listed in Table I. Table II shows the coordinated control data. Note that the rated power of DG1 inverter is considered to be twice of that of DG2 and one and a half times of DG3 (and this fact is reflected in maximum current values). Furthermore, APF1 rated power is twice of APF2. Other parameters of primary and secondary control can be found in [21]. To evaluate the proposed control scheme, simulation process is divided into four steps:

- First Step ($0<t<2$s)
  Virtual impedance loops for fundamental component are active.
- Second Step ($2<t<4$s)

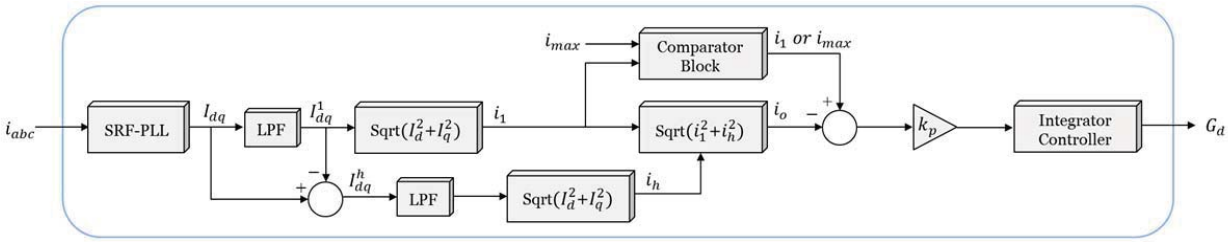


Fig. 9. Block diagram of inverter nominal power constraint.

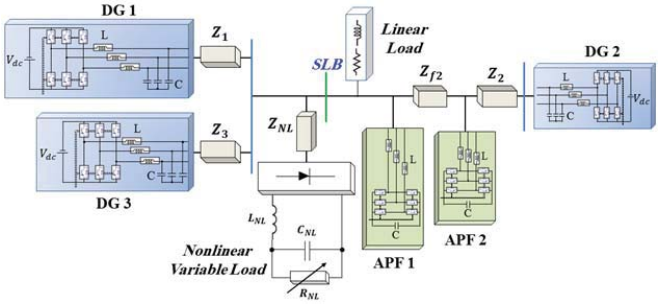


Fig. 10. Test system.

TABLE I
TEST SYSTEM PARAMETERS

Distribution lines							
$Z_1(\Omega)$		$Z_2(\Omega)$		$Z_3(\Omega)$	$Z_{NL}(\Omega)$	$Z_{f2}(\Omega)$	
0.2+j1.131		0.1+j0.565		0.15+j0.848	0.2+j1.005	0.05+j0.226	
Nonlinear load				Linear load	APFs power stage		
C_{NL} (μF)	$R_{NL}(\Omega)$	L_{NL}(mH)		$Z_L(\Omega)$	L_{f1}(mH)	C_1(μF)	L_{f2}(mH)	C_2(μF)
235	20-80	0.084		125+j6.283	17	2000	12	1500

TABLE II
CONTROL PARAMETERS

APFs			
Capacitor PI controller		Sampling period (s)	
K_p	K_i	1.25×10^{-4}	
0.5	0.05		
PI controllers			
5th harmonic		7th harmonic	
K_p	K_i	K_p	K_i
18	250	8	100
Constraints (integral controller)			
Nominal power constraint		THD constraint	
K_p		K_d	
3		0.5	
Maximum of inverters current amplitude in dq frame (A)			
DG_1	DG_2	DG_3	
18	9	13.5	

Selective harmonic virtual impedances are added to the previous step; so primary control is completely active.

- Third Step (4<*t*<7s)
  Secondary control is initiated with voltage compensation of SLB by using the interface inverters.
- Fourth Step (7<*t*<10s)
  APFs are added to secondary control and cooperation between interface inverters and APFs to compensate SLB voltage is established.
- Fifth Step (10<*t*<13s)
  In this step, nonlinear load is reduced so voltage distortion of SLB is mitigated and APFs are switched off.

Note that droop and voltage/current controllers are active in all steps.

To examine coordination process in different conditions of system, two scenarios are considered and the above five steps are involved in the first scenario while in the second scenario the first four steps are included:

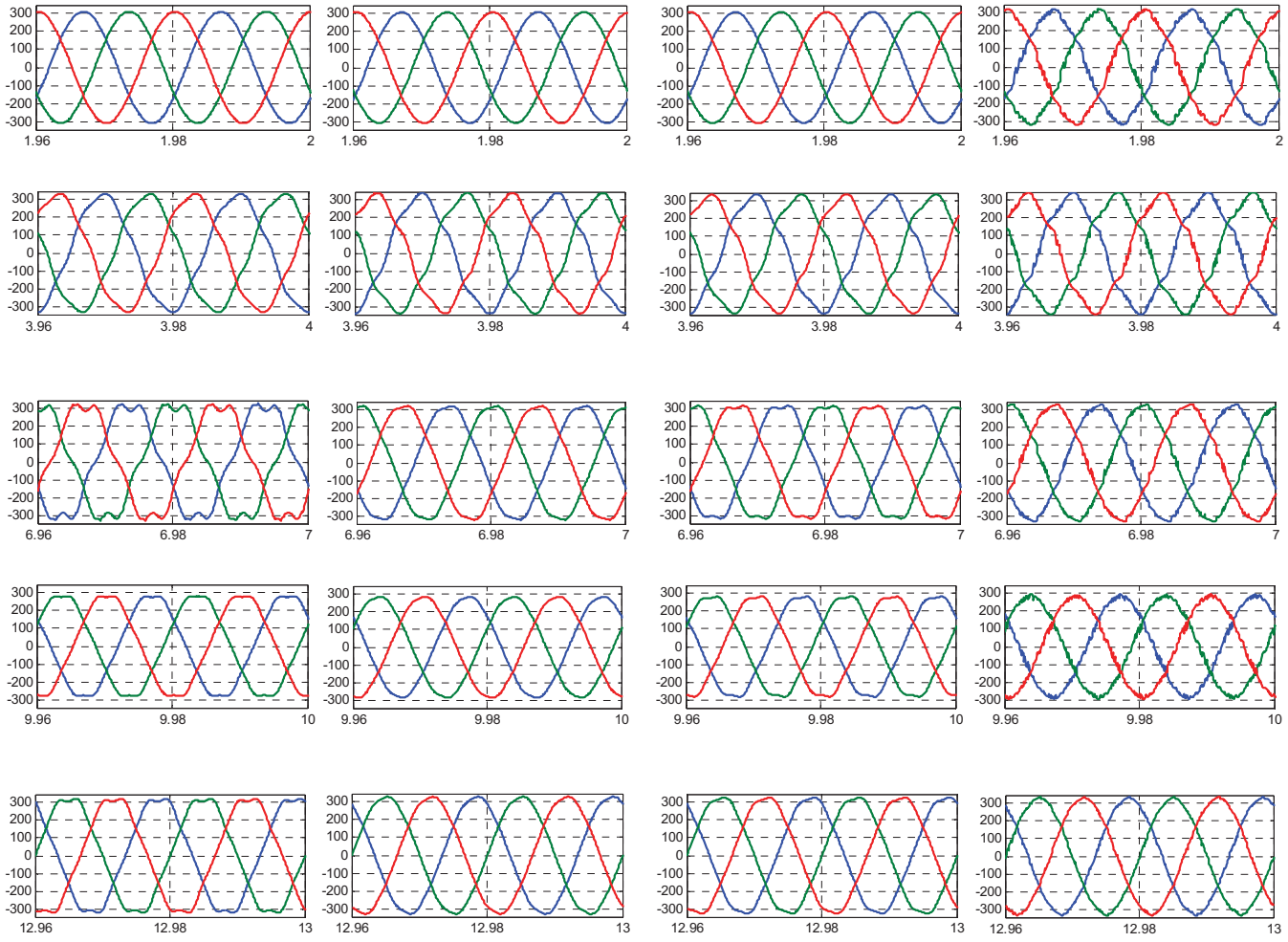
- Scenario 1
  Violation of interface inverter nominal power of DG1 and DG2 and violation of THD constraint in DG1 and DG3 until step four and no violation in step five.
- Scenario 2
  For the sake of simplicity and to avoid excessive paper length, in this scenario, DG3 and APF2 are removed and the case with violation of both constraints for two remaining DGs inverters is studied.

It is worth noting that the parameters of primary, secondary and coordinated controls are the same in both scenarios.

A. Scenario one

Fig. 11 shows output voltage of DGs and SLB voltage in all five steps. To compare voltage waveforms in different steps, this figure shows two last cycles of each step for DGs and SLB. It can be observed that output voltages of DGs are distortion-free in the first step demonstrating the good performance of droop controllers, virtual impedance and voltage/current control loops. However, voltage of SLB is distorted due to the line impedances. Since selective virtual impedance loop is added to the primary control in the second step, harmonic current sharing is improved (Fig. 12) in price of increased voltage distortion at DGs buses and SLB. In the third step, secondary control initiates and it can be seen that SLB voltage is improved, significantly; but output voltage of DG1 is made distorted, severely and DG3 output voltage is not satisfactory. In step four, the coordinated control is initiated and APFs undertake a part of compensation; thus, output voltage of all DGs are improved. Consequently, due to voltage harmonic reduction of SLB (by changing resistive branch of nonlinear load from 20 to 80 Ω), DGs efforts for compensating SLB is reduced. As a result, no violation is occurred in this step (see Fig. 14) so cooperation of APF is not required and APF is switched off while voltage waveform of DGs terminal are not very distorted.

For instance, Fig. 12 shows rms value of 5th current harmonic of DGs in α-axis. As shown in Fig. 12, output harmonic current of DG2 is more severe in the first step whereas this DG is smaller than others. In the second step, harmonic current of DG2 is decreased while that of DG1 is increased. Thus, considering the DGs rating (Table II), sharing harmonic current between DGs is improved. It can be seen in the third step that harmonic current of each unit is dependent on the unit cooperation rate in compensation. According to equations (6) and (7), this rate is set based on the DG rating



(a) (b) (c) (d)

Vertical axis: voltage(V), Horizontal axis: time(s)

Fig. 11. Voltage waveforms (Scenario 1): (a) DG1, (b) DG2, (c) DG3, (d) SLB.

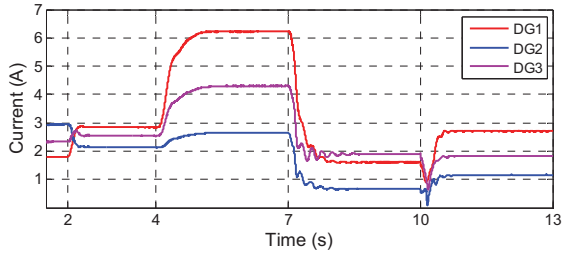


Fig. 12. RMS of 5th current harmonic (Scenario 1).

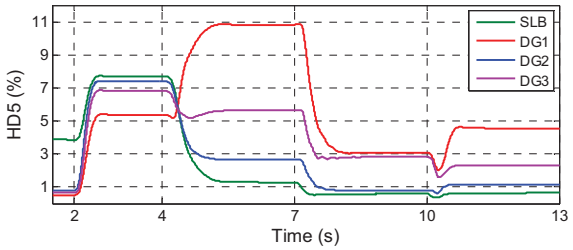


Fig. 13. 5th Voltage harmonic distortion (Scenario 1).

considering a droop characteristic. In step four, harmonic current in all DGs is generally reduced due to undertaking a part of compensation by APFs. It should be mentioned that in this step, selective virtual impedance is still active, but harmonic current sharing is not maintained as good as previous step. Note that another equipment (APFs) is added in step four which is not included in harmonic current sharing between DGs local controls. In other words, sharing of harmonic current between inverters is done using selective virtual impedance, but this sharing between inverters and APFs is happened based on compensation rates of APFs (S_i). Finally, in step five harmonic current in three DGs are still low whereas APFs are switched off. It is for reduction of voltage harmonic distortion in this step. It can be seen in step four of Fig. 12 that harmonic current sharing is achieved again because APFs are switched off in this step. Note that 7th harmonic has the same behavior of 5th harmonic but the relative figure is not included to avoid excessive paper length.

Fig. 13 illustrates the percentage of 5th voltage harmonic distortion at DGs buses and SLB. According to this figure, in the first step, voltage harmonic distortions of DGs are very small, but this parameter is relatively high in SLB due to voltage drop on line impedances. The percentage of voltage harmonic distortion of all buses is increased in the second step

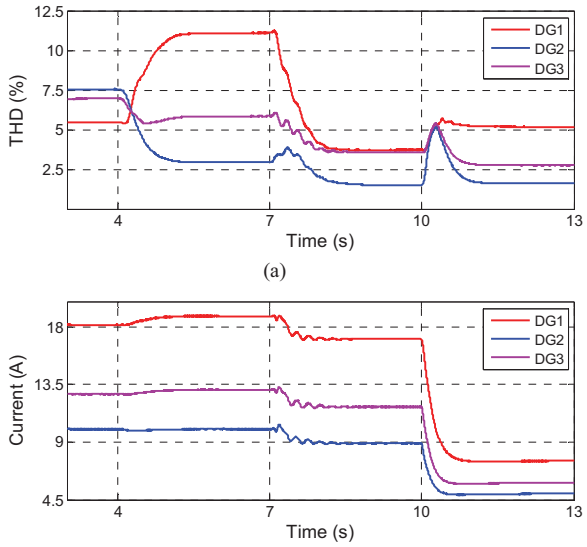


Fig. 14. Constraint-related curves (Scenario 1): (a) THD of voltage, (b) nominal power (current amplitude in dq frame).

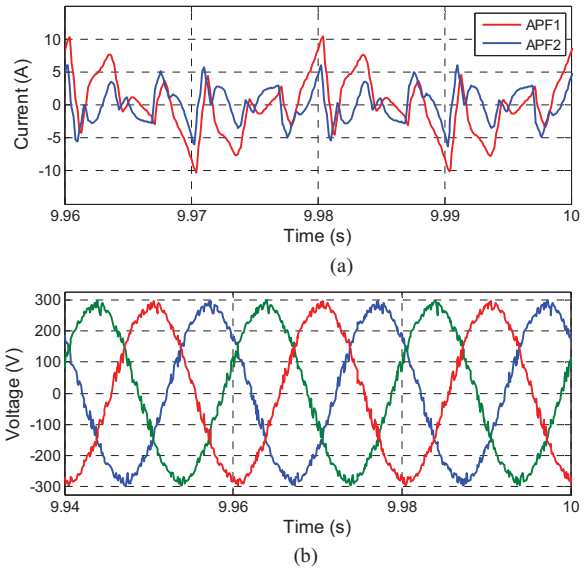


Fig. 15. APFs output voltage and current (Scenario 1): (a) APFs single phase of current, (b) APF2 three phase voltage.

since selective virtual impedance causes voltage harmonic increase to share harmonic current.

In the third step, it is shown that voltage harmonic distortion of DG1 is increased significantly while this parameter is decreased for DG2 and DG3. However, voltage harmonic distortion of SLB is mitigated to the reference value in this step. Note that due to relatively low impedance between DG2 terminal and SLB in this scenario, the voltage behavior is similar in these two buses. In step four, APFs help DGs to compensate SLB harmonics and consequently, voltage distortion of DG1 is reduced, significantly while SLB distortion is maintained at the reference value. It shows the good performance of APFs in undertaking a part of compensation instead of inverters. As it is shown in Fig. 13, voltage harmonic distortion of all buses is low in step five even when APFs are disconnected.

The curves related to constraints are depicted in Fig. 14 and show that violation of THD constraint of DGs output voltage is occurred for DG1 and DG3 while violation of inverters nominal power is taken place for DG1 and DG2 inverters in the third step. However, both violations are removed in step four by APF participation in compensation. In step five it is shown that output current of DGs are decreased because the nonlinear load is decreased, as a result, DGs effort for compensating SLB is reduced. Note that in this step, in order to existing no violation, DGs compensate SLB completely and APFs are switched off because they are not needed.

Finally, Fig. 15 shows single phase output current of APFs and three-phase output voltage of APF2 in step four that APFs are active. As mentioned before, APF1 rated power is twice of APF2 so APF1 compensation effort is twice of APF2. It can be seen in Fig. 15(a) that harmonic current injection of APF1 is almost twice of that of APF2. Note that APFs current generally includes three components: fundamental component that APFs consume for fixing their dc links and 5^{th} and 7^{th} harmonic components which are injected to SLB for compensation.

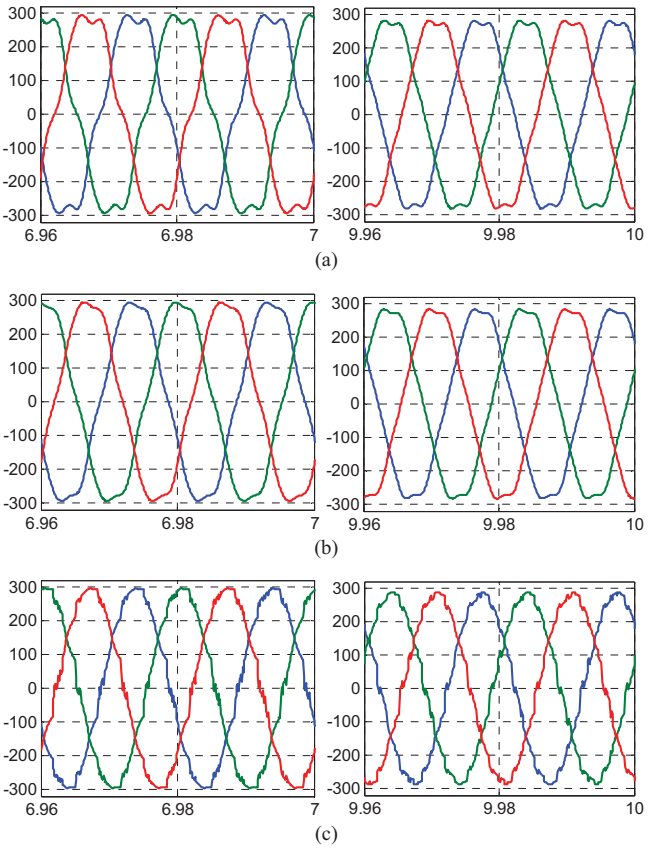


Fig. 16. Voltage waveform (Scenario 2): (a) DG_1, (b) DG_2, (c) SLB.

B. *Scenario two*

To provide necessary conditions to reach this scenario, the resistive branch of linear load is doubled, the resistive branch of nonlinear load is set to 30 Ω and Z_2 impedance is quadrupled. Note that in the figures and explanations presented below, it is tried to avoid repeating the

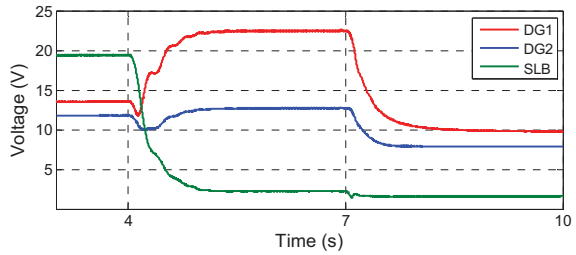
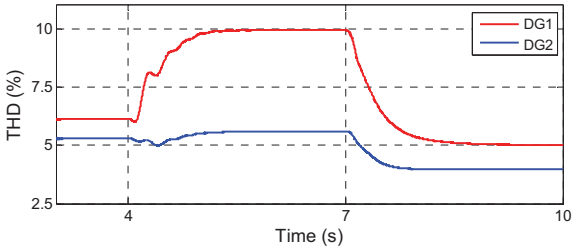
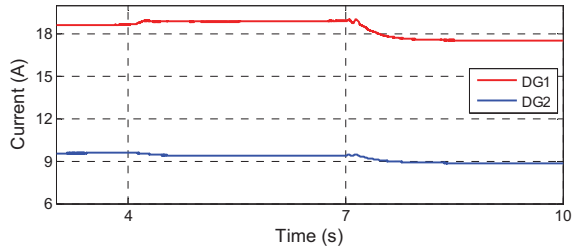


Fig. 17. RMS of 5th voltage harmonics (Scenario 2).



(a)



(b)

Fig. 18. Constraint-related curves (Scenario 2): (a) THD of voltage, (b) nominal power (current amplitude in dq frame).

aforementioned points.

Fig. 16 depicts two last cycles of DGs and SLB voltage in third and fourth steps in which compensation of SLB occurs without and with APF1, respectively. It is shown that output voltage of both DGs are distorted in step three, but the voltage of SLB is acceptable due to compensation by DGs. In step four, distortion of DGs output voltage is reduced because of participation of APF1 in compensation. Moreover, the voltage distortion of SLB is remained approximately unchanged in this step.

Fig. 17 shows rms of 5th voltage harmonic of DGs and SLB in steps three and four. It is shown that in step four, DGs voltage harmonics are mitigated and SLB voltage distortion is remained unchanged.

Fig. 18 shows constraint-related curves in the second scenario. It can be observed that violation from THD of voltage in both DG buses is abated in step four. Furthermore, output current of both DGs is decreased in this step due to lower compensation effort.

VI. Conclusion

This paper has proposed a hierarchical two-level control scheme to enhance power quality in main buses of an islanded microgrid. Primary level includes droop controller, voltage and current loops and selective virtual impedance. Secondary control manages the compensation of SLB voltage harmonics by coordinated control of DGs inverters and active power filter. During compensation by the DGs, if THD value at any of DG buses exceeds the maximum value and/or any of interface inverters has to tolerate overload, APF cooperates in compensation in coordination with interface inverters. To evaluate the effectiveness of coordinated control, two simulation scenarios are defined. Simulation results show that by using the proposed hierarchical scheme, acceptable power quality is provided simultaneously at SLB and DGs buses of microgrid in both scenarios.

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