

## **Mitigation of Harmonics in Grid-Connected and Islanded Microgrids via Virtual Admittances and Impedances**

Micallef, Alexander; Apap, Maurice; Spiteri-Staines, Cyril; Guerrero, Josep M.

*Published in:*  
I E E E Transactions on Smart Grid

*DOI (link to publication from Publisher):*  
[10.1109/TSG.2015.2497409](https://doi.org/10.1109/TSG.2015.2497409)

*Publication date:*  
2017

*Document Version*  
Early version, also known as pre-print

[Link to publication from Aalborg University](#)

*Citation for published version (APA):*  
Micallef, A., Apap, M., Spiteri-Staines, C., & Guerrero, J. M. (2017). Mitigation of Harmonics in Grid-Connected and Islanded Microgrids via Virtual Admittances and Impedances. *I E E E Transactions on Smart Grid*, 8(2), 651 - 661 . <https://doi.org/10.1109/TSG.2015.2497409>

### **General rights**

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal -

### **Take down policy**

If you believe that this document breaches copyright please contact us at [vbn@aub.aau.dk](mailto:vbn@aub.aau.dk) providing details, and we will remove access to the work immediately and investigate your claim.



# Mitigation of Harmonics in Grid-Connected and Islanded Microgrids via Virtual Admittances and Impedances

Alexander Micallef, *Graduate Student Member, IEEE*, Maurice Apap, *Member, IEEE*, Cyril Spiteri-Staines, *Member, IEEE* and Josep M. Guerrero, *Fellow, IEEE*

**Abstract**—Optimization of the islanded and grid-connected operation of microgrids is important to achieve a high degree of reliability. In this paper, the authors consider the effect of current harmonics in single phase microgrids during both modes of operation. A detailed analysis of the effect of the output impedance of the considered primary control loops on the harmonic output of the considered voltage source inverters (VSIs) is initially carried out. A virtual admittance loop is proposed to attenuate the current harmonic output in grid-connected operation that is generated due to the grid voltage distortion present at the point of common coupling (PCC) and due to local non-linear loads. The paper also considers the harmonic current sharing and resulting voltage harmonics at the PCC during islanded operation of the microgrid. A capacitive virtual impedance loop was implemented to improve the harmonic current sharing and attenuate the voltage harmonics at the PCC. Experimental results are given to validate the operation of the proposed algorithms.

**Index Terms**—Microgrids, Current Harmonics, Harmonic Compensation, Droop Control, Virtual Impedance, Virtual Admittance.

## NOMENCLATURE

PCC	Point of common coupling.
VSIs	Voltage source inverters.
THD	Total harmonic distortion.
PR	Proportional-resonant.
VC-VSIs	Voltage controlled-voltage source inverters.
$T_1, T_2$	Isolation transformers.
S1, S3	Output contactors.
Sg	Static switch.
$G_p(s), G_q(s)$	P - $\theta$ and Q - E droop controllers respectively.
$m, n_i$	Integral gains of the P - $\theta$ and Q - E droops respectively.
$m_d, n$	Proportional gains of the P - $\omega$ and Q - E droops respectively.
$n_d$	Derivative gain of the Q - E droop.
$P^*$	Active power reference (grid-connected operation).
$Q^*$	Reactive power reference (grid-connected operation).

$V_C(s)$	Voltage across the capacitor of the LC filters.
$i_{o1}(s), i_{o2}(s)$	Current injected by the respective inverter into the PCC.
$R_1$	Inverter side choke resistance.
$L_1$	Inverter side choke inductance.
$R$	Damping resistance of the output filter.
$G_V(s), G_I(s)$	Voltage and current controllers respectively.
CLTF	Closed loop transfer function.
$R_v$	Virtual output resistance.
$Z_d(s)$	Capacitive virtual impedance transfer function.
$k_{ph}$	Proportional gains of $Z_d(s)$ at each considered harmonic.
$k_{ih}$	Integral gains of $Z_d(s)$ at each considered harmonic.
$Z_L(s)$	Impedance of the inverter side inductor $L_1$ .
$V_{THD}$	Voltage THD.
TDD	Total demand distortion.

## I. INTRODUCTION

INVERTERS connected to a microgrid must support both grid-connected and islanded operation through their primary control loops. The droop control algorithm enables operation in both modes but has some well known power quality performance limitations due to any harmonic current flows. The presence of the grid greatly affects the harmonic current flows in the microgrid network, since the characteristics of stiff grids (e.g.: voltage, frequency) are not affected by power quality disturbances such as harmonics. There is a harmonic current sharing problem during islanded operation, due to the harmonic demand from local non-linear loads. In addition, these harmonic currents also induce voltage harmonic distortion at the point of common coupling (PCC). During grid-connected operation, the voltage source inverters (VSIs) are required to output sinusoidal voltage and current into the grid. However, the VSIs can inject additional harmonic currents into the grid either due to the presence of voltage harmonics at the PCC and local non-linear loads. The injected harmonic currents increase the power losses and may cause stability problems in the local network.

Harmonic current sharing and voltage harmonic distortion are the main power quality concerns during islanded operation of the microgrid. Due to the droop control loops, the harmonic

A. Micallef, M. Apap and C. Spiteri-Staines are with the Department of Industrial Electrical Power Conversion, University of Malta, Malta. MSD 2080. E-mail: alexander.micallef@um.edu.mt

J. M. Guerrero is with the Department of Energy Technology, Aalborg University, Denmark. E-mail: joz@et.aau.dk

current sharing depends on the output impedance of the inverters and the line impedances. The harmonic currents also induce voltage harmonic distortion at the PCC due to current requirements from local non-linear loads [1]. These voltage harmonics may cause stability issues due to resonances present on the microgrid [2] and thus harmonic damping techniques must be considered. The harmonic currents increase due to improper harmonic current sharing, which results in higher voltage distortion at the PCC.

Harmonic current injection into the grid is one of the main concerns during grid-connected inverters, since these harmonic currents increase the power losses and may cause stability problems in the local network. The grid interconnection standards [3], [4] address the harmonic current injection problem and specify individual harmonic limits. In addition, these standards also specify that the total harmonic current distortion (THD) of the current injected into the grid should be less than 5% with the inverter at the rated output power and at ideal grid conditions. It is well known that grid voltage distortion present at the PCC of the inverters increases their current harmonic output.

Traditional techniques for harmonic mitigation involve installing series passive or active filters which can however compromise the stability of the microgrid during islanded operation. Additional shunt passive or active filters can be introduced into the microgrid and were considered by several authors [5]–[7]. However these result in an expensive solution since these do not give any additional contribution to the operation of the microgrid. Selective harmonic compensation techniques can also be applied to improve the harmonic current sharing and mitigate the voltage distortion due to harmonic currents in islanded microgrids. A harmonic conductance-harmonic VAr droop was proposed in [2], [8] while a capacitive virtual impedance loop was proposed by the authors in [1], [9] to achieve these aims. Savaghebi et al. in [10] add a secondary control loop in addition to inner proportional-resonant (PR) controllers with the aim to provide additional selective harmonic compensation. However, the communications have severe limitations when determining the correct phase angle for the injected harmonic current and when synchronizing the harmonic output current.

Selective harmonic compensation algorithms implemented in the microgrid inverters can also be applied to grid-connected microgrids. Algorithms available in literature can be grouped in two major categories; repetitive harmonic controllers [11]–[13] and linear harmonic compensators [5], [14], [15]. Repetitive harmonic controllers improve the THD of the output current at the cost of complex design and implementation of the controllers. On the other hand, linear harmonic compensators can be simply implemented in the form of second order generalized integrators (SOGIs) [5], [14]. The linear harmonic compensators are then tuned such that their center frequency is at odd multiples of the fundamental which reduces the closed loop impedance of the inverters at these harmonic frequencies. This reduction in the output impedance reduces the voltage harmonics present at the PCC of the inverters. This minimizes the injected harmonic current since the inverters supply only the harmonic current required by the loads. Grid

voltage harmonic compensation can be also achieved through feed-forward compensation [16]–[18]. Abeyasekera et al. in [16] consider using an optimized feed-forward disturbance rejection while Wang et al. in [17] consider using a PD feedforward scheme. In [18], Li et al. use a full feed forward scheme to reduce the injected harmonic current in real grid scenarios. However, although the performance of feed-forward techniques achieves a good level of performance, the main drawback is that for complex controllers, such as the cascaded PR controllers with harmonic compensation, the resulting feed-forward transfer function becomes impractical due to its high order and complexity.

In this paper, two distinct control loops are being proposed to target the effect of current harmonics in grid-connected and islanded operation. A generalized capacitive virtual impedance loop was implemented to improve the harmonic current sharing between the inverters in the microgrid while at the same time selectively dampening the voltage harmonics at the PCC in islanded operation. The capacitive virtual impedance achieves its aims by monitoring the output current of the inverter and generates a voltage vector which is then applied to the input of the voltage control loop. Virtual impedances have been used in literature to improve the power sharing between inverters [19]–[23] and for selective voltage harmonic compensation of voltage controlled-VSIs (VC-VSIs) [1], [9] during islanded operation. In addition, a virtual admittance loop is being proposed which provides selective attenuation of the output current harmonics of the single phase VC-VSIs during grid-connected operation. The virtual admittance achieves its aims by monitoring the output voltage of the inverter and generates a current vector which is then applied to the input of the current control loop. Virtual impedances for selective current harmonic compensation have been applied for grid-connected current source rectifiers [24] but to the authors' knowledge, such compensation techniques are not yet documented for grid-connected VC-VSIs in a microgrid.

The rest of the paper is organized as follows. In Section II, a description of the microgrid experimental setup for operation into grid-connected and islanded mode is given, including the inner and outer control loops of the VC-VSIs. Section III contains a detailed analysis of the output impedance of the microgrid VC-VSIs. A description of the capacitive virtual impedance loop which provides additional insight to the harmonic current sharing achieved when using such a primary control loop is given in section IV. The proposed virtual admittance loop for grid-connected harmonic compensation is described in section V. A summary of the obtained experimental results is given in Section VI that show the suitability of the proposed algorithms in achieving their respective aims.

## II. SINGLE-PHASE MICROGRID SETUP FOR ISLANDED AND GRID-CONNECTED OPERATION

The single phase microgrid proposed in this paper considers the case where a group of neighboring households in a residential area, are connected together to form a microgrid. Each household has local energy generation and any energy source can be used with the microgrid inverters. The energy sources

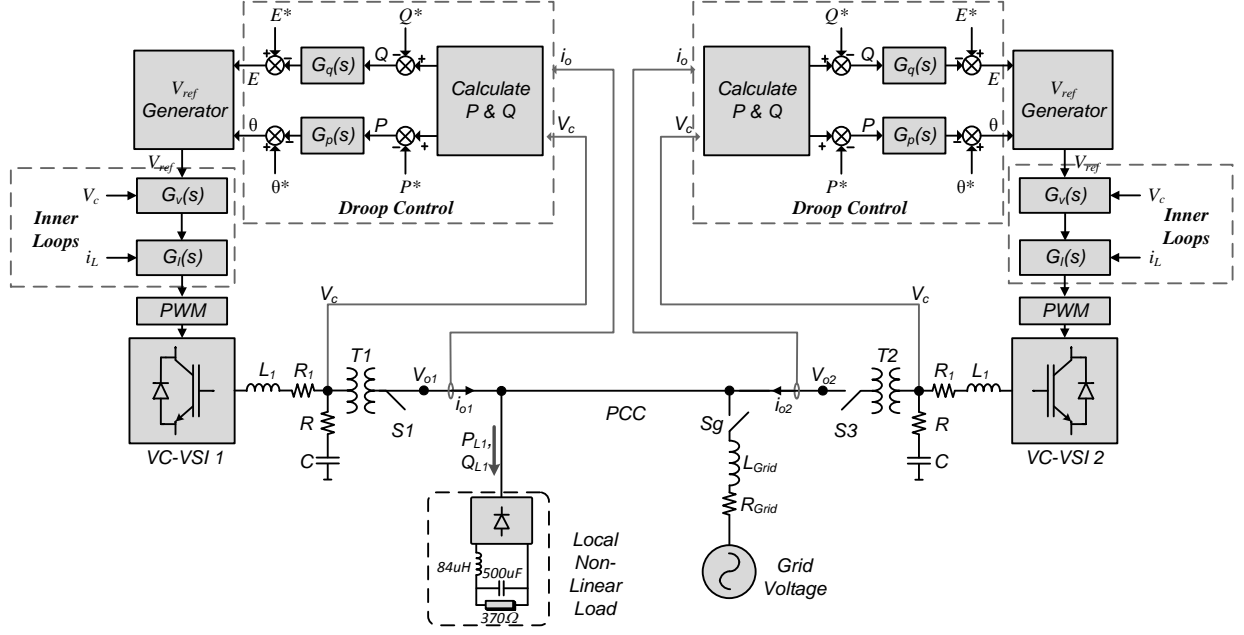


Fig. 1. Block diagram of the single phase microgrid setup for islanded and grid-connected operation.

are replaced by a DC power supply since the interactions due to the intermittency of the renewable energy sources are not relevant to the algorithms proposed in this paper. The block diagram of the considered experimental setup is shown in Fig. 1. A VC-VSI topology was considered for the two microgrid inverters, which only use local voltage and current measurements. The inverters are interfaced to the PCC via LC filters with additional 1:1 isolation transformers  $T_1$  and  $T_2$ . A local non-linear load is connected to the PCC, consisting of a single phase rectifier with smoothing capacitor. Switches  $S_1$  and  $S_3$  allow the VC-VSIs to synchronize to the PCC voltage prior to their connection while switch  $S_g$  acts as a static switch.

#### A. Outer Droop Control Loop

The microgrid VC-VSIs employ droop control to regulate the active and reactive power outputs in both modes of operation. The active power output is controlled by using a (P -  $\omega$ ) droop while the reactive power output is controlled by using a (Q - E) droop. The inputs to the droop controller are the active and reactive power measurements determined from the capacitor voltage  $V_C(s)$  and the current output by the respective inverter  $i_{ox}(s)$  as shown in Fig. 1. The droop control algorithm can be mathematically expressed by:

$$\begin{aligned} \theta &= \theta^* - G_p(s)(P - P^*) \\ &= \theta^* - (m_d + \frac{m}{s})(P - P^*) \end{aligned} \quad (1)$$

$$\begin{aligned} E &= E^* - G_q(s)(Q - Q^*) \\ &= E^* - (n_d + n + \frac{n_i}{s})(Q - Q^*) \end{aligned} \quad (2)$$

where  $\theta^* = \omega^*/s$  is the reference phase angle;  $G_p(s)$  and  $G_q(s)$  are the droop controllers of the active and reactive power respectively; and  $P^*$  and  $Q^*$  are the active and reactive

powers references respectively. The design procedure for the droop controller implemented in this paper was already described in detail in [1], [9]. The droop gains that were used for the results given in this paper are:  $m = 0.03 \text{ rad/W.s}$ ,  $m_d = 0.002 \text{ rad/W.s}^2$ ,  $n = 0.06 \text{ V/VAr}$ ,  $n_i = 0.12 \text{ V.s/VAr}$  and  $n_d = 0.005 \text{ V/VAr.s}$ .

#### B. Inner Control Loops

The inner control loops consist of a voltage loop and an inner current loop which are both regulated by Proportional-Resonant (PR) controllers with selective harmonic control as shown in the block diagram in Fig. 2. The voltage loop regulates the voltage  $V_C(s)$  across the capacitor of the output LC filter while the inner current loop regulates the current  $i_{Lx}(s)$  through the respective inverter side inductor  $L_1$ . The transfer functions of the voltage and current controllers are [1], [9]:

$$G_V(s) = K_{pV} + \sum_{h=1,3,5,7} \frac{k_{1Vh}s}{s^2 + \omega_{cVh}s + \omega_h^2} \quad (3)$$

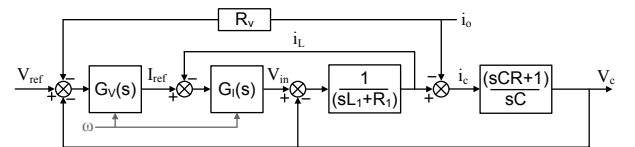


Fig. 2. Block diagram of the inner control loops of both inverters.  $L_1$  is the inverter side inductance,  $C$  is the filter capacitance,  $R_1$  is the inverter side choke resistance and  $R$  is the damping resistance,  $V_{ref}$  is the voltage reference obtained from the droop control loop,  $i_L$  is the current through  $L_1$ ,  $i_{ox}$  is the current output by the respective inverter  $x$  and  $R_v$  is the virtual resistance.

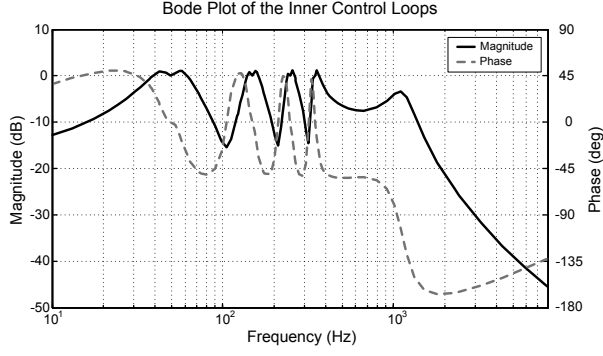


Fig. 3. Bode plot of the transfer function  $\frac{V_C(s)}{V_{ref}(s)}$  ignoring the effect of the virtual output resistance  $R_v$  for the following output filter parameters:  $L_1 = 1\text{mH}$ ,  $R_1 = 0.065\Omega$ ,  $R = 1\Omega$  and  $C = 25\mu\text{F}$ .

$$G_I(s) = K_{pI} + \sum_{h=1,3,5,7} \frac{k_{iIh}s}{s^2 + \omega_{cIh}s + \omega_h^2} \quad (4)$$

where  $K_{pV}$  and  $K_{pI}$  are the proportional gains,  $k_{iVh}$  and  $k_{iIh}$  are the resonant gains at the harmonic frequency,  $\omega_{cVh}$  and  $\omega_{cIh}$  determine the bandwidth at each harmonic frequency and  $\omega_h$  is the resonant frequency where  $\omega_h = h\omega$ . The PR controllers adapt to the varying droop frequency since the frequency of the microgrid voltage varies due to the droop control. The closed loop transfer function (CLTF) of the inner loops can be obtained by applying the block diagram reduction technique on the block diagram of Fig. 2. At this stage, consider that the virtual output resistance  $R_v = 0\Omega$ , therefore the CLTF can be expressed by:

$$V_C(s) = \frac{G_I(s)G_V(s)Z_C(s)}{Z_C(s) + Z_L(s) + G_I(s) + G_I(s)G_V(s)Z_C(s)} V_{ref}(s) - \frac{Z_C(s)(Z_L(s) + G_I(s))}{Z_C(s) + Z_L(s) + G_I(s) + G_I(s)G_V(s)Z_C(s)} i_o(s) \quad (5)$$

where  $Z_L(s) = sL_1 + R_1$  and  $Z_C(s) = (sCR + 1)/sC$ . The bode plot of the voltage CLTF  $\frac{V_C(s)}{V_{ref}(s)}$  for the inner loops is shown in Fig. 3. Fig. 3 shows the magnitude and phase response of the cascaded inner loops. The cascaded inner loops exhibit a bandwidth of 40Hz at the fundamental frequency for a switching frequency of 8kHz, while the selective harmonic control terms introduce bandpass characteristics at 150Hz, 250Hz and 350Hz in addition to the fundamental frequency as

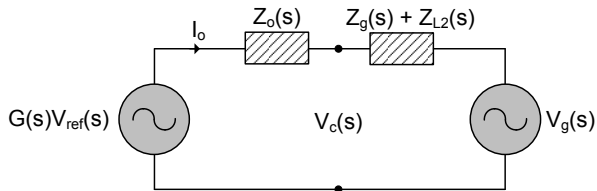


Fig. 4. Equivalent Thevenin circuit for a grid-connected VC-VSI where  $Z_o(s)$  is the output impedance of the inverter,  $Z_{L2}(s)$  is the impedance of the transformer at the output of the respective inverter and  $Z_g(s)$  is the grid impedance at the PCC.

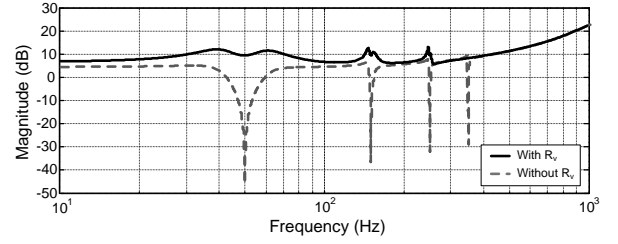


Fig. 5. Bode plot of the inverter output impedance  $Z_o(s)$  with and without the virtual resistance  $R_v = 3\Omega$ .

shown in Fig. 3. The designed PR controller gains are:  $K_{pV} = 0.1$ ,  $K_{pI} = 2$ ,  $k_{iV} = 0.4\omega_h$ ,  $k_{iI} = 0.4\omega_h$ ,  $\omega_{cVh} = 0.002\omega_h$  and  $\omega_{cIh} = 0.002\omega_h$ .

### III. ANALYSIS OF THE OUTPUT IMPEDANCE OF THE MICROGRID INVERTERS

The CLTF can be represented by a two-terminal Thevenin equivalent circuit as:

$$V_C(s) = G(s)V_{ref}(s) - Z_o(s)i_o(s) \quad (6)$$

where  $G(s) = \frac{V_C(s)}{V_{ref}(s)}$  is the voltage gain transfer function and  $Z_o(s)$  represents the output impedance transfer function of the VC-VSI. Hence from (6), the output impedance  $Z_o(s)$  of the inverter is seen to depend on the voltage and current controllers in addition to the impedance of the output filter. The Thevenin's equivalent circuit of the inverter in grid-connected operation is shown in Fig. 4. The bode plot of the output impedance  $Z_o(s)$  given in Fig. 5 shows that the output impedance of the inverter is very low at the 50Hz, 150Hz, 250Hz and 350Hz due to the PR controllers which explains why PR controllers are capable of minimizing the harmonic output from the inverters.

The virtual output resistance  $R_v$  was included in the inner control loops with the aim of improving the stability of the inverter as shown in Fig. 2. The CLTF of the inner loops including the effect of  $R_v$ , can now be expressed as:

$$V_C(s) = \frac{G_I(s)G_V(s)Z_C(s)}{Z_C(s) + Z_L(s) + G_I(s) + G_I(s)G_V(s)Z_C(s)} V_{ref}(s) - \frac{G_I(s)G_V(s)Z_C(s)R_v + Z_C(s)(Z_L(s) + G_I(s))}{Z_C(s) + Z_L(s) + G_I(s) + G_I(s)G_V(s)Z_C(s)} i_o(s) \quad (7)$$

$R_v$  also appears in the output impedance transfer function  $Z_o(s)$  of the new two-terminal Thevenin equivalent circuit derived from (7). The bode plot of the output impedance including the effect of  $R_v$  is also given in Fig. 5. The output impedance of the inverter is now finite over the whole frequency range and the compensation provided by the PR controllers becomes insufficient to attenuate the output harmonics. Therefore, voltage and current harmonics are injected in the grid at all frequencies if the grid has non-zero voltage harmonics during grid-connected mode. In addition local non-linear loads will increase the harmonic current output by the inverters. The finite impedance causes voltage harmonics at



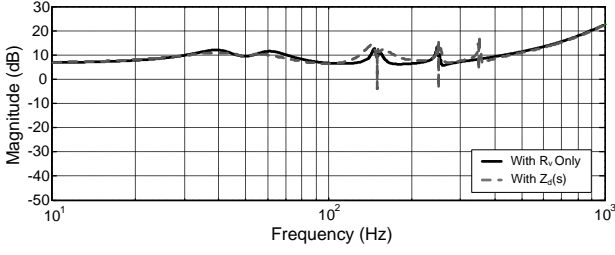


Fig. 9. Bode plot of the inverter output impedance with  $R_v = 3\Omega$  only and with  $Z_d(s)$

$$V_C(s) = \frac{G_I(s)G_V(s)Z_C(s)}{Z_C(s) + Z_L(s) + G_I(s) + G_I(s)G_V(s)Z_C(s)} V_{ref}(s) - \frac{G_I(s)G_V(s)Z_C(s)Z_d(s) + Z_C(s)(Z_L(s) + G_I(s))}{Z_C(s) + Z_L(s) + G_I(s) + G_I(s)G_V(s)Z_C(s)} i_o(s) \quad (11)$$

Hence, the frequency response shown in Fig. 3 which was obtained for the cascaded voltage transfer function  $V_c(s)/V_{ref}(s)$  still applies in this case. This is expected since the capacitive virtual impedance transfer function  $Z_d(s)$  only depends on the output current  $i_o(s)$ . The output impedance of the inverters with the virtual resistance  $R_v$  of  $3\Omega$  is compared with the new output impedance with the additional virtual capacitive impedance in Fig. 9. The capacitive virtual impedance only affects the output impedance of the inverters at the 3<sup>rd</sup>, 5<sup>th</sup> and 7<sup>th</sup> harmonics, while the characteristics at all the other frequencies are not affected. Hence the stability of the inner loops is not compromised with the additional optimization loop.

## V. VIRTUAL ADMITTANCE-BASED CURRENT HARMONIC COMPENSATION IN GRID-CONNECTED OPERATION

The proposed virtual admittance loop improves the output current THD of the VC-VSIs due to grid voltage harmonics. This admittance emulates the behavior of passive tuned filter bank at the output of the VC-VSI as shown in Fig. 10. Each filter is tuned at a specific harmonic frequency and the low frequency harmonics up to the 13<sup>th</sup> harmonic were considered. The virtual admittance transfer function  $Y_d(s)$  can then be obtained by deriving the transfer function for this virtual bank of passive filters as shown in this section.

The block diagram of the proposed virtual admittance  $Y_d(s)$  is shown in Fig. 11 and is made from two parts: harmonic voltage extraction and harmonic compensation. The first step is the extraction of the voltage harmonics present in the grid voltage via a series of bandpass filters tuned at the required frequencies. Hence:

$$V_h(s) = \frac{\omega_n s}{s^2 + \omega_n s + \omega_h^2} V_o(s) \quad (12)$$

where  $V_h$  is the harmonic voltage component,  $\omega_n$  determines the bandwidth of the bandpass filter,  $\omega_h$  is the  $n^{\text{th}}$  harmonic frequency and  $V_o$  is the PCC voltage measured at the output of the VC-VSI. The voltage at each harmonic is then multiplied by the admittance of the corresponding tuned filter so as to

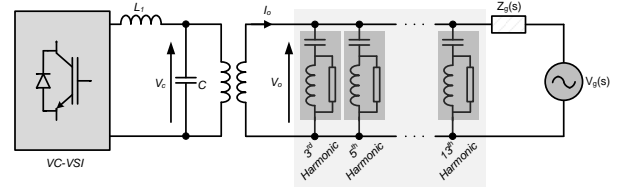


Fig. 10. Concept diagram for the proposed virtual admittance  $Y_d(s)$  which was designed to emulate the behavior of a passive tuned filter bank.

obtain the harmonic current compensation for the inner control loops. The admittance  $Y_h(s)$  for each of the considered virtual shunt passive filters is given by:

$$Y_h(s) = C_h \frac{\omega_n s^2 + \omega_h^2 s}{s^2 + \omega_n s + \omega_h^2} \quad (13)$$

where  $\omega_n$  determines the bandwidth at each harmonic and  $\omega_h$  is the  $n^{\text{th}}$  harmonic frequency. The virtual admittance transfer function  $Y_d(s)$  can then be obtained by combining  $Y_h(s)$  for all the considered harmonics. Hence:

$$i_h(s) = \sum_{h=3}^{13} V_h(s) Y_h(s) \quad (14)$$

$$= C_h \frac{\omega_n s}{s^2 + \omega_n s + \omega_h^2} \frac{\omega_n s^2 + \omega_h^2 s}{s^2 + \omega_n s + \omega_h^2} V_o(s) \quad (15)$$

$$Y_d(s) = \sum_{h=3}^{13} C_h \frac{\omega_n s (\omega_n s^2 + \omega_h^2 s)}{(s^2 + \omega_n s + \omega_h^2)^2} \quad (16)$$

where  $i_h(s) = Y_d(s)V_o(s)$  is the harmonic current applied to the input of the current loop. The unknown gain for each harmonic frequency  $C_h$ , can be determined from the magnitude of (16) at  $\omega = \omega_h$ , by defining the attenuation provided by  $Y_h(s)$  at  $\omega = \omega_h$ . The resulting bode plot for the designed virtual admittance transfer function  $Y_d(s)$  is shown in Fig. 12.

## VI. EXPERIMENTAL RESULTS

The experimental setup shown in Fig. 13 consists of two 2kVA Semikron single phase full bridge inverters with LC

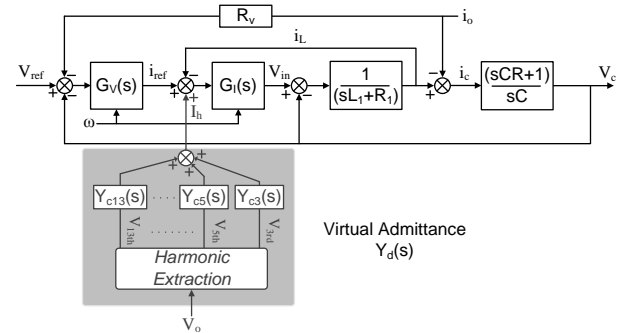


Fig. 11. Block diagram of the inner control loops showing the proposed virtual admittance loop where  $i_h(s) = Y_d(s)V_o(s)$  and  $i_h(s)$  is the harmonic current compensation applied to the inverter current loop and  $V_o$  is the locally measured PCC voltage.



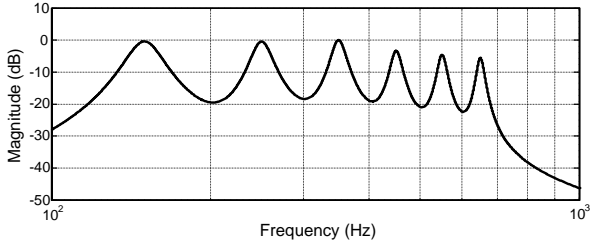


Fig. 12. Magnitude vs. frequency response of the virtual admittance transfer function  $Y_d(s)$ .

output filters and a local non-linear load. The inductance and resistance referred to the primary of transformer T1 are  $L_2 = 4.2\text{mH}$  and  $R_2 = 0.958\Omega$  respectively with a magnetizing inductance of  $L_M = 2.75\text{H}$ . The inductance and resistance of the transformer T2 referred to the primary are  $L_2 = 2.5\text{mH}$  and  $R_2 = 0.465\Omega$  respectively with a magnetizing inductance of  $L_M = 0.63\text{H}$ . A dSPACE DS1103 PPC controller was used to implement the control algorithms of the VC-VSI microgrid inverters. The sampling frequency of the voltage and current measurements and the frequency of the unipolar pulse width modulation signals for the IGBTs is 8kHz. The reference voltage and frequency of the microgrid VC-VSIs are 220V RMS and 50Hz respectively.

#### A. Islanded Voltage Harmonic Compensation

Initially the microgrid was in islanded mode and the two VC-VSIs were connected in parallel to supply the local non-linear load. The improvements in harmonic current sharing and in the voltage harmonic distortion at the PCC were then verified experimentally by comparing the performance of the islanded microgrid with and without the capacitive virtual impedance loop.

The magnitude of the voltage harmonics that were measured at the PCC with and without the capacitive virtual impedance are given in Fig. 14. The  $V_{THD}$  measured without compensation was of 2.414% while with compensation the  $V_{THD}$  was reduced to 1.826%. This implies a reduction of 24.3% in the  $V_{THD}$  thereby showing the effectiveness of the algorithm in attenuating the voltage harmonics at the PCC. The current harmonics with and without compensation are shown in Fig. 15. Therefore one can observe that the introduction of

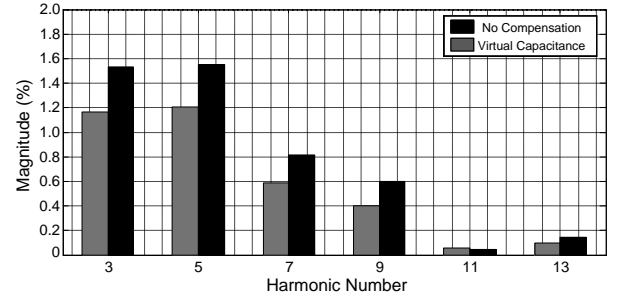


Fig. 14. Voltage harmonics at the PCC obtained by the experimental setup during islanded operation expressed as a percentage of the fundamental voltage component.

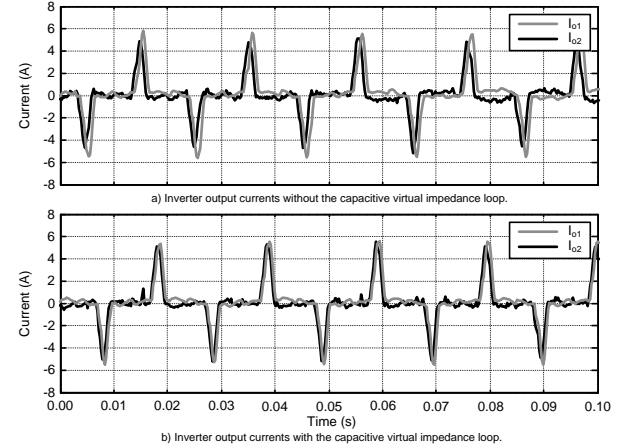


Fig. 15. Current Sharing at the PCC obtained by the experimental setup during islanded operation.

the capacitive impedance loop also improves significantly the harmonic current sharing.

Additional tests were performed to verify the operation of the proposed capacitive virtual impedance for the case of active and reactive power mismatches between the inverters. Mismatch in the power shared between the two inverters was achieved by modifying the droop gains of Inverter 1 to  $m = 0.015\text{rad/W.s}$  and  $n = 0.03\text{V/VAr}$ . The  $P - \omega$  droop gains of the inverters are therefore sized according to  $2m_1 = m_2 = 0.03\text{rad/W.s}$  while the  $Q - E$  droop gains of the inverters are  $2n_1 = n_2 = 0.06\text{V/VAr}$ . This implies that for the same voltage and frequency deviations, Inverter 1 should output twice the active and reactive power output of Inverter 2. No additional changes were performed in both the simulation model and experimental setup. The improvements in harmonic current sharing and in the voltage harmonic distortion at the PCC were then verified experimentally by comparing the performance of the islanded microgrid with and without the capacitive virtual impedance loop.

The harmonic current output by the inverters should be divided according to the ratio of their droop gains. However, without the additional virtual impedance loop, the harmonic current sharing between the inverters is determined by the ratio of the output impedances of the inverters as discussed in Section III. This results in harmonic voltage distortion

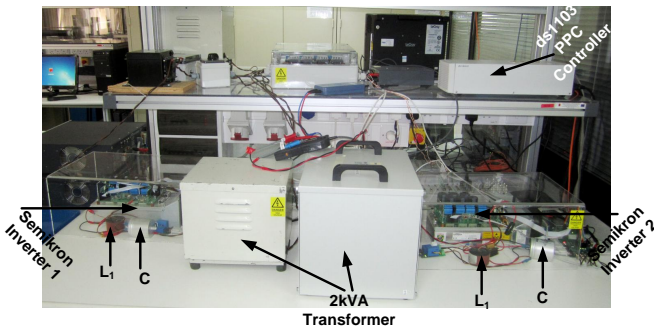


Fig. 13. Laboratory experimental setup for the single phase microgrid.

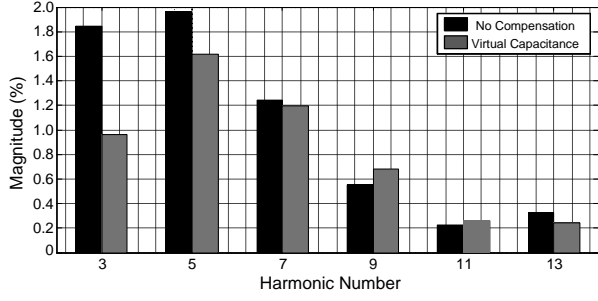


Fig. 16. Voltage harmonics at the PCC obtained by the experimental setup during islanded operation for power mismatches between the two inverters expressed as a percentage of the fundamental voltage component.

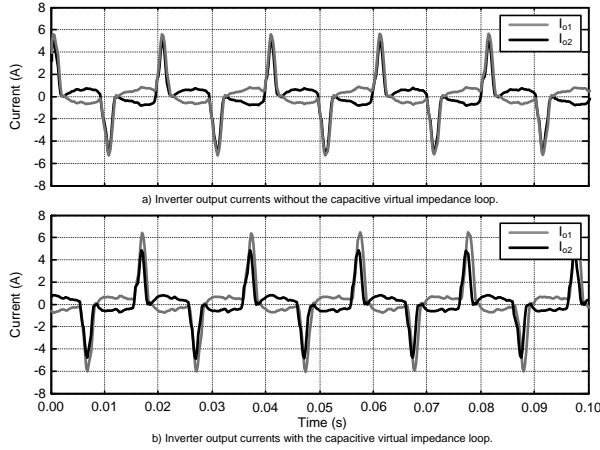


Fig. 17. Current Sharing at the PCC obtained by the experimental setup during islanded operation for power mismatches between the two inverters.

levels which were measured at 3.04% without compensation as shown in Fig. 16. The harmonic current output by the inverters is shown in Fig. 17 and it is quite evident that the harmonic current sharing does not occur according to the inverter droop gains.

When the capacitive virtual impedance is introduced the  $V_{THD}$  was reduced to 2.36% as shown in Fig. 16. This implies a reduction of 22.7% in the  $V_{THD}$  thereby showing the effectiveness of the algorithm in attenuating the voltage harmonics at the PCC. The current harmonics with the capacitive virtual impedance are also shown in Fig. 17. One can observe that, the capacitive impedance loop reduces the harmonic current supplied by inverter 2 when compared to the uncompensated case. This implies an improvement in the harmonic current sharing which now occurs nearly according to the inverter droop gains.

### B. Grid-Connected Operation Including the Local Non-Linear Load

The microgrid was then synchronized and connected to the grid with the VSIs in grid-connected mode. The active and reactive power demand of the VSIs were fixed at 1600W and 0Var respectively. Although in grid-connected operation the main supply of current harmonics to the local loads is obtained from the utility grid, the low output impedance of the

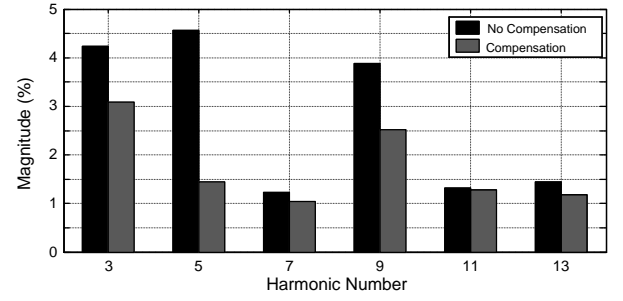


Fig. 18. Current harmonics output by inverter 1 at the nominal power output of 1600W with the grid voltage THD at 1%.

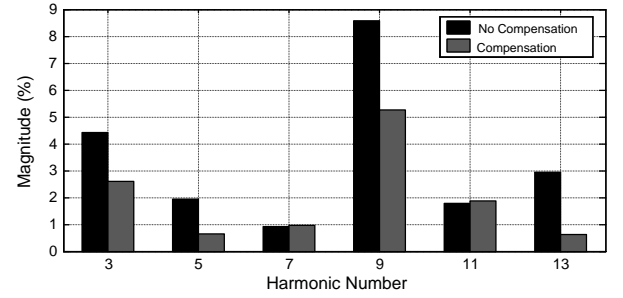


Fig. 19. Current harmonics output by the inverter 2 at the nominal power output of 1600W. The grid voltage THD is at 1% with additional current harmonics drawn by the non-linear load.

VSIs causes the VSIs to share some of the harmonic demand from the local loads. The additional harmonic current injection reduces the maximum output power that can be exported into the grid by the VSIs. In addition there is also grid voltage distortion of the local utility grid which was measured at 1%. The output current harmonics for the VC-VSIs without compensation at the nominal power of 1600W are given in Fig. 18 and Fig. 19.

Characterizing the harmonic distortion at the output of the inverter using the THD is misleading when the output current of the inverter is less than the nominal power rating [25]. A meaningful way to describe the harmonic content is through the total demand distortion (TDD) which defines the total demand as a percentage of the selected load current such as the peak demand [25]. The resulting current TDD for inverter 1 is 6.46% while that for inverter 2 is 9.04%. The power factor including both displacement and distortion factors of both inverters is 0.96. The difference in output current THD of the inverters is due to the different output transformer impedances. T1 causes the resonant frequency of the output filter to be close to the 5<sup>th</sup> harmonic thereby causing a larger 5<sup>th</sup> harmonic current to flow. T2 causes the resonant frequency of the output filter to be close to the 9<sup>th</sup> harmonic thereby causing a larger 9<sup>th</sup> harmonic current to flow.

The output current harmonics of the inverters are attenuated when the virtual admittance loop is enabled as shown in Fig. 18 and Fig. 19. The inverter output power was kept constant at 0Var and 1600W and the power factor remained unchanged at 0.96. The resulting current TDD dropped to 3.96% for inverter 1 and to 5.22% for inverter 2, which implies a reduction of

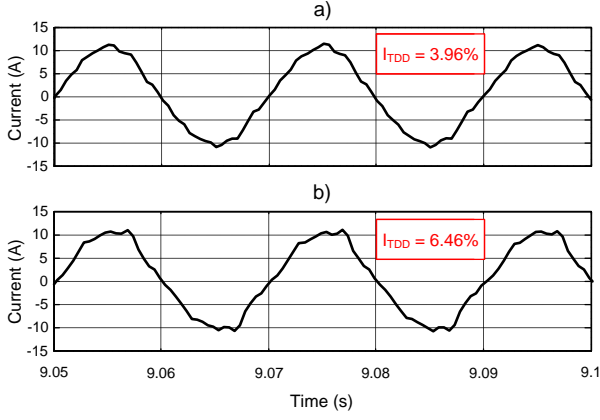


Fig. 20. Experimental results showing the output current of inverter 1 at 1600W. The grid voltage THD is at 1% with additional current harmonics drawn by the non-linear load. a) With grid harmonic compensation b) Without grid harmonic compensation.

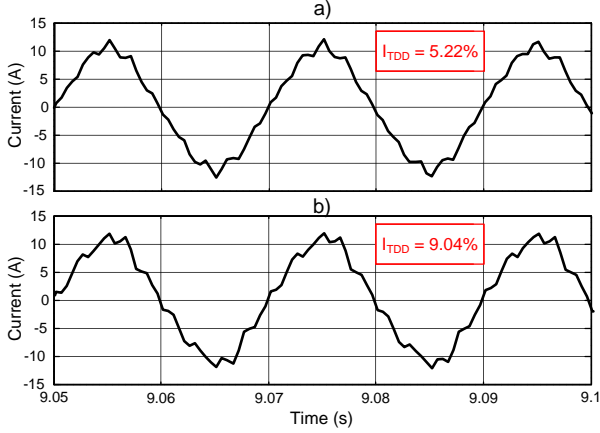


Fig. 21. Experimental results showing the output current of inverter 2 at 1600W with the grid voltage THD at 1%. a) With grid harmonic compensation b) Without grid harmonic compensation.

39% and 42.3% respectively. The effect on the inverter output current is shown in Fig.20 and Fig.21 where the current with compensation becomes more sinusoidal due to the reduction in harmonics.

### C. Effectiveness Of The Virtual Admittance Loop At Different Power Outputs

Additional tests were carried out at different power levels to verify the performance of the proposed virtual admittance loop. The power output of each inverter was increased in steps of 100W up to the nominal power and the TDD of the output current was noted in each case. The results for Inverter 1 are given in Fig.22 while a similar curve was observed for inverter 2. One may note that due to the TDD the high dependence that the output power of the inverter has on the current THD is avoided and the attenuation in the harmonics can be observed more clearly. This is an obvious conclusion since the magnitude of the harmonic currents are not affected by the changes in the power output of the inverter while the fundamental current component varies according to the active

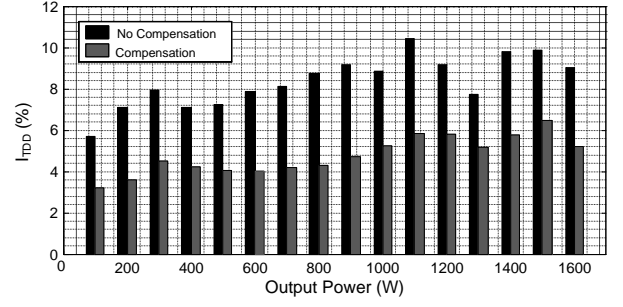


Fig. 22. Total Demand Distortion of the output current vs. inverter output power for inverter 1.

power output. The proposed grid-compensation loop is seen to compensate for the grid harmonics independently from the power level of the inverter. The reduction in TDD which was achieved at the different output powers by the virtual admittance loop was of 40% over the whole output power range.

## VII. CONCLUSION

This paper considers the effect of current harmonics in islanded and grid-connected microgrids. In this paper, virtual impedances and admittances were proposed to improve the harmonic reduction of linear harmonic compensators. The linear harmonic compensators were implemented in the form of PR controllers which were tuned such that their center frequency is at odd multiples of the fundamental. A virtual admittance loop was proposed in this paper with the aim to attenuate the harmonic current injection by the VC-VSIs into the grid due to grid voltage harmonic distortion. A virtual capacitive impedance loop was used in islanded mode to improve the harmonic current sharing and attenuate the voltage harmonics at the PCC due to a single phase rectifier load. Experimental results were given to verify the operation of the proposed algorithms in achieving their respective aims.

In islanded operation, experiments were carried out with the two VSIs supplying a single phase rectifier load which cause voltage distortion at the PCC with a measured THD of 2.414%. When the virtual capacitive impedance loop was enabled, the  $V_{THD}$  decreased by 24.3% to 1.826% while the harmonic current sharing improved significantly. In grid connected operation, experiments were carried out at a nominal power output of 1600W. The TDD of the output current decreased by approx. 40% for both inverters when the virtual admittance loop was enabled. The power factor of the inverter was not affected by the change in distortion factor since its contribution is negligible when compared to the displacement angle. Additional results have shown that the improvement in TDD is obtained over the whole output power range, with an average reduction calculated at 40% for both inverters. Therefore, the operation of the PR controllers was improved significantly with the introduction of the virtual impedances and admittances. The proposed loops also have the additional advantage of being much simpler to design and implement than grid feed-forward compensation techniques for

this application. Grid feed-forward compensation techniques for the cascaded PR controllers with harmonic compensation as considered in this paper would result in an impractical feed-forward transfer function due to its high order and complexity.

## APPENDIX A

### DESIGN DATA FOR THE CAPACITIVE VIRTUAL IMPEDANCE LOOP

Inverter	VC-VSI 1	VC-VSI 2
$k_{p3}$	$3.7840 \Omega$	$3.5120 \Omega$
$k_{i3}$	$3.2987 F^{-1}$	$2.2619 F^{-1}$
$k_{p5}$	$3.7840 \Omega$	$3.5120 \Omega$
$k_{i5}$	$5.4987 F^{-1}$	$3.7699 F^{-1}$
$k_{p7}$	$3.7840 \Omega$	$3.5120 \Omega$
$k_{i7}$	$7.6969 F^{-1}$	$5.2779 F^{-1}$

## APPENDIX B

### DESIGN DATA FOR THE VIRTUAL ADMITTANCE LOOP

The gains  $C_h$  that were designed for selective harmonic compensation of the 3<sup>rd</sup>, 5<sup>th</sup> and 7<sup>th</sup> harmonic via the virtual admittance are equal to  $17 \times 10^{-5} \Omega^{-1}$ ,  $6.2 \times 10^{-5} \Omega^{-1}$  and  $3.3 \times 10^{-5} \Omega^{-1}$  respectively.

## REFERENCES

- [1] A. Micallef, M. Apap, C. Spiteri-Staines, J. M. Guerrero, and J. C. Vasquez, "Reactive Power Sharing and Voltage Harmonic Distortion Compensation of Droop Controlled Single Phase Islanded Microgrids," *IEEE Trans. Smart Grid*, vol. 5, no. 3, pp. 1149–1158, May 2014.
- [2] T.-L. Lee and P.-T. Cheng, "Design of a New Cooperative Harmonic Filtering Strategy for Distributed Generation Interface Converters in an Islanding Network," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1919–1927, Sep. 2007.
- [3] "IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems," *IEEE 1547-2003*, 2003.
- [4] "Characteristics of the utility interface for photovoltaic systems," *IEC 61727*, 2004.
- [5] J. Miret, M. Castilla, J. Matas, J. Guerrero, and J. Vasquez, "Selective Harmonic-Compensation Control for Single-Phase Active Power Filter With High Harmonic Rejection," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3117–3127, Aug. 2009.
- [6] S. Chakraborty and M. Simoes, "Experimental Evaluation of Active Filtering in a Single-Phase High-Frequency AC Microgrid," *IEEE Trans. Energy Convers.*, vol. 24, no. 3, pp. 673–682, Sep. 2009.
- [7] J. M. Guerrero, P. C. Loh, T.-I. Lee, and M. Chandorkar, "Advanced Control Architectures for Intelligent Microgrids—Part II: Power Quality, Energy Storage, and AC/DC Microgrids," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1263–1270, Apr. 2013.
- [8] M. Savaghebi, A. Jalilian, J. C. Vasquez, and J. M. Guerrero, "Secondary Control for Voltage Quality Enhancement in Microgrids," *IEEE Trans. Smart Grid*, vol. 3, no. 4, pp. 1893–1902, Dec. 2012.
- [9] A. Micallef, M. Apap, C. Spiteri-Staines, and J. M. Guerrero, "Selective virtual capacitive impedance loop for harmonic voltage compensation in islanded MicroGrids," in *IECON 2013 - 39th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2013, pp. 7968–7973.
- [10] M. Savaghebi, J. M. Guerrero, A. Jalilian, and J. C. Vasquez, "Mitigation of voltage and current harmonics in grid-connected microgrids," in *2012 IEEE Int. Symp. Ind. Electron.*, May 2012, pp. 1610–1615.
- [11] G. Escobar, P. Mattavelli, M. Hernandez-Gomez, and P. R. Martinez-Rodriguez, "Filters With Linear-Phase Properties for Repetitive Feed-back," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 405–413, Jan. 2014.
- [12] K. Zhou, Y. Yang, F. Blaabjerg, and D. Wang, "Optimal Selective Harmonic Control for Power Harmonics Mitigation," *IEEE Trans. Ind. Electron.*, vol. PP, no. 99, 2014.
- [13] Y. Yang, K. Zhou, H. Wang, F. Blaabjerg, D. Wang, and B. Zhang, "Frequency Adaptive Selective Harmonic Control for Grid-Connected Inverters," *IEEE Trans. Power Electron.*, vol. PP, no. 99, 2014.
- [14] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.
- [15] M. Castilla, J. Miret, J. Matas, L. Garcia de Vicuna, and J. Guerrero, "Control Design Guidelines for Single-Phase Grid-Connected Photovoltaic Inverters With Damped Resonant Harmonic Compensators," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4492–4501, Nov. 2009.
- [16] T. Abeyasekera, C. M. Johnson, D. J. Atkinson, and M. Armstrong, "Suppression of Line Voltage Related Distortion in Current Controlled Grid Connected Inverters," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1393–1401, Nov. 2005.
- [17] X. Wang, X. Ruan, S. Liu, and C. K. Tse, "Full Feedforward of Grid Voltage for Grid-Connected Inverter With LCL Filter to Suppress Current Distortion Due to Grid Voltage Harmonics," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3119–3127, Dec. 2010.
- [18] W. Li, X. Ruan, D. Pan, and X. Wang, "Full-Feedforward Schemes of Grid Voltages for a Three-Phase LCL-Type Grid-Connected Inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2237–2250, Jun. 2013.
- [19] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla, "Hierarchical Control of Droop-Controlled AC and DC Microgrids—A General Approach Toward Standardization," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 158–172, Jan. 2011.
- [20] J. M. Guerrero, J. C. Vasquez, J. Matas, M. Castilla, and L. G. de Vicuna, "Control Strategy for Flexible Microgrid Based on Parallel Line-Interactive UPS Systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 726–736, 2009.
- [21] W. Yao, M. Chen, J. Matas, J. M. Guerrero, and Z.-M. Qian, "Design and Analysis of the Droop Control Method for Parallel Inverters Considering the Impact of the Complex Impedance on the Power Sharing," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 576–588, Feb. 2011.
- [22] J. Matas, M. Castilla, L. G. de Vicuña, J. Miret, and J. C. Vasquez, "Virtual Impedance Loop for Droop-Controlled Single-Phase Parallel Inverters Using a Second-Order General-Integrator Scheme," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 2993–3002, Dec. 2010.
- [23] M. Savaghebi, A. Jalilian, J. C. Vasquez, and J. M. Guerrero, "Secondary Control Scheme for Voltage Unbalance Compensation in an Islanded Droop-Controlled Microgrid," *IEEE Trans. Smart Grid*, vol. 3, no. 2, pp. 797–807, Jun. 2012.
- [24] R. Ni, Y. W. Li, Y. Zhang, N. R. Zargari, and Z. Cheng, "Virtual Impedance-Based Selective Harmonic Compensation (VI-SHC) PWM for Current Source Rectifiers," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3346–3356, Jul. 2014.
- [25] IEEE Std 519-2014, "IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems, 2014.



Alexander Micallef (S'09) received the B.Eng.(Hons.) degree, the M. Sc. degree in communication engineering and the Ph.D. degree in microgrids from the University of Malta, Malta, in 2006, 2009 and 2015, respectively. Since 2008 he has been an Assistant Lecturer with the Department of Industrial Electrical Power Conversion at the University of Malta. In 2012, he was a visiting PhD student at the Department of Energy Technology, Aalborg University, Denmark. His research interests include power electronics, renewable energy systems, energy management systems, control and management of distributed generation and energy storage systems in AC and DC microgrids.



Maurice Apap (M'07) received the B.Eng. (Hons.) and M.Sc. degree in electrical engineering from the University of Malta, Malta in 1996 and 2001 respectively, and the Ph.D. degree in power electronics from the University of Nottingham, Nottingham, U.K. in 2006. He is currently a Senior Lecturer and Head of the Department of Industrial Electrical Power Conversion at the University of Malta. His research interests include power electronic converters and the control of electrical drives.



**Cyril Spiteri Staines** (M'94) received the B.Eng.(Hons.) degree from the University of Malta in 1994, and the Ph.D. degree in Electrical Engineering from the University of Nottingham, 1999. In 1995, he joined the Faculty of Engineering, University of Malta as an Assistant Lecturer, where he became a Lecturer in 1999, Senior Lecturer in 2004, and Associate Professor in 2007. From 2003 to 2004, he was a Postdoctoral Researcher and Visiting Lecturer at the University of Nottingham.

His research interests include sensorless AC motor drives, power converter control and grid connection of renewable energy sources. Prof. Spiteri Staines is a member of the IEEE, IET and IEEJ.



**Josep M. Guerrero** (S'01-M'04-SM'08-F'14) received the B.S. degree in telecommunications engineering, the M.S. degree in electronics engineering, and the Ph.D. degree in power electronics from the Technical University of Catalonia, Barcelona, in 1997, 2000 and 2003, respectively. He was an Associate Professor with the Department of Automatic Control Systems and Computer Engineering, Technical University of Catalonia, teaching courses on digital signal processing, field-programmable gate arrays, microprocessors, and control of renewable

energy. In 2004, he was responsible for the Renewable Energy Laboratory, Escola Industrial de Barcelona. Since 2011, he has been a Full Professor with the Department of Energy Technology, Aalborg University, Aalborg East, Denmark, where he is responsible for the microgrid research program. From 2012 he is also a guest Professor at the Chinese Academy of Science and the Nanjing University of Aeronautics and Astronautics. His research interests is oriented to different microgrid aspects, including power electronics, distributed energy-storage systems, hierarchical and cooperative control, energy management systems, and optimization of microgrids and islanded minigrids. Prof. Guerrero is an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and the IEEE Industrial Electronics Magazine. He has been Guest Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS Special Issues: Power Electronics for Wind Energy Conversion and Power Electronics for Microgrids, and the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS Special Sections: Uninterruptible Power Supplies systems, Renewable Energy Systems, Distributed Generation and Microgrids, and Industrial Applications and Implementation Issues of the Kalman Filter. He was the chair of the Renewable Energy Systems Technical Committee of the IEEE Industrial Electronics Society.