Performance Comparison of Phase Shifted PWM and Sorting Method for Modular Multilevel Converters

Haddioui, Marcos Rejas; Máthé, Lászlo; Burlacu, Paul Dan; Pereira, Heverton A. ; Sangwongwanich, Ariya; Bongiorno, Massimo; Teodorescu, Remus

Published in:
Proceedings of the 17th Conference on Power Electronics and Applications, EPE'15-ECCE Europe

DOI (link to publication from Publisher):
10.1109/EPE.2015.7311700

Publication date:
2015

Document Version
Early version, also known as pre-print

Performance Comparison of Phase Shifted PWM and Sorting Method for Modular Multilevel Converters

Marcos Rejas[1], Laszlo Mathe[1], Paul Dan Burlacu[1], Heverton Pereira[2], Ariya Sangwongwanich[1], Massimo Bongiorno[3] and Remus Teodorescu[1]

[1] Aalborg University
Aalborg, Denmark
marcosrejas@gmail.com
lam@et.aau.dk pdb@et.aau.dk
ars@et.aau.dk ret@et.aau.dk

[2] Federal University of Viçosa
Viçosa, Brazil
hevertonaugusto@yahoo.com.br

[3] Chalmers University
Goteborg, Sweden
massimo.bongiorno@chalmers.se

Abstract

Modular Multilevel Converters (MMC) are the solution of preference in HVDC applications due to modularity, scalability, low losses and low filtering requirement. Carrier-based (PWM) and carrier-less (nearest level control) modulation can be applied. By using advanced sorting methods focusing on keeping the capacitor voltage ripple under some limit, unnecessary switching events are eliminated leading to reduced switching losses. This paper presents a comparison between the steady-state performances in terms of output voltage THD and equivalent switching frequency of the Phase Shifted Carrier PWM and NLC plus sorting methods.

I Introduction

Modular Multilevel Converter (MMC) topology is a very promising solution for high power applications such as High Voltage Direct Current (HVDC), high-power STATCOM or high voltage drives. Due to their low switching frequency leads to high efficiency and the high number of output voltage levels requires a minimal grid side filter. Another advantage is that the large number of modules present in the topology ensures fault tolerant operation [1]. In Fig. 1 (a) the structure of MMC is presented, where each leg has an upper and lower arm which together supplies the phase currents (i_a, i_b, i_c). Each arm consist of n series connected sub-modules (SMs) together with an arm inductor (L_{arm}) and resistance (R_{arm}). The simplest construction for the SMs is the so called Half Bridge (HB) topology, through which a capacitor can be inserted or bypassed [2]. Thus, the number of the inserted capacitor voltages from a leg results the phase voltage of the converter. Similarly, the output current is resulted from the difference between the upper and lower arm current. Beside the output current of the MMC a circulating current is present in the converter, which circulates between legs and the DC link. However, the circulating current has no direct impact on the output current it is important to control it in order to maintain high efficiency of the converter [3]. From control point of view the system becomes complex as it is schemed in Fig. 2, several outer loops, such as current voltage control, has to be ensured. Additionally, in case of MMC, especially when large number of SMs are employed, internal control has to be established which ensures balance between the capacitor voltages and controls the circulating current. Several modulation strategies have been proposed in order to control the SM switches, they can be divided in two main classes: carrier based and sorting based algorithms (also called as carrier-less) [3]. From the carrier based modulation techniques, such as: Carrier Disposition (CD) and Phase Shifted Carrier (PSC) Pulse Width Modulation (PWM), PSC-PWM is the most promising due to its independent controllability in the SM [3-5]. Due to the different advantages/disadvantages of the carrier based and sorting method it is difficult to choose the suitable algorithm. In this paper a comparison between PSC-PWM and module sorting methods is presented. In the next section a small overview of the PSC-PWM and carrier-less methods are presented. In the third section two case scenarios are simulated: first when low

number of SMs are employed (4 SMs per arm) and a case scenario with large number of SMs (40SMs per arm). An evaluation of the two cases are also done in the section. In the fourth section an experimental evaluation is performed for the case when low number of modules are used. Finally, the conclusions of the analysis are presented.

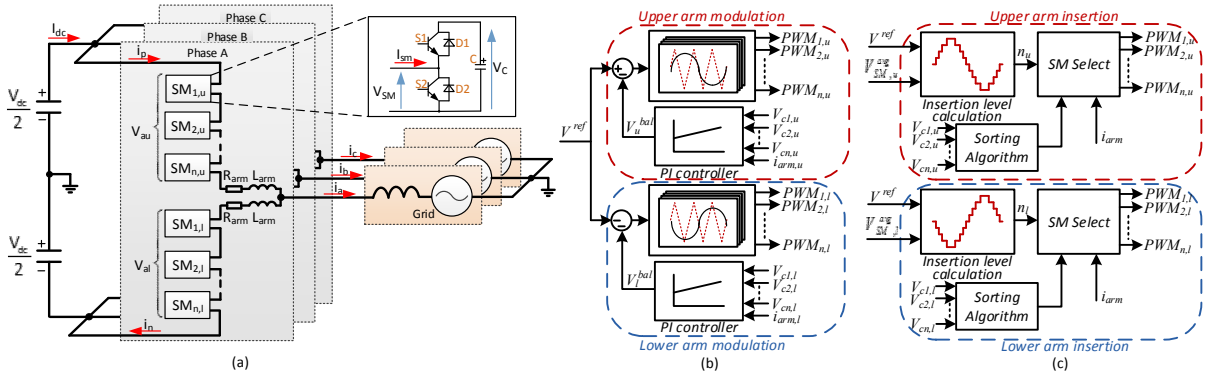

Fig. 1 Structure of: (a) three phase grid connected MMC, (b) PSC-PWM method and (c) NLC+sorting method.

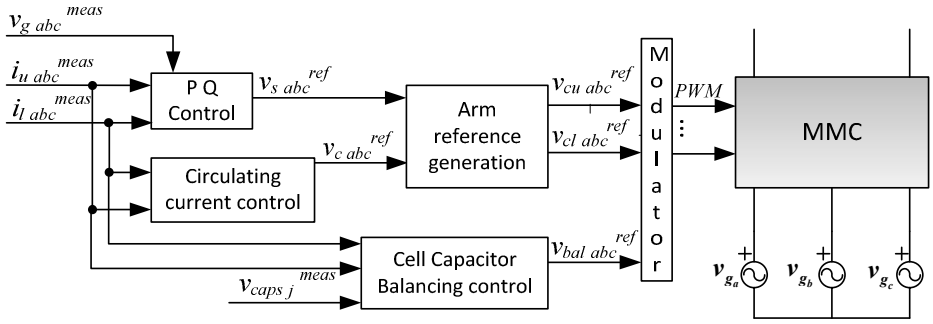

Fig. 2 Typical control block scheme for MMC used in HVDC.

II Description of PSC-PWM technique and sorting algorithm

Different strategies have been proposed in the literature to control the switches from MMC converters. Based on the pulse generation mechanism of two level converters the PSC-PWM method assigns a carrier wave to each SM with the same frequency, amplitude but different phase. The waveforms used for pulse generation for the upper and lower arm SMs are visualized in Fig. 3 (a) for the case when $n=4$. The modulation inside one SM works similarly as for two level converters, when the reference signal is above the carrier the capacitor from SM is inserted, while it is bypassed when the reference signal goes below the carrier. The phase shift between the carrier waves in an arm should be $2\pi/n$ in order to minimize the harmonic content of the output voltage [6]. It has been also analytically proved that the phase shift between the upper and lower arm carriers (noted with θ in Fig. 3 (a)) should be 0 in case n is odd and π/n when n is even to achieve the best performance [4]. The integer multiple between the switching frequency and fundamental frequency should be avoided in order to maintain the balancing between the capacitor voltages [5]. However, in order to control the circulating current and to maintain a balance between the capacitor voltages average and balancing control loop has to be applied as it is shown in Fig. 1 (b) and (c). The capacitor voltage balancing algorithm is based on calculation of the error between the actual voltage of the SM's capacitor and the reference (received form the central controller) which goes into a proportional controller. By considering the sign of the current in the SM, which shows if the capacitor is charging or discharging, the reference value for the modulator is adjusted. With other words the balance is ensured by increasing the actual reference (the

capacitor is inserted for longer time) when the voltage of the capacitor is less than the average should be and charging current is flowing in the SM.

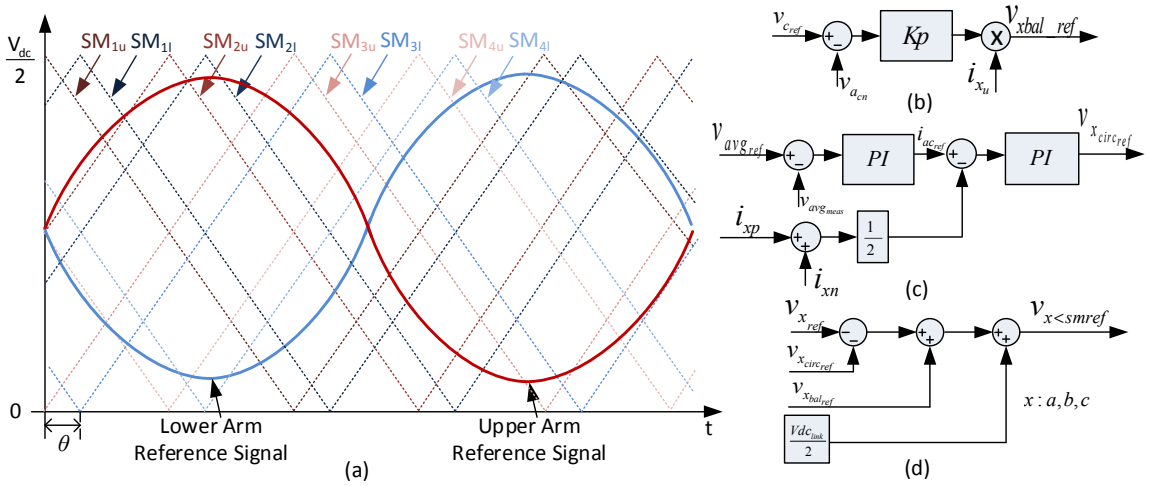

Fig. 3 (a) Pulse generation mechanism for PSC-PWM scheme, (b) block scheme of the capacitor voltage balancing (c) block scheme of the averaging control, and (d) reference signal generation for the SM's modulators in the three-phases.

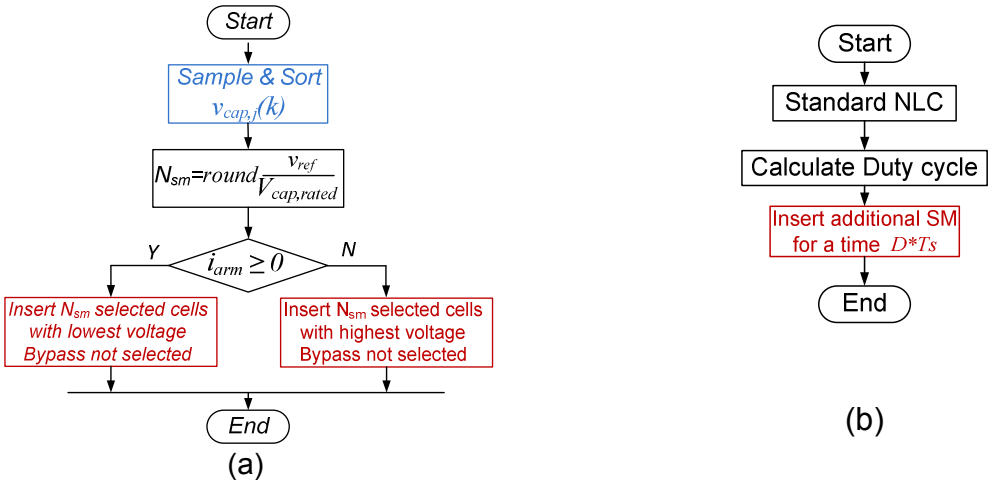

Fig. 4 (a) Standard NLC algorithm flowchart (b) NLC + PWM algorithm flowchart.

While in the other case, when the capacitor voltage in higher than the average the reference is increased when discharging current is flowing. With the average control it can be eliminated the AC components form the circulating current, a PI controller can be used to obtain the reference circulating current from the measured and reference average voltage. Then, with another PI controller the reference voltage can be obtained. The converter can operate without average control, however, the efficiency will not be the highest.

Another way to generate the *on-off* state of the switches from the MMC is to use sorting algorithms. Generally, the method is based on an external control loop, such as the open loop Nearest Level Control (NLC), or closed loop: Tolerance Band (TB) modulation or Selective Harmonic Elimination (SHE) PWM. In each sampling period the external control algorithm provides a reference voltage which is approximated by the number of the inserted SMs [7-10]. Then, the sorting algorithms are based on a constant update frequency; in each update period it is calculated from the reference voltage the number of the modules which needs to be inserted as shown in Fig. 4. This insertion level is obtained by dividing the resultant reference voltage with the average capacitor voltage. Usually, the calculated insertion level is not an integer number, rounding is used to obtain an exact number for the

inserted capacitors. This method is used for the comparison in this paper and it referred as NLC. In order to achieve better approximation, reducing the error caused by rounding, one SM per arm should be inserted by using PWM technique. In this way the average voltage during an update period becomes equal with the reference voltage. This is the third method used for the comparison and it is referred as NLC+PWM.

In contrast to PSC-PWM which requires a voltage balancing loop for the SMs, the sorting algorithm is providing intrinsic balancing of the capacitor voltages. The balancing is achieved by sorting those cells which have high capacitor voltage in discharging mode and sort those with low charge for the charging mode [9]. Typically, the master controller creates a ranking list with the capacitor voltages and selects the highly charged modules when discharging. A disadvantage of the intrinsic balancing is that after an update period several SMs can be discharged to a slightly lower voltage level than the average; thus, they are exchanged with another modules with higher charge. This creates extra switching losses and also voltage peaks and drops appears in the output voltage. A way to minimize the extra switching is to consider the previous insertion state as it is described in [8]. Another method to reduce the number of switching used to exchange a discharged cap with a charged one from the same arm, is to set a tolerance band. Then, the capacitor exchange is performed only if one of the capacitor's voltage goes out from allowed tolerance band [9]. This method has been selected also for the comparison. Similarly as proposed in [9] the tolerance band was set to be 10% above the nominal capacitor voltage. This method is referred as PWM with Capacitor Ripple Control (PWM-CRC [9]) in this paper.

As a conclusion both of the methods (with carrier or carrier-less) are suitable to control an MMC; however, it is not straight forward how to compare their performance. With both PSC-PWM and sorting methods the same number of maximum output voltage level of *n+1* can be achieved. In case of PSC-PWM the number of switching during a fundamental period is constant, while this number is variable in case of sorting method. By increasing the number of the employed SMs the above presented modulation methods are showing different behaviour. In the next section the efficiency, THD of the output current of an MMC with different modulation strategies are evaluated for low and high number of SMs.

III Evaluation of the PSC-PWM and the Sorting methods

In order to evaluate the modulation methods an MMC model with low number of SMs (4 SMs per arm) and a model with high number of modules (40 SMs per arm) has been built in simulation software named PLECS. The SM capacitance for the two cases has been chosen based on [11]:

$$C_{sm} = \frac{|S|}{3\omega} \frac{1}{V_{DC} V_{cell_{nom}} \Delta V} \quad (1)$$

where S is the apparent power of the converter, V_{DC} is the value of the full DC-link, $V_{cellnom}$ is the nominal cell voltage and ΔV is desired cell voltage ripple in per unit. Then, for simulation of the system with 4 SMs an arm inductance of L_{arm}= 25mH and for the capacitor from the SMs resulted C_{sm}=30μF. For the system with 40 SMs L_{arm}= 25mH while C_{sm} = 310 μF. The main parameters of the considered HVDC are summarized in Table 1.

Table 1: Parameters of the MMC used in HVDC

Active power	300 MW	
cos φ	0.957	
DC link voltage	±320 kV	
Alternating voltage	400 kV	
Arm inductance	0.015 pu.	

In order to evaluate solely the modulator performance the simulations has been done in open loop, avoiding in this way the effect of the current controllers. Also, in order to avoid the effects of the load on the harmonic content of the output voltage and current a resistive load has been connected.

The voltage ripple in the capacitor has been calculated in percentage where the amplitude of the AC component has been divided with the nominal capacitor voltage, this means 0% is a pure DC value while 100% means the amplitude of the ripple is equal with the nominal capacitor voltage value. For the circulating current the amplitude peak to peak of the ripple was divided by the nominal current of the converter.

In Fig. 5 the simulated output voltage waveform of the MMC with four SMs per arm for four different modulation techniques are presented. On the first look it seems the number of switching is different for the four methods, however, this is due to the fact when a capacitor in an arm gets discharged is bypassed and another one from the same arm with higher charge is inserted. Then, this capacitor exchange will cause on the output voltage waveform only a small change. Moreover, it can be noticed, that the error in the output voltage respect to the reference voltage is higher for the cases where no modulation is performed. In Fig. 6 the spectrum of the output voltages are presented for each modulation method. The spectrum of PSC-PWM has large harmonic content around the cell switching frequency (447 Hz). In case of sorting with PWM the main group of harmonics are placed around 3 kHz (two times the sampling frequency). For the two sorting cases without PWM consist of spread low frequency harmonics, which is very inconvenient, from grid filters point of view.

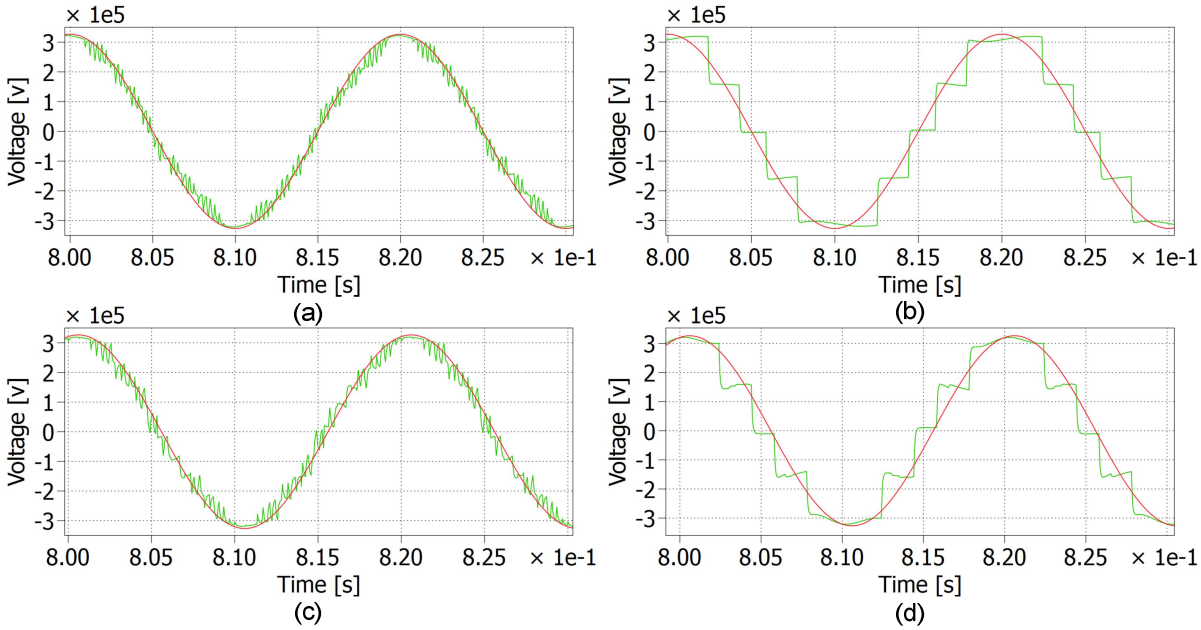

Fig. 5 Output voltage waveform of a phase of the MMC when: (a) PSC-PWM, (b) NLC, (c) NLC+PWM and (d) NLC+CRC modulation technique has been used.

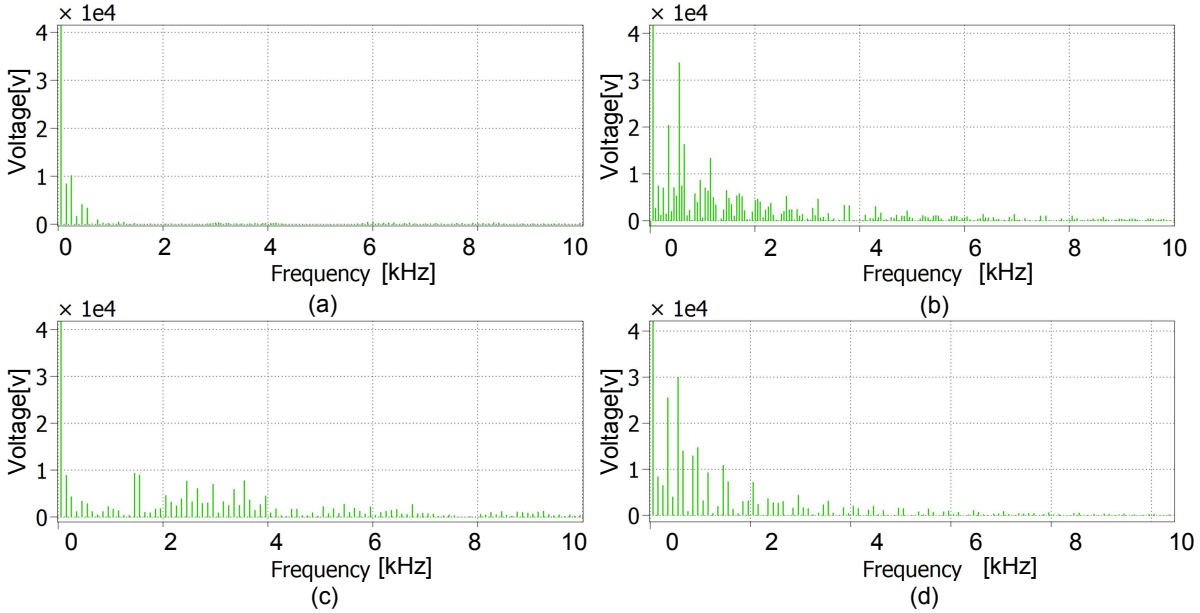

Fig. 6 Harmonic Spectrum of the output voltage waveform in case of: (a) PSC-PWM, (b) NLC, (c) NLC+PWM and (d) NLC+CRC.

Table 2 Characteristic parameters of the simulation when 4 SMs are placed in an arm.

Modulation Technique	PSC-PWM	NLC	NLC+PWM	NLC+CRC
Switching freq. [Hz]	447	400-500	400-500	400-500
Output voltage THD [%]	8.25	17.2	9.7	17.6
Sampling freq. [Hz]	3576	3250	1500	15000
Capacitor voltage ripple [%]	15	9	10	10
Circulating current ripple [pu]	5.8	3.8	5.3	4.26

Based on the above presented simulations in Table 2 the main parameters, such as output voltage THD, capacitor voltage ripple and circulating current ripple, of the four modulation methods have been inserted. From THD point of view PSC-PWM and NLC+PWM have the best performance, while the methods without modulation the THD content is higher. On the other side, the capacitor voltage and the circulating current ripple is considerably smaller when sorting methods were used.

A very important factor from external control point of view, especially when low number of SMs are used, is the sampling frequency. The NLC+CRC has almost 10 times larger sampling compared to the other method, which ensures the best controller performance in the overall system. Due to the low sampling frequency NLC+PWM has a high circulating current ripple while a very slight decrease can be noticed on the output voltage THD. When the control of the MMC is designed it is important decision is to use distributed or centralized control. The PSC-PWM has the advantage compared to the NLC methods is that the modulation can be distributed in the SMs [12]. As a conclusion for low number of SMs NLC+CRC gives a very good compromise, with a slight increase in the capacitor voltage and circulating current ripple compared to NLC and NLC+PWM, while high sampling frequency can be obtained. The main reason to select PSC-PWM as modulator would be due to the possibility to distribute the modulation in the SMs.

The simulation results for the second case when large number of SMs are employed (40 SMs per arm) is presented in Fig. 7. For this case scenario the arm inductance has been set to L_{arm}= 25mH, and the SM capacitor to 310μF.

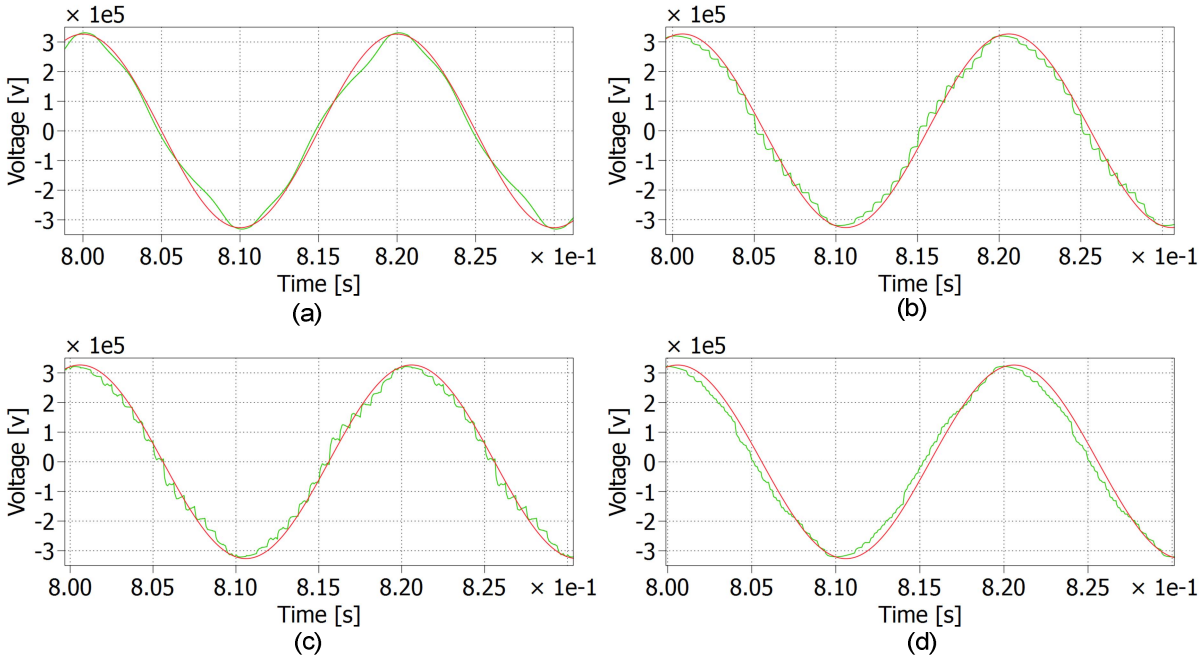

Fig. 7 Output voltage: (a) PSC-PWM (b) NLC (c) NLC+PWM (d) NLC+CRC.

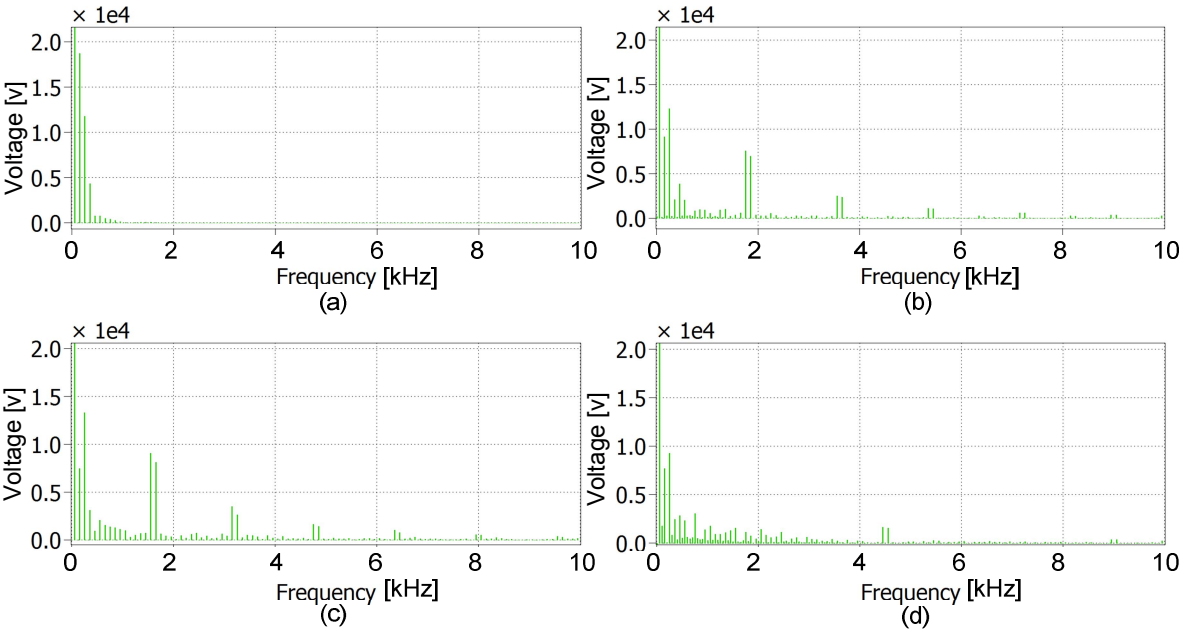

Fig. 8 Harmonic Spectrum of the output voltages where: (a) PSC-PWM, (b) NLC, (c) NLC+PWM, and (d) NLC+CRC modulation methods were used.

For this case a switching frequency of 247 Hz per SM has been chosen for the PSC-PWM. The frequency has been chosen in a way to not be an integer multiply of the fundamental frequency in order to avoid imbalances at the capacitor voltage [4]. Then, the capacitor sampling frequency becomes 19760 Hz, as it can be seen in Table 3. Due to the high number of capacitors in this case, in the standard NLC method after each sampling period a high number of capacitors have to be exchanged, which leads to a lower sampling period when the number of switching is similar to PSC-PWM.

Table 3 Characteristic parameters of the simulation when 40 SMs are placed in an arm

Modulation Technique	PSC-PWM	NLC	NLC+PWM	NLC+CRC
Switching freq. [Hz]	247	200-300	200-300	200-300
Output voltage THD [%]	7.35	6.42	6.86	4.77
Sampling freq. [Hz]	19760	1800	1500	4500
Capacitor voltage ripple [%]	18	15	18	15
Circulating current ripple [pu]	6.47	5.3	5.3	5.88

As a conclusion, for high number of SMs is that the NLC will generate high number of switching during a fundamental period because many capacitors are exchanged (in the same arm a capacitor is bypassed while another one is inserted without having any effect on the output voltage, it is done solely for capacitor voltage balancing) after one sampling. At high number of SMs, the number of voltage levels are also increased and the modulation of a single module in an arm (in order to achieve better approximation) produced a smaller increase in the output voltage. The usage of a tolerance band for the capacitor voltage produces reduces the cell exchange in the arms, leading to reduce the switching frequency and therefore the switching losses in the SMs. The PSC-PWM has the advantage of ensuring evenly distributed switching losses between the SMs, and also gives the possibility to distribute the modulation in the SMs reducing the calculation load of the central calculation unit. In terms of THD the NLC+CRC has a better performance due to the high sampling frequency that it can be achieved.
In Table 4 are depicted the results of the comparison where the output voltage THD is fixed. It can be noticed that for the same THD, the NLC and NLC+PWM methods offers higher switching frequency than the other two methods.

Table 4 Characteristic parameters of the simulation when 40 SMs are placed in an arm.

Modulation Technique	PSC-PWM	NLC	NLC+PWM	NLC+CRC
Output voltage THD [%]	4.65	4.7	4.7	4.7
Switching freq. [Hz]	387	600	600-800	250-400
Sampling freq. [Hz]	30960	3750	3500	4750
Capacitor voltage ripple [%]	22	10	10	16
Circulating current ripple [pu]	5.9	4.7	4.7	5.3

IV Experimental validation

A small scale MMC setup has been built for experimental test and it is shown in Fig. 9. Similarly to the simulation with low number of SMs the setup is formed by 4 SMs in each arm. The parameters of the laboratory setup are shown in Table 5. In the setup EtherCAT communication network has been established between the SMs and the central calculation unit. The implemented modulation techniques are: PSC-PWM, Standard NLC and NLC + PWM. Limited by the EtherCAT communication bandwidth the high sampling NLC-CRC method was not implemented. The measured waveforms with the setup are presented in Fig. 10. Comparing the waveform with the simulated results presented in Fig. 5 and Fig. 6 it can be noticed that they are very similar.

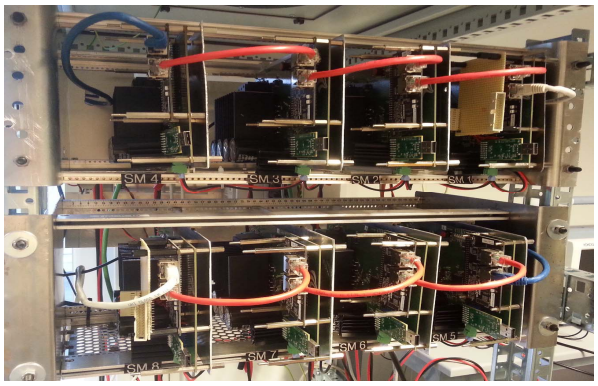

Table 5: Parameters of the MMC setup

DC link voltage	400 V
Cap. voltage	100 V
Arm Resistance	0.2 Ω
Arm Inductance	1.8 mH
Load Resistance	35.5 Ω

Fig. 9 Picture of the single phase MMC setup.

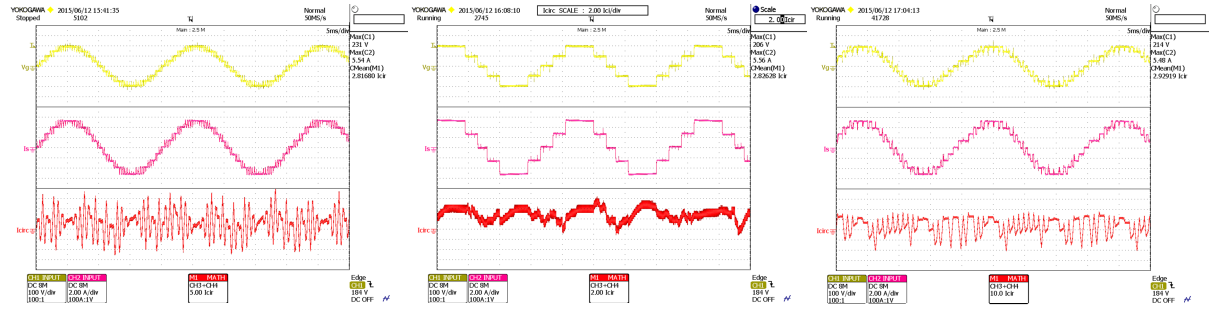

Fig. 10 Experimental results of the three modulation methods. In the top plot of (a), (b) and (c) output voltage, middle plot of (a), (b) and (c) output current, bottom plot of (a), (b) and (c) circulating current. Modulation methods : (a) PS-PWM, (b) sorting with standard NLC, (c) NLC with PWM.

Similarly to the simulations the sampling frequency, output voltage THD, capacitor voltage ripple, circulating current ripple has been introduced in Table 6.

Table 6 Measurement results with 4 SMs/arm

Modulation Technique	PSPWM	NLC	NLC+PWM
Sampling freq. [Hz]	888	2400	900
Capacitor voltage ripple [%]	4	1.8	1.5
Output voltage THD [%]	13	17	16
Circulating current ripple [pu]	11	2.5	11.5

V Conclusions

A comparison between modulation techniques NLC, NLC+PWM, NLC+CRC and PSC-PWM for MMC has been carried out. The same number of switching events during a fundamental period has been maintained for all the modulation methods during the tests. Two cases, first with low number of SMs per arm (4 SMs) and a second case with high number of SMs per arm have been analyzed.

At low number of SMs the NLC+CRC has a big advantage of operation with high sampling frequency compare to the other methods. This is an important factor from the overall system point of view. The modulation of a single module on an arm ensures better approximation of the reference voltage, reducing the low frequency harmonic content of the output voltage.

At high number of SMs when NLC and NLC+PWM method is used a very small difference in the cell capacitor voltages can lead to bypass of a capacitor and insertion of another one in the

same arm just to maintain their voltage balanced. This has almost no effect on the output voltage increasing switching loss. The modulation of a single module on an arm at high number of SMs has low influence on the output voltage performance. However, it increases the complexity of the entire system. For high and low number of SMs, the PSC-PWM has the advantage compare to the other methods the modulation can be distributed in the SMs and the switching losses are evenly distributed between the SMs.

References

[1] R. Teodorescu, E.-P. Eni, L. Mathe, and P. Rodriguez, "Modular Multilevel Converter Control Strategy with Fault Tolerance," in *International Conference on Renewable Energies and Power Quality (ICREPQ'13)*, Bilbao (Spain), 2013.

[2] A. Nami, L. Jiaqi, F. Dijkhuizen, and G. D. Demetriades, "Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 18-36, 2015.

[3] S. Debnath, Q. Jiangchao, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 37-53, 2015.

[4] L. Binbin, Y. Rongfeng, X. Dandan, W. Gaolin, W. Wei, and X. Dianguo, "Analysis of the Phase-Shifted Carrier Modulation for Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 297-310, 2015.

[5] K. Ilves, L. Harnefors, S. Norrga, and H. P. Nee, "Analysis and operation of modular multilevel converters with phase-shifted carrier PWM," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 396-403.

[6] D. G. Holmes and B. P. McGrath, "Opportunities for harmonic cancellation with carrier-based PWM for a two-level and multilevel cascaded inverters," *Industry Applications, IEEE Transactions on,* vol. 37, pp. 574-582, 2001.

[7] N. A. Khan, L. Vanfretti, L. Wei, and A. Haider, "Hybrid Nearest Level and open loop control of modular multilevel converters," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014, pp. 1-12.

[8] M. Schroeder, S. Henninger, J. Jaeger, A. Rasic, H. Rubenbauer, and T. Lang, "An enhanced modulator concept for the Modular Multilevel Converter," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014, pp. 1-10.

[9] A. Hassanpoor, L. Angquist, S. Norrga, K. Ilves, and H. P. Nee, "Tolerance Band Modulation Methods for Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 311-326, 2015.

[10] G. Konstantinou, M. Ciobotaru, and V. Agelidis, "Selective harmonic elimination pulse-width modulation of modular multilevel converters," *Power Electronics, IET,* vol. 6, pp. 96-107, 2013.

[11] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, F. J. Moreno, K. J. Dyke, and D. R. Trainer, "Cell capacitor sizing in modular multilevel converters and hybrid topologies," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014, pp. 1-10.

[12] H. Shaojun, R. Teodorescu, and L. Mathe, "Analysis of communication based distributed control of MMC for HVDC," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-10.