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A Review of Passive Power Filters for Three-Phase Grid-Connected Voltage-Source Converters

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***Abstract*— In order to reduce size and cost, high-order passive filters are generally preferred in power converters to cancel out high-frequency harmonics caused by pulsewidth modulation. However, the filter resonance peaks may require the use of passive dampers to stabilize the interactions between the load and source impedances. Furthermore, the stabilizing effect is more difficult to be guaranteed for cost-optimized filters, which are characterized by low-inductance and high-capacitance passive components. In this paper, several passive filter topologies used to interface voltage-source converters with the utility grid are reviewed and evaluated in terms of damping capability, stored energy in the passive components, and power loss in the damping circuit. In addition, the influences of different switching frequencies of power converters on the passive filter design are discussed in the range 1–15 kHz. Illustrative design examples of the passive filters and experimental data are also provided.**

***Index Terms*— LCL filter, passive filters, resonance damping, trap filter, voltage-source converters (VSCs).**

I. Introduction

DESIGNING passive filters is known to be a complex task [1]. When the harmonic source is a grid-connected voltage-source converter (VSC), then different harmonic spectra on the converter side of the passive filter [2], possible resonance conditions (due to the interaction of the filter with the system impedance) [3], or variation of the harmonic emission with the operating point of the power converter are just a few prerequisites that have to be considered in the design procedure of the passive filter [4]. The harmonic content in a steady-state operation at the point of common coupling (PCC) is, in general, limited by grid connection standards. Several harmonic limits for low-voltage (LV) networks (e.g., VDE-AR-N 4105 [5]), medium-voltage (MV) networks (e.g., BDEW [6]), and LV/MV networks (e.g., IEEE 1547 [7]) are summarized in Table I.

TABLE I
HARMONIC CURRENT LIMITS (% OF RATED CURRENT) FOR SEVERAL GRID CONNECTION STANDARDS

Harmonic order, h	VDE-AR-N 4105 (LV) [5]	BDEW (MV)* [6]	IEEE 1547 (LV & MV) [7]
5	2.08	2.06	4
7	1.39	2.84	4
11	0.69	1.8	2
13	0.55	1.32	2
17	0.42	0.76	1.5
19	0.35	0.62	1.5
23	0.28	0.42	0.6 (23≤h<35)
25	0.21	0.35	
25 < h < 40	5.2/h	8.67/h	0.3 (h>35)
40 < h < 180	6.24/h	6.24/h	

*referred to 400 V and a Short Circuit Ratio (SCR) of 20.

At the component level, additional design considerations are related to the physical design of the passive filter, such as the following:

1) magnetic material adopted for the filter inductors [8], [9];
2) loss and temperature rise in the inductors [10];
3) cooling method [10], [11].

To account for all the aforementioned design factors, multiobjective optimization of the overall conversion system is to be considered, and all can influence on the cost, size, and efficiency of the filter [12]. In addition, the filter design also depends on the adopted filter topology. For a simple inductor (L filter), which is illustrated in Fig. 1, together with other typical passive filter configurations, the resonance of the filter with the system impedance is avoided, since the utility grid is inductive below a few kilohertz in most applications. A large inductance in the L filter is required to limit the high-frequency switching ripple, which results in a bulky and expensive passive filter. However, the low ripple condition leads to a very high efficiency, similar to 50/60 Hz utility transformers. The drawbacks are very high cost and excessive voltage drop across the inductor, which limits the use of this solution for applications above several kilowatts [13], unless interleaved [14] or multilevel VSCs [15] are employed. On the other hand, a low-pass LC or LCL filter provides two or three times more attenuation depending on the adopted cutoff frequency. As a result, a reduced size and cost of the filter

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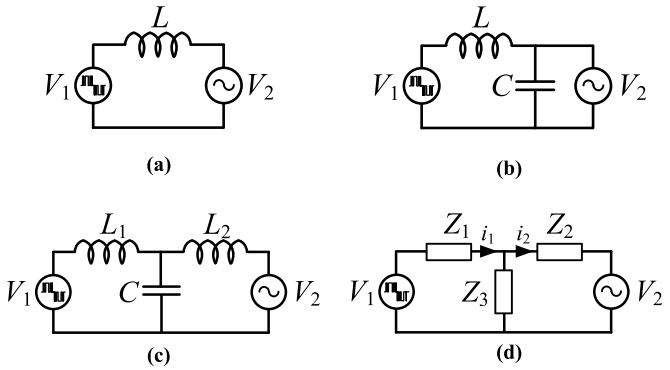


Fig. 1. Passive filters for a two-level grid-connected VSC (per-phase schematics with V_1 the line to line converter voltage and V_2 is the PCC voltage). (a) L filter. (b) Low-pass LC filter. (c) Low-pass LCL filter. (d) Generalized high-order filter model.

can be obtained. On the assumption that the grid impedance is inductive, the LC filter can be perceived as an LCL filter. More complex passive filters, including single or multiple shunt-connected LC-traps [16], can be simplified in a similar way to the LCL filter, by using the generalized high-order filter model from Fig. 1(d).

Particular contributions related to the LCL filter design may include the following:

1) parameter selection based on a conceptual approach [13];
2) parameter selection based on detailed analytical model of the filter [17];
3) optimization based on parameter selection and physical design of the passive components [12].

The LCL filter [18] can be seen, to some extent, as a generalized interfaced high-order filter model (T equivalent circuit), which can describe the stability interactions between the load and source impedance of grid-connected VSCs [19], [20]. The resonance peaks inherent to high-order passive filters may require the use of damping to stabilize the interactions between the load and the source impedances. Explicitly, the filter resonances increase the risk of harmonic amplification at the PCC and can deliberately be avoided by the use of shunt passive-damped filters [21] or active damping control methods [22]. However, in the case of cost-optimized filters, characterized by low-inductance and high-capacitance passive components [23]–[25], the resonance damping is more difficult to be guaranteed. High capacitance in the filter results in high ripple content, both at the converter side inductance and capacitor current/voltage, which adds cost to the sensing system needed to measure the feedback variables required for active damping methods. Sensorless active damping can also be employed, by cascading a digital filter with the current controller loop; however, they are sensitive to parameter variations and system uncertainties [26]. On the other hand, the use of passive damping methods increase the VAr rating of the filter and the associated damping losses [27] in such a way that passive damping is not practical to implement [28]. Then, there is limited evidence of how significant the passive damping losses are, especially for high harmonic current in the shunt capacitor of the filter. To stabilize the control system, proper passive-damped filter solutions and their evaluation for a wide range of operating scenarios become interesting from a practical design point of view (e.g., to minimize the damping losses).

Several passive filter topologies to dampen the filter resonance have been reviewed or discussed in [29]–[31]. However, only limited information about the choice of the damping circuit ratings is given. In [32] and [33], a comparative analysis of the filters is completed for a fixed switching frequency, and one cannot decide which filter topology is best suited, if the application or target switching frequency of the VSC is different [34]. In addition, the amount of resonance damping attenuation and its impact on the dynamic performance of the current controllers and system stability are omitted. Therefore, in this paper, several passive filter topologies used to interface the VSCs with the utility grid are reviewed and evaluated in terms of damping capability, stored energy in the passive components, and power loss in the damping circuit. The damping capability is evaluated using the optimal passive damping design method proposed in [35], while the maximum peak criteria applied in [36] are adopted to ensure the stability of the control system. In addition, the influences of different operating switching frequencies of power converters on the passive filter design are also discussed in the range 1–15 kHz.

An overview of the LCL filter design procedures is described in the forthcoming section with design examples for illustration. In Section III, the selection of several passive filter topologies for dampening the filter resonances is presented. In Section IV, a discussion on the applied methods used to evaluate the passive filters is given. Then, the evaluation of the passive filters is performed for different operating conditions, including different switching frequencies, attenuation requirements, and position of the current sensors. Experimental validation and conclusions complete the content of this paper.

II. Overview of LCL Filter Design

The design of high-order filters is consistent with the LCL filter design in most situations [37]. Therefore, different design criteria are given for the LCL filter in the following.

A. Conventional LCL Filter Design

A step-by-step design procedure for an LCL filter was introduced in [13]. It was suggested that the resonance frequency of the filter should lie between ten times the line frequency and half the switching frequency in order to ensure effective attenuation of the switching harmonics, and to prevent resonances caused by switching harmonics or low-order harmonics from grid background voltage distortion. The design guidelines apply for an operating switching frequency (f_s) of 5∼10 kHz [37]–[43]. In addition, the design procedure proposed in [13] enables a relatively fast design of the passive filter with a reduced number of iterations [25]. For example, it can be summarized as the following.

1) Select the converter side inductance (L_1) based on desired maximum current ripple in inductor ($\Delta i_{1\max}$). A rough estimation of the maximum current ripple in the inductor for a three-phase VSC with the conventional space vector modulation (SVM) can be found from the

volt-second balance principle across the inductor during one instance of the switching period ($1/f_s$) [44]

$$L_1 = \frac{V_{\rm dc}}{24 f_s \Delta i_{1\max}} \tag{1}$$

where $V_{\rm dc}$ is the dc-link voltage of the VSC.

2) Select filter capacitance (C) as a percentage (x) of the base capacitance at rated conditions

$$C = x\% \frac{S}{2\pi f_1 V_{ll}^2} \tag{2}$$

where S is the apparent power of the VSC, f_1 is the fundamental frequency of the grid, and V_{ll} is the grid line to line voltage. The capacitor value should be limited to 5% in order to not decrease the power factor.

3) The total inductance should be limited to 10% in order to limit the voltage drop across the inductors.

Additional dependencies between the filter capacitance and voltage drop across the filter inductors and ac sensors position (used for the reference current control and grid synchronization) were introduced in [45] in order to not overrate the VSC. In [46], the total inductance of the LCL filter is adopted based on a desired control bandwidth that should ensure the VSC controllability. In [38], a split function is used to divide the total inductance of the filter between the converter and grid side inductance. It was shown that in order to limit the current ripple in the converter side inductance (to reduce power loss in the filter) and increase the filter attenuation, it is required that the converter side inductance be dominant in the filter. The filter design based on the consideration of the converter current ripple and some attenuation requirements was proposed in [47]. A similar work is presented in [48] with useful analytical expressions given on how to design the converter side inductor with respect to the saturation level of the magnetic core. The drawback of the above design methods is the conservative choice of parameters, especially for an inexperienced practicing engineer.

B. Optimal Design With Minimization of the Stored Energy

The optimization of the filter parameters based on the minimum stored energy with additional considerations on the ripple current, dc-link voltage reserve for controllability, and attenuation of the filter (derived based on specified harmonic standard limits and analytical solutions of the harmonic voltage spectrum related to the pulse width modulation (PWM) method) are given in [17]. Referring to the notations given in Fig. 1(d), an optimal design method of the LCL filter can be performed as follows.

1) *Define the State-Space Model of the Filter:* The currents on the converter (i_1) and grid side (i_2) of the filter can be written as function of the converter voltage (V_1), grid voltage (V_2) and the corresponding filter admittances, as [32]

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = -\begin{bmatrix} Y_{11} \\ Y_{22} \end{bmatrix} V_1 - \begin{bmatrix} Y_{12} \\ Y_{22} \end{bmatrix} V_2. \tag{3}$$

The filter input admittance (Y_{11}), filter reverse transadmittance (Y_{12}), filter attenuation or forward transadmittance (Y_{21}) and filter output admittance (Y_{22}) in (3) can be written as a function of the equivalent impedances of the filter components [32]

$$\begin{bmatrix} Y_{11} \\ Y_{12} \\ Y_{21} \\ Y_{22} \end{bmatrix} = \frac{1}{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3} \begin{bmatrix} Z_2 + Z_3 \\ -Z_3 \\ Z_3 \\ Z_1 + Z_3 \end{bmatrix}. \tag{4}$$

2) Calculate the amplitude of the converter voltage harmonics, V_1(h), according to the selected PWM method using a simulation platform. To reduce the computational time [25], the amplitude of the individual voltage harmonics can be analytically calculated as indicated in [2] as a function of the harmonic order, dc-link voltage, and modulation index.

3) Calculate the maximum filter admittance ($\rm Y_{21max}$) required to ensure the attenuation of dominant harmonics specific to the PWM method according to applicable harmonic current limits ($i_{\rm limit}$) defined in grid connection standards or other power quality standards, for example, one of those indicated in Table I

$$Y_{21\max}(h) = \frac{i_{\rm limit}(h)}{V_1(h)}. \tag{5}$$

4) Choose the filter components based on the allowable current ripple in the converter side inductance, overrating of the VSC, and so on, by fulfilling the following filter admittance attenuation condition:

$$Y_{21}(h) \le Y_{21\max}(h). \tag{6}$$

In Fig. 2(a), the attenuation admittance $Y_{21}(h)$ is evaluated for a switching/sampling frequency (f_s) of 10 kHz at the ($m_f - 2$) harmonic order as a function of the variation of reasonable values of the LCL filter parameters (where m_f is the modulation frequency, defined as the ratio between the switching frequency and the fundamental frequency). Assuming that the SVM method is used, $Y_{21\max}(m_f - 2)$ is -60 dB for the IEEE 1574 standard. The characteristic frequency of the filter (f_0), defined as the resonance frequency of the filter when there is no resistance in the passive filter, is shown in Fig. 2(b).

Fig. 2 shows that for a 10-kHz VSC, resonance frequencies lower than $\sim 0.2\ f_s$ will lead to conservative designs of the passive filter. From Fig. 2(a), there are sufficient solutions in the design space that fulfills the admittance attenuation condition. To reduce the size and cost of the passive filter, some additional design constraints can be imposed, such as the limitation of stored energy in the inductive components [17], [23]–[25]. In [17], it has been shown that different sets of filter parameters can cause the same attenuation of the filter or similar transient response. Similar conclusions were obtained in [23], when the optimization was performed for different weight ratios between the stored energy of the inductors and capacitors.

The contributions from the filter and the grid equivalent resistances are taken into account in [24], where the filter

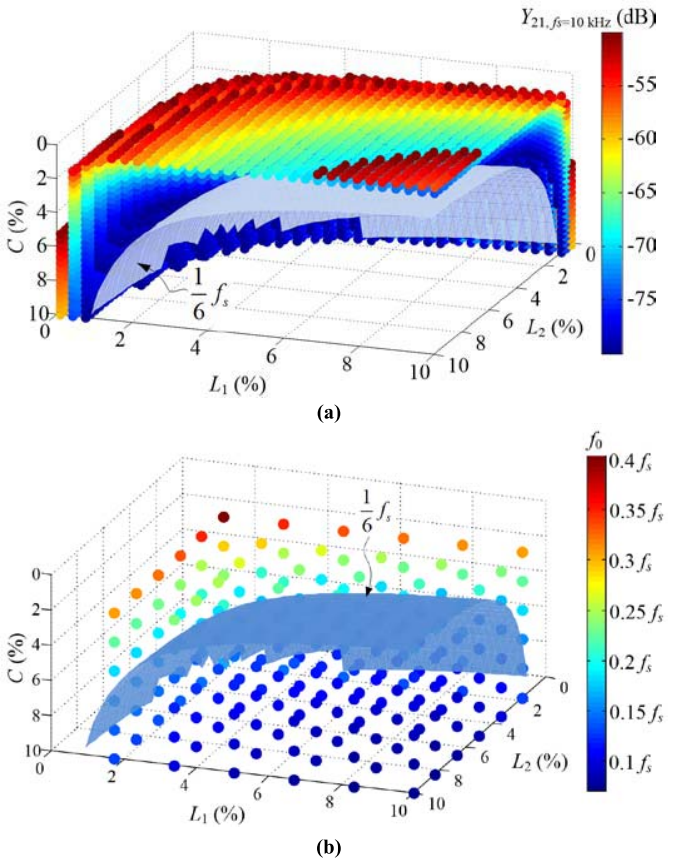
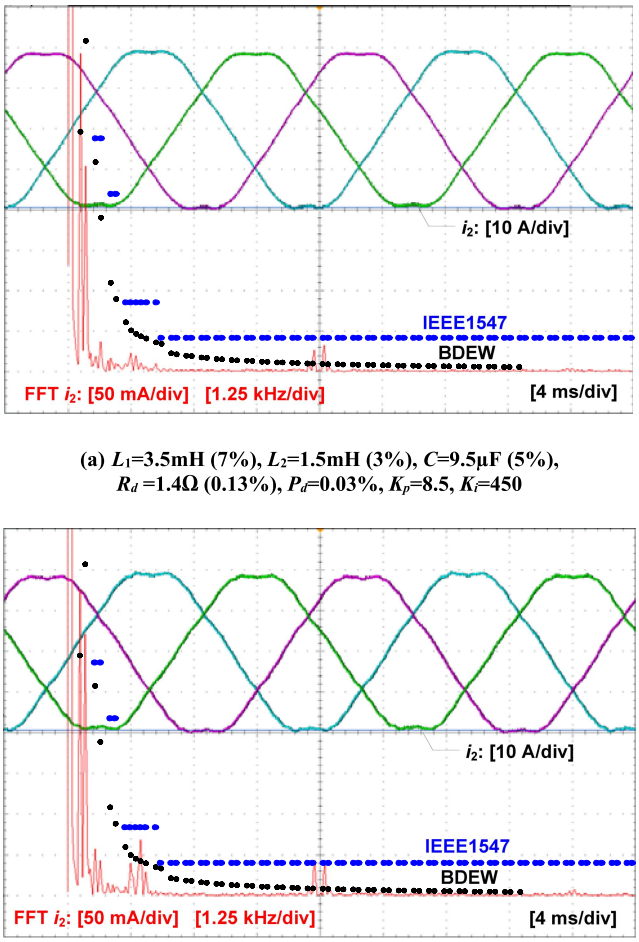


Fig. 2. LCL filter parameters variation as function of (a) high-frequency attenuation admittance, Y_{21} (f_s = 10 kHz) and (b) characteristic frequency, f_0.



(a) L_1=3.5mH (7%), L_2=1.5mH (3%), C=9.5μF (5%), R_d =1.4Ω (0.13%), P_d=0.03%, K_p=8.5, K_i=450

(b) L_1=2mH (4%), L_2=1.5mH (3%), C=20μF (10%), R_d =1.6Ω (0.3%), P_d=0.4%, K_p=5, K_i=250

Fig. 3. Measurements for a designed LCL filter showing the output current harmonics response compared with IEEE 1547 and BDEW limits for a 10-kVA VSC with converter current control and V_{dc} = 700 V and f_s = 5 kHz. (a) Conservative approach. (b) Optimized filter.

is optimized in order to obtain minimum-cost inductors (and therefore filter), which results in very low percentage inductors and high capacitance values. In [25], the total inductance of the filter is minimized for a variable grid frequency specific to aircraft power systems, with relatively high values of the filter capacitors (suggested for the synchronous SVM). However, a high capacitance value in the filter decreases the resonance frequencies in the filter, which, in turn, increases the low-frequency harmonic content and the total harmonic distortion (THD) of the grid current [23]. As a consequence, the optimization of filter parameters, which takes into account the THD limits, is suggested in [49] by considering both the open and closed loop forms of the filter and control system. In [50], the minimization of the total inductance of the filter, which leads to a minimum rms current in the converter side inductance is obtained for an LCL filter applied to a MW range VSC. As a result, a very high filter percentage capacitance (∼40%) was obtained.

C. LCL Filter Design Comparison Between Conventional and Optimal Approach

A two-level 10-kW VSC with a 5-kHz switching frequency is selected to review the previous two design methods. Assuming about 10% ripple in L_1, the resulting inductance is 3.5 mH or 7% according to (1). A 5% filter capacitance from (2) translates into 9.5 μF capacitance. The grid side inductance L_2 is selected 3% or 1.5 mH according to condition 3) from Section II-A. The optimal design method considers the minimization of the stored energy in the filter inductors (7% total inductance and 10% capacitance are chosen). The steady-state current waveform and the filter/VSC ratings are shown in Fig. 3(a) for the conservative approach and in Fig. 3(b) for the optimized filter. The size of the filter for the optimized scenario results in decreased size/cost of the filter by roughly 35%. However, the power losses in the damping resistor used to avoid oscillations are increased by a factor of 13 due to the increased capacitance and increased ripple in the filter inductance. Consequently, the low-order harmonics are more severe (measurements made under same grid condition).

The above example is only to illustrate some possible design scenarios. For the elevated switching frequency, the conservative approach will lead to an increased size compared with the given example. The design of the filters fulfills the IEEE 1547 standard. The more stringent BDEW recommendations imply the use of increased ratings to fulfill the grid connection requirement.

TABLE II
POWER LOSS IN THE VSC AND *LCL* FILTER WITH LAMINATED Fe-Si INDUCTORS(%)

Reference	Frequency range	VSC loss	Filter loss	Core loss calculation method	Verified
[51]	2~6 kHz	0.8~1.5 %	0.1~0.2 %	iGSE	–
[53]	2~12 kHz	0.5~1 %	0.3~0.5 %	NSE	–
[12]	3~12 kHz	0.5~1.2 %	1.2~2.2 %	i^2GSE +loss mapping	yes

D. Parameter Selection Based on Physical Design of Passive Components

All aforementioned designs neglect the influence of the high ripple content and the associated losses in the converter side inductance current due to minimized inductance. Especially, there is an efficiency versus size/cost tradeoff, which dictates the final choice of parameters. In [51], the improved generalized Steinmetz equation (iGSE) is used to investigate the loss of the filter with the aim to minimize the weight of a 2∼6 kHz power filter used in a 1.2-MVA VSC. The Pareto front optimization of the power loss of inductors and semiconductors reveal only a small range variation of the inductor and semiconductor losses (20–30%) with changing the modulation method, core material (laminated Fe-Si versus amorphous), or winding material (Cu versus Al).

The weight of the filter can be decreased by a factor of 4 by increasing the total VSC losses with 50%. Power loss of inductors are in the range 0.1∼0.2% while the semiconductor losses are in the range 0.8∼1.5% depending on the aforementioned variables. The presence of a 5% grid inductance can reduce the filter weight by roughly 40%. However, these results are open for interpretation, since the iGSE method cannot accurately describe the inductor core loss under PWM excitation and dc-bias field strength [52].

In [53], the power loss in the LCL filter and VSC are evaluated at no-load condition using the natural Steinmetz extension method. Here, the core loss results in the range of 0.3%∼0.5% for a switching frequency of 2∼12 kHz, while the power loss in the semiconductors as 0.5%∼1% depending on the modulation method and dc-link voltage. However, the evaluation of instantaneous iron loss in the inductors in [54] show that under load conditions the core loss can be significantly higher. Therefore, different optimized designs of the LCL filter are performed for the grain-oriented Fe-Si material in [12] using more accurate loss models. It is shown that adopting around 20% maximum ripple in the converter side inductance, the total filter loss is in the range of 1.2∼2.2% depending on the adopted volume and switching frequency of the filter. The LCL filter prototype built in [12] yields around 1.8% total power loss, out of which ∼80% of the loss is related to the converter side inductance only. In Table II, a summary of power losses in the VSC (semiconductor and switching loss) and losses in the passive filter is made.

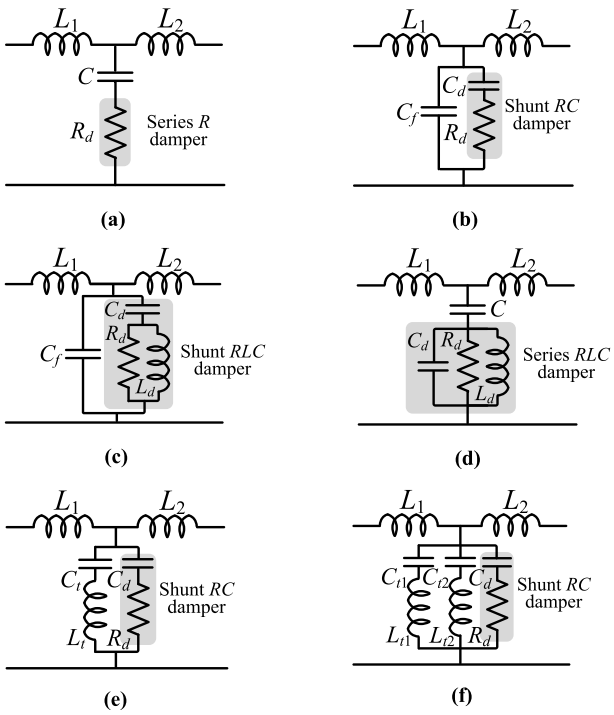


Fig. 4. Selected passive-damped filters to be used in grid-connected VSCs (damper name is referred to with respect to the filter capacitor position). (a) LCL filter + series damper. (b) LCL filter + shunt RC damper. (c) LCL filter + shunt RLC damper. (d) LCL filter + series RLC damper. (e) Trap + shunt RC damper. (f) 2traps + shunt RC damper.

III. FILTER TOPOLOGY SELECTION

It was previously mentioned how a low-pass LCL filter [18] or a trap filter [40] adopted to cancel the ripple content related to the switching device operation can benefit from reduced size and cost. Both filter configurations originates from traditional passive filters used in power system transmission or HVDC systems [27]. The choice of the passive damping topology used to limit the resonance condition of the filters is, in general, based on the conventional shunt passive-damped filters specific to power systems [1], [27], [55] or may be based on shunt or series passive damping methods found in traditional low power dc-dc converter applications [56], [57]. When no physical passive damping circuit is adopted, the equivalent circuit of the filter should consider some damping in order to account for the frequency dependence or the parasitic effects of the passive components. From the passive filter topologies presented in [1], [27], and [55]–[57] only a few are found practicable in today's power conversion units.

A. LCL Filter With Series Resistor

A damping resistor in series with the filter capacitor is one of the most adopted passive damping solutions due to its simplicity in design and implementation [13]. This filter solution is illustrated in Fig. 4(a) with the equivalent series resistance of inductors omitted for simplicity. The damping resistor can also be placed in parallel with the filter capacitor but this solution is not practical since a high ripple current will flow into the resistor [30]. The attenuation performance of the filter can be analyzed by the filter attenuation admittance Y_{21} given in (4). Calculating for the LCL filter with damping

resistor, it results in

$$Y_{21}(s) = A_0 \frac{\frac{Q}{\omega_0}s + 1}{\frac{s^2}{\omega_0^2} + \frac{Q}{\omega_0}s + 1} = A_\infty \frac{\frac{\omega_0}{Q \cdot s} + 1}{\frac{\omega_0^2}{s^2} + \frac{\omega_0 Q}{s} + 1} \quad (7)$$

where A_0 denotes the filter characteristic at frequencies lower than the characteristic frequency ω_0, A_∞ is the characteristic above ω_0 and Q the quality factor of the overall filter [44]. A_0, A_∞, ω_0 and Q can be written as

$$A_0 = \frac{1}{s\,(L_1 + L_2)} \quad A_\infty = \frac{R_d}{L_1 L_2 s^2}$$
$$Q = R_d \sqrt{\frac{C_\Sigma}{L_\Sigma}} = \frac{R_d}{R_0} \quad \omega_0 = \sqrt{\frac{1}{L_\Sigma C_\Sigma}} \quad (8)$$

where L_Σ is the equivalent inductance given by the parallel connection of L_1 and L_2; C_Σ is the equivalent capacitance of the filter given by C; R_d is the damping resistor and R_0 is the characteristic resistance of the filter. For shunt passive damping methods, A_0 have the same formulation as indicated in (8). However, the high-frequency attenuation asymptote given by A_∞ will change depending on the adopted passive filter.

B. LCL Filter With Shunt RC Damper

An improved damping solution can be the shunt RC damper illustrated in Fig. 4(b). The main benefit of this filter is that the high-frequency attenuation of the filter is retained to 60-dB/decade. In addition, the power losses in resistor can decrease with a proper choice of the split capacitor ratio [58]. More details about this filter topology can be found in [35].

C. LCL Filter With Shunt RLC Damper

A good high-frequency attenuation and very low damping loss can be obtained by the second-order damped filter (RLC circuit in parallel with the filter capacitor) as illustrated in Fig. 4(c) [29], since the fundamental current in the resistor is bypassed by the additional damping inductance L_d.

D. LCL Filter With Series RLC Damper

Similar benefits can be obtained by the use of a selective resonant circuit as proposed in [32] and illustrated in Fig. 4(d). The filter contains an additional parallel RLC circuit connected in series with the filter capacitor in which the damping inductor and the capacitor selectively bypasses the damping resistor at low and high frequencies.

The damping element can also be placed in parallel or in series with the grid side inductor [44]. However, the maximum resonance attenuation that can be obtained is more limited compared with the previous damping solutions. In addition, the hardware implementation is impractical, especially if there is no physical grid side inductor in the filter.

E. Trap Filter With Shunt RC Damper

The close-to-zero impedance of the trap filter around the switching harmonics makes it possible to decrease the size of the filter even more compared with the LCL filter [4], [37], [59]–[62]. However, above the tuning frequency, the trap filter is purely inductive and the overall filter attenuation is reduced to only 20 dB/decade. Therefore, an additional capacitor connected in parallel with the trap filter can increase the high-frequency attenuation [60], [61]. However, the presence of multisplit capacitors in the trap filter creates multiple resonances in the filter [61], [62], which increases the risk of resonance amplification between the grid and the filter. Theoretically, the same damping methods can be used for the trap filter as in the LCL filter case. However, the passive damping is more difficult for the trap filter, since the filter components count increases and the advantages over the LCL filter are reduced [33].

A shunt RC damping circuit seems to be a natural choice to damp the trap filter resonance as presented in [60], [62], and [63]. Such circuit is presented in Fig. 4(e).

F. 2traps Filter With Shunt RC Damper

The reduction of the filter size is further possible by adopting multiple single tuned filters in the LCL filter configuration [16] (filter volume decreased by ∼50% in [35] using two single tuned filters). In [64], it was shown that is possible to decrease the filter volume by adopting up to three traps tuned at the switching frequency and its multiples. The shunt RC damper used for the 2*traps* filter is illustrated in Fig. 4(f). Similar to the LCL filter, the design procedures for the trap filters were proposed in [4], [35], [37], [40], [60], [64], and [65].

IV. Passive Damping Design and Stability Criteria

A decreased size and cost of the filter implies to minimize the filter inductance by adopting a higher current ripple in the converter side inductance and a consequently larger capacitance to ensure the same attenuation performance. To retain reasonable power loss in the filter (less than 2%) implies adopting magnetic materials, which can ensure low losses under the high ripple condition [66]. This inevitably leads to an increased risk of harmonic instabilities as results in low resonance frequencies due to high filter capacitance and/or high ripple in the converter side current. To stabilize the interactions between the source and load impedances, the power losses caused by the use of passive damping circuits should be very limited in order not to reduce the system efficiency significantly [67].

A. Passive Damping Design

While a large set of solutions are available for the practicing engineer when an LCL or a trap filter is chosen (as indicated in the design space from Fig. 2), the design of the passive damping circuit is typically straightforward. For instance, if only a series resistor as shown in Fig. 4(a) is adopted, then its value can be found from (8) as percentage (y) of R_0

$$R_d = y\%R_0. \quad (9)$$

The parameter y should be limited up to 30% (resulting in a maximum quality factor of 0.3) in order to limit the power loss in the resistor and to ensure enough attenuation of the filter resonant peaks. For more complex passive filters

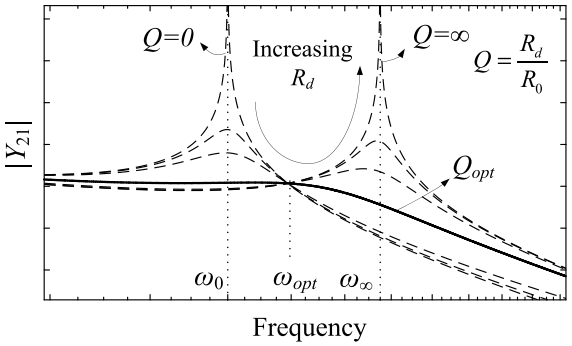


Fig. 5. Optimum quality factor and frequency for passive filters with split capacitors and/or inductors.

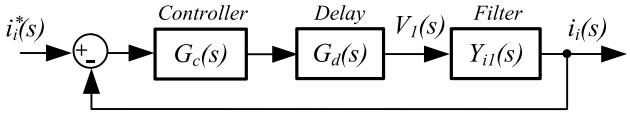


Fig. 6. Current control structure of an VSC connected to an ideal grid voltage source ($i = 1$: converter current is controlled, $i = 2$: grid current is controlled).

with split capacitors or inductors, the design methods given in [35] and [56] can be used to derive the value of the damping resistor. It can be briefly summarized as follows.

1) Design the main passive filter parameters without additional damping, using either of the design method given in Section II and calculate the filter characteristic resistance R_0 and frequency, ω_0 using (8).
2) Find the optimum frequency (ω_{opt}) and quality factor (Q_{opt}) of the filter with damping circuit which minimizes the peak in the filter attenuation admittance. Analytical solutions are given in [35] for the passive filters illustrated in Fig. 4(b), (e), and (f). For other passive filter topologies, the optimum damping parameters can be found using similar derivations. In Fig. 5, the principle of optimum damping is illustrated for passive-damped filters with split capacitor and/or inductors.
3) Choose the ratio of the split capacitors and/or inductors and decide the final value of the quality factor as a tradeoff between damping performance (attenuation of the resonance peak) and power loss in the damping resistor.

B. Stability Criteria and Transient Performance

The closed loop current controller for the converter ($i = 1$) or grid side current ($i = 2$) feedback is illustrated in Fig. 6. The closed loop system includes the current controller (G_c), the delay due to digital computation (G_d) and the plant of the control loop given by the filter (Y_{i1}). The delay is responsible for a phase lag in the control system and typically accounts for up to about 1.5 of the sampling period T_S [45]. The Nyquist stability criterion can be used to assess the control stability, i.e., no $-180°$ crossings should occur when the magnitude of the open loop gain is above 0 dB. The open loop transfer function ($Y_{\mathrm{ol,i}}$) corresponding to the closed loop system from Fig. 6 is given as

$$Y_{\mathrm{ol},i}(s) = G_c(s)G_d(s)Y_{i1}(s), \quad i = 1, 2. \tag{10}$$

The stability of the open loop has a consequent impact on the resonance damping solution of the filter. In addition, for the control system to be stable, the number of encirclements of the critical point $(-1, 0)$ in the open loop transfer function should not change. The maximum peak criteria is adopted in the following in order to simplify the stability analysis of the filter as indicated in [36]. The maximum peak criteria make use of the sensitivity indicator M_S, which denotes the amount of resonance (i.e., maximum peaking) in the sensitivity transfer function $S(s)$ of the control system. $S(s)$ and M_S for the current control feedback are defined as [36]

$$\begin{cases} S_i(s) = \dfrac{1}{1 + Y_{\mathrm{ol},i}(s)}, & i = 1, 2. \\ M_{Si} = \max|S_i(j\omega)| \end{cases} \tag{11}$$

The inverse of the maximum sensitivity gain, $(M_s)^{-1}$ gives the closest distance between the critical point $(-1, 0)$ and the open loop transfer function. Therefore, it contains information about both the gain margin and phase margin of the control system. There are generally applicable design guidelines for a control system to be stable and robust, such as M_S to be lower than 2 (absolute value). Therefore, the lower the value of M_S, the better the robustness, while for stability and performance of the control system, M_S should be close to 1 [68]. For $M_S = 2$, the closed loop poles are well inside the unit circle and the system is said to be stable (controller damping factor of about 0.7). With this design approach, it becomes easy to guarantee the desired dynamic performance of the system.

C. Application of Maximum Peak Criteria for Resonance Damping

The critical frequency is an important parameter in deciding the passive damping solution. For a sampling frequency equal with the switching frequency, the critical frequency is 1/6th of the sampling frequency [69]. Then, for the grid current control feedback, no damping is required if the resonance frequency of the filter seen in the control system is higher than the critical frequency [69]. The opposite is true for the converter current control feedback [70].

The maximum sensitivity gains for the two current feedback solutions are illustrated in Fig. 7. Recalling the LCL filter design space solutions from Fig. 2, it follows from Fig. 7 that for converter current feedback, adopting no passive damping implies very large ratings of the passive components, which leads to very high cost of the filter. In addition, larger L_1 and lower C will improve the control stability (it is expected high percentage values of L_1 and lower values of C and L_2 for a robust filter). For the grid current feedback, it is possible to avoid the use of damping since a large set of filter parameters in the design space fulfill the attenuation requirements. For this case, the stability is mainly improved by decreasing the filter capacitance.

If the operating switching frequency decreases, the available solutions in the design space from Fig. 2 are reduced and the use of damping is mandatory in order to ensure the

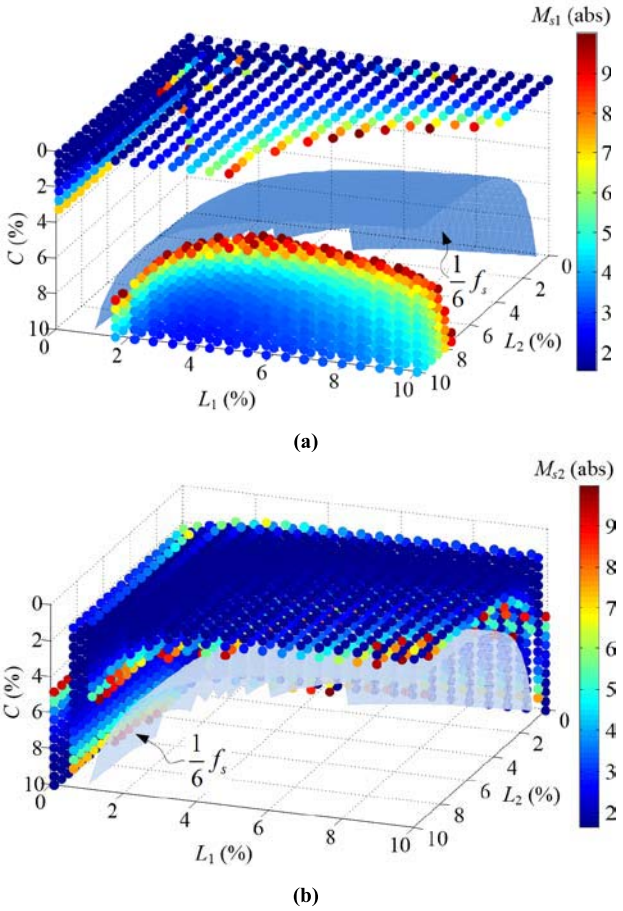


Fig. 7. LCL filter parameter variation as function of the maximum sensitivity (M_S) gain, when $f_s = 10$ kHz. (a) Converter current control. (b) Grid current control.

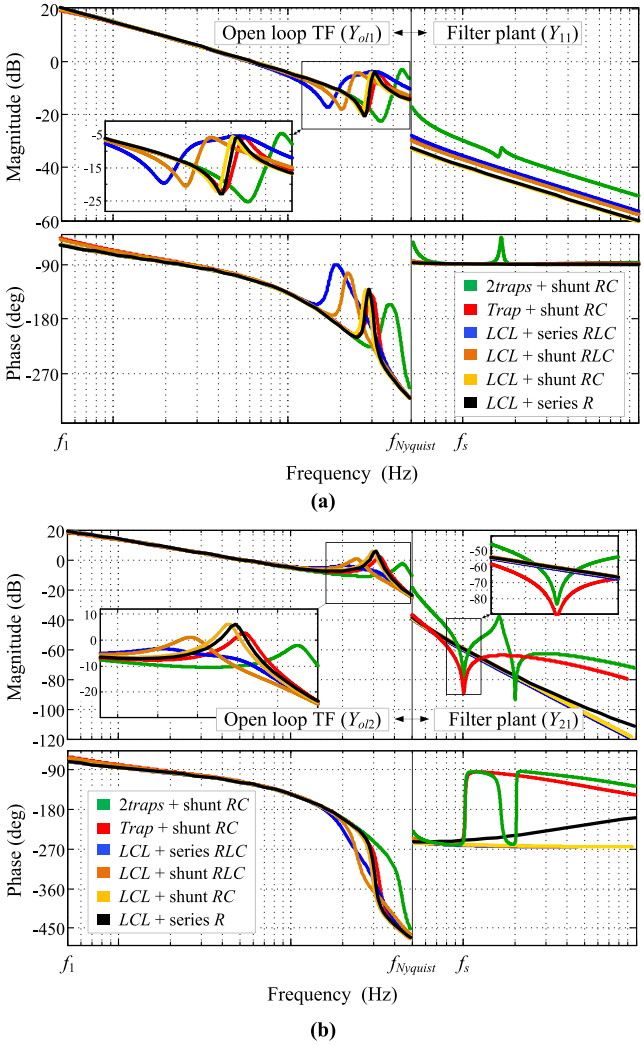


Fig. 8. Frequency response of the passive filters (see Fig. 4) with $M_s \approx 2$. (a) Converter current control. (b) Grid current control.

control stability. In either case, the attenuation of the filter around the resonance frequency of the filter should be carefully investigated. In addition, for good dynamic performance of the control system, M_S should be chosen no larger than 2. By adding passive damping, the design space from Fig. 2 increases and more solutions are available for the filter designer. Then, in order to reduce the power loss in the damping resistor or to meet some stability or transient performance criteria (such as $M_s \approx 2$), the quality factor of the filter can be decreased and adjusted accordingly until the controller specifications are met.

An illustrative example of the frequency response for the selected passive filters for the converter and grid current feedback control are illustrated in Fig. 8. The passive filters are designed to provide the same attenuation of the dominant harmonics, $M_s \approx 2$ and an X/R ratio of 2, around the resonance frequency is selected for the inductive components. The attenuation of the filters can be identified from the magnitude diagram illustrated in Fig. 8(b). The sampling delay ($G_d(s)$) of 1.5 sampling periods in the control system is modeled with a second-order Pade approximation [71].

V. Passive Filters Evaluation

A. Passive Filter Design Prerequisites

The use of passive damping implies different component ratings depending on the operating conditions, mainly given by the operating switching frequency, current feedback method, or harmonic attenuation requirement. Therefore, the passive filters are evaluated as a function of the operating switching frequency and current feedback (i_1 for converter and i_2 for the grid current). In addition, two different harmonic standards are considered for the review, one is the BDEW standard, which is more stringent and used for high power applications (switching frequency $\approx$ 1–5 kHz); the other one is the IEEE 1547, which is more tolerable and can be used for a wide range of applications (switching frequency $\approx$ 1–15 kHz). All the filters are designed to have the same attenuation of the switching harmonic content, except the trap topologies which are designed in a such a way that harmonics around the multiples of the switching frequency complies with the harmonic regulation limits [37]. The resonance attenuation is selected to be the same for all the passive filters, e.g., the sensitivity gain ($M_S \approx 2$) is the same for all the passive filters.

A conventional asymmetrical SVM with one-third harmonic injection is adopted for minimum current ripple and high dc-link voltage utilization [21]. The dc-link voltage is assumed constant for all switching frequencies. However, a high voltage

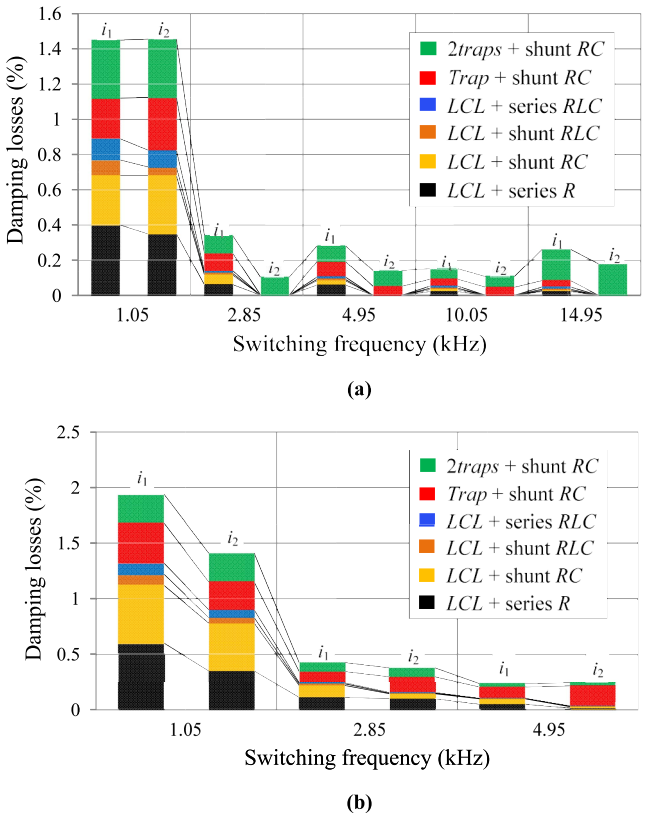


Fig. 9. Damping losses as function of switching frequency for converter (i_1) and grid current control (i_2) calculated according to [58]. (a) IEEE 1547. (b) BDEW.

drop across the inductors for low switching frequencies can lead to very different results with changing the dc-link voltage [51]. The effect would be less significant for switching frequencies above 2.5 kHz. The VSC is operated with unity power factor. It is expected that the results do not vary significantly with different power factors. The converter side inductor L_1 is the dominant component of the filter since it handles both the fundamental and switching ripple current from the power converter. Therefore, in the following, L_1 is referred to as ripple or PWM inductor. L_2 is referred to as line (sine wave) inductor since it is connected in series with the line impedance. To minimize the size of the filter, the ripple current is chosen variable and dependent on the adopted switching frequency. The same applies for the choice of the filter capacitor C. In addition, the sampling frequency is adopted equal with the switching frequency.

B. Passive Damping Losses

The passive filters are designed in such a way to ensure that power losses corresponding to the passive damping circuit are limited to reasonable and practical values. This implies in most of the cases the use of low capacitance values. In Fig. 9, the damping losses are illustrated with different operating switching frequencies of the VSC. The damping losses are averaged for one fundamental period.

For low operating switching frequencies, the damping losses of the series damping resistor is in the same range as the shunt RC damper solution. The key passive damping topologies are the series and shunt RLC circuits, which provide close-to-zero damping loss, especially if the switching frequency is higher than 2.85 kHz. For the grid current feedback and IEEE 1547 recommendations, no damping is required for the LCL filter for frequencies higher than 2.85 kHz. It is not the case for the more stringent attenuation levels as the BDEW recommendations. The damping loss of the 2*traps* filter is relatively larger than other topologies for the IEEE 1547 recommendations due to the fact that it provides reduced sized inductors, and high ripple current flows into the damping circuit.

C. Passive Filter Components Ratings

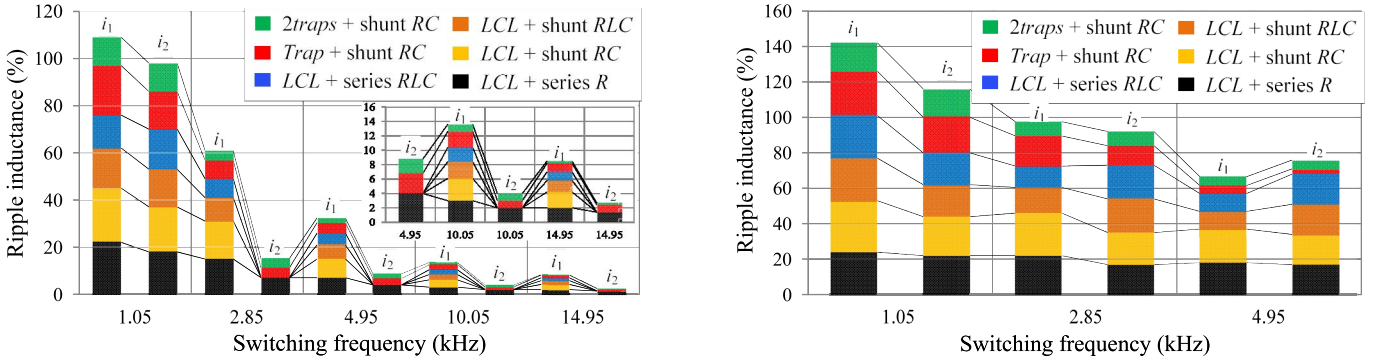
The ratings of the ripple inductance are illustrated in Fig. 10(a). A large difference in the ripple inductance (while keeping the same filter attenuation and dynamic performance) is seen because the ripple in the PWM inductor is chosen variable for different topologies in order to achieve low size of the overall filter.

The size of the line inductance is shown in Fig. 10(b). To guarantee low size of the filter and to ensure the dynamic performance, in case of the converter current feedback, the ripple inductance is chosen higher than the line inductance, while the capacitance is chosen as small as possible to limit the damping loss (<0.5%). For the grid current feedback, the filter inductances are kept around the same, while the capacitance value again is limited. The only exceptions are the series and shunt RLC damping circuits, which allow increased capacitance size in the filter due to the very low damping loss capability. Hence, low size and cost of these filter solutions can be expected.

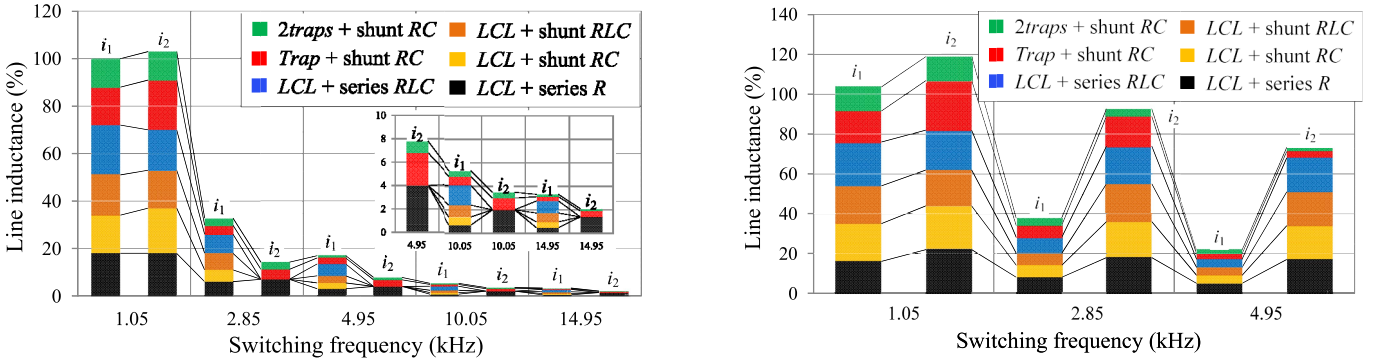
The capacitance values are illustrated in Fig. 10(c). No additional damping circuit ratings or trap inductors ratings are given, since these ratings are typically small compared with the main filter components, as it will be shown in Section V-D. In addition, the passive damping loss gives a good indication about the damping resistor ratings and practicability of the damping circuit. The total stored energy in the inductive filter components is shown in Fig. 10(d) in order to evaluate the size of each passive filter. Compared to the LCL filter, the trap filter can provide 20%∼40% reduction in size for switching frequencies above 2.5 kHz. The 2*traps* configuration can reduce the filter size up to 70% depending on the operating condition. The size of the other passive filters is within ±20% range. In addition, passive damping does not influence the size of the overall filter by more than 10%.

D. Passive Damping Performance

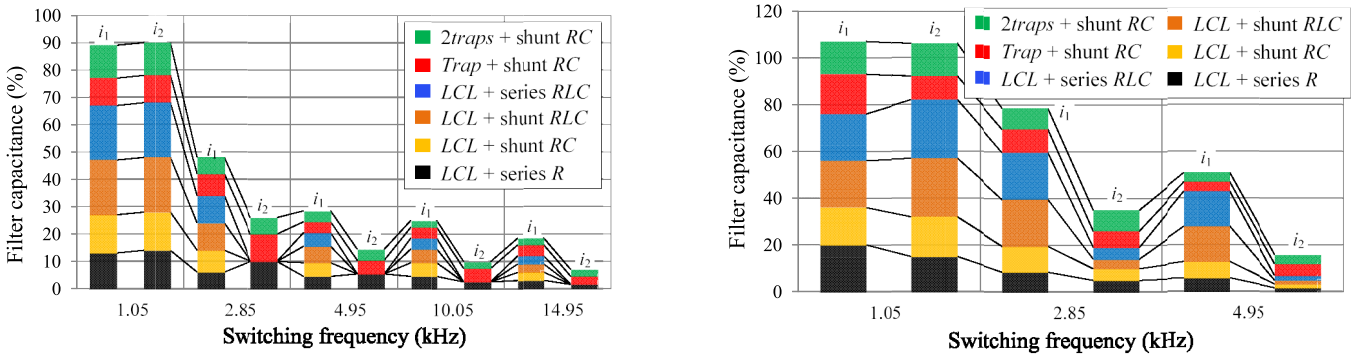
Another important evaluation which cannot directly be drawn from the above analysis is that the series and shunt RLC damping circuits provide more design freedom in the selection of parameters. For example, if more resonance attenuation is required, then it is possible to configure the filters in such a way to obtain low damping loss, which is not the case with the shunt RC damper and the series R damper case. Furthermore, for the BDEW standard it is more difficult to obtain good dynamic performance and to ensure low sensitivity gains.



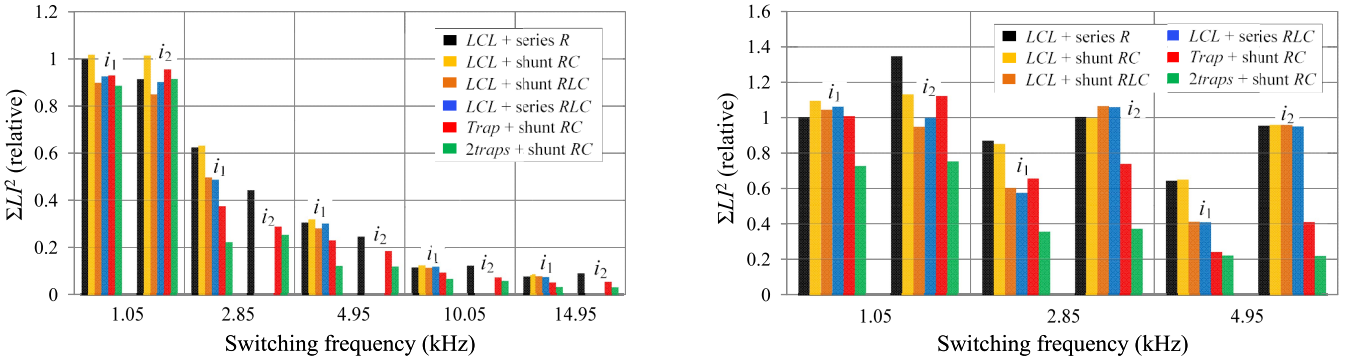
(a) IEEE 1547 (left) and BDEW (right)



(b) IEEE 1547 (left) and BDEW (right)



(c) IEEE 1547 (left) and BDEW (right)



(d) IEEE 1547 (left) and BDEW (right)

Fig. 10. Filter size evaluation for converter (i_1) and grid current control (i_2) by (a) ripple inductance, (b) line inductance, (c) total capacitance, and (d) total relative stored energy in inductors (relative to the LCL + series R damper, converter current control and $f_s = 1.05$ kHz).

To illustrate the performance of different passive dampers, the power loss in the damping resistor and current controller specifications are shown in Table III by varying the quality factor of the filters. Since the quality factor of the filters as given in (8) depends on all the filter components, the influence of the filter component tolerance on the specific

TABLE III
PASSIVE DAMPING EVALUATION AND CURRENT CONTROLLER SPECIFICATIONS

Damping topology	Q [relative]	$Y_{ol,2}$ [dB]		PM [deg]		GM [dB]		Bw [Hz]		P_d [%]	
		C_{high}	C_{low}	C_{high}	C_{low}	C_{high}	C_{low}	C_{high}	C_{low}	C_{high}	C_{low}
LCL + Series *R* C_{high}=15%; C_{low}=1.6%.	Q = 0.03	3.65	12.1	89.5	65.3	8.32	5.92	418	1419	0.11	0.0084
	Q = 0.15	-3.28	1.4	89.5	65.2	8.33	6.01	258	1322	0.53	0.041
	Q = 0.3	-7.2	-3.5	89.5	65.2	8.36	6.17	239	1181	1.05	0.0831
	Q = 0.45	-9.2	-6	89.5	65	8.41	6.33	227	1069	1.57	0.123
LCL + Shunt *RC* C_{high}=17% C_{low}=1.65%	0.1 Q_{opt}	4.7	14.5	89.3	65.2	7.96	5.75	394	1407	0.08	0.0045
	0.5 Q_{opt}	0	6.5	89	65.2	8	5.88	378	1391	0.34	0.011
	Q_{opt}	-1.2	4.65	89.3	65.2	8.1	6.08	294	1412	0.61	0.016
	1.5 Q_{opt}	-0.8	5.4	89.3	65.1	8.2	6.24	265	1444	0.87	0.022
LCL + Series *RLC* C_{high}=25% C_{low}=2%	0.1 Q_{opt}	3.2	10.9	88.8	64.8	7.11	4.57	344	1268	0.15	0.006
	0.5 Q_{opt}	-3.8	0	88.8	64.7	6.97	4.54	298	1180	0.11	0.0053
	Q_{opt}	-5.8	-3	88.8	64.7	6.75	4.14	263	1056	0.067	0.003
	1.5 Q_{opt}	-5.3	-2.5	88.8	64.7	6.62	3.75	254	992	0.05	0.0024
LCL + Shunt *RLC* C_{high}=25% C_{low}=1.65%	0.1 Q_{opt}	4.1	12.8	88.9	65.2	7.31	5.75	355	1402	0.08	0.005
	0.5 Q_{opt}	-1.9	3.5	88.9	65.2	7.18	5.82	320	1365	0.05	0.004
	Q_{opt}	-3.5	1.45	88.9	65	7.1	5.87	294	1358	0.03	0.0025
	1.5 Q_{opt}	-2.9	2.3	88.9	65.2	7.8	5.85	288	1404	0.02	0.002
Trap + shunt *RC* C_{high}=10% C_{low}=5%	0.1 Q_{opt}	3.95	9.2	90	66	9.13	7.87	208	900	0.25	0.52
	0.5 Q_{opt}	-1.3	-0.7	90	66	9.23	7.9	206	876	0.28	0.234
	Q_{opt}	-2.65	-2.6	90	66	9.23	8	204	843	0.42	0.18
	1.5 Q_{opt}	-2.18	-2	90	66	9.23	8.13	201	819	0.58	0.178
2*traps* + shunt *RC* C_{high}=14% C_{low}=4%	0.1 Q_{opt}	3.77	10.3	90.17	66.3	9.37	8.56	199	771	0.62	0.035
	0.5 Q_{opt}	-1.67	0.68	90.1	66.3	9.37	8.56	198	769	0.27	0.031
	Q_{opt}	-3.07	-1.2	90.2	66.3	9.4	5.59	196	763	0.44	0.035
	1.5 Q_{opt}	-2.67	-0.5	90.2	66.3	9.44	8.64	194.6	756	0.63	0.052

topology can also be assessed by varying the quality factor. To take into account the influence of the filter capacitance value on the damping loss, two scenarios are considered. One is referred to as a high capacitance scenario (C_{high}) and uses the results calculated for 1.05-kHz switching frequency and BDEW specifications. The low capacitance scenario (C_{low}) uses the results simulated for 4.95 kHz switching frequency and the same harmonic recommendations.

In Table III is shown how the series *R* and shunt *RC* dampers are limited for the use in high damping situations. The controller bandwidth information can be used to design the range of harmonic compensators, which can suppress the low-order current harmonics that corresponds to voltage background distortion from the utility grid. In addition, the current harmonic order, that can be compensated from the control system, can be increased to the resonance frequency of the filter if a virtual *RC* damping control scheme is adopted in the current controller [72].

VI. EXPERIMENTAL RESULTS

In order to demonstrate the previous design considerations, the passive filters have been designed for an 11 kW–10 kHz three-phase power converter. The setup used for experimental validation is illustrated in Fig. 11 and comprises a Danfoss FC302 inverter, which is controlled through a dSPACE 1007 platform using P+R current controllers [73]. The dc-link voltage is kept constant from a Yaskawa active rectifier to 700 V. Hence, no dc voltage control loop is used.

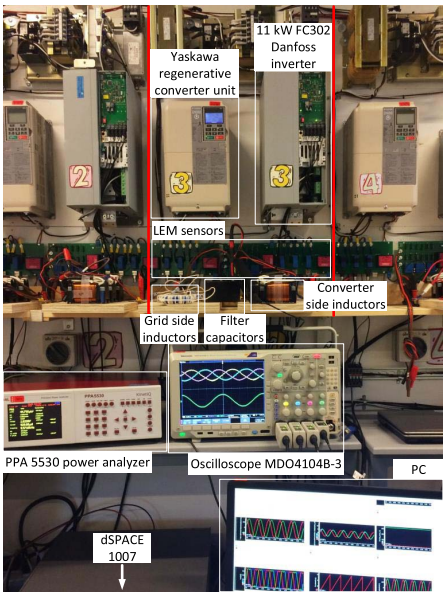


Fig. 11. Experimental hardware setup used for the evaluation of different passive filters.

The experimental setup is connected to a 400 V (line to line voltage), 50 Hz power grid.

The power loss in the resistor and the switching harmonics attenuation are measured using a Newton 4th power analyzer (PPA 5530) and presented in Table IV. In Table V, the ratings of the designed passive filters are illustrated.

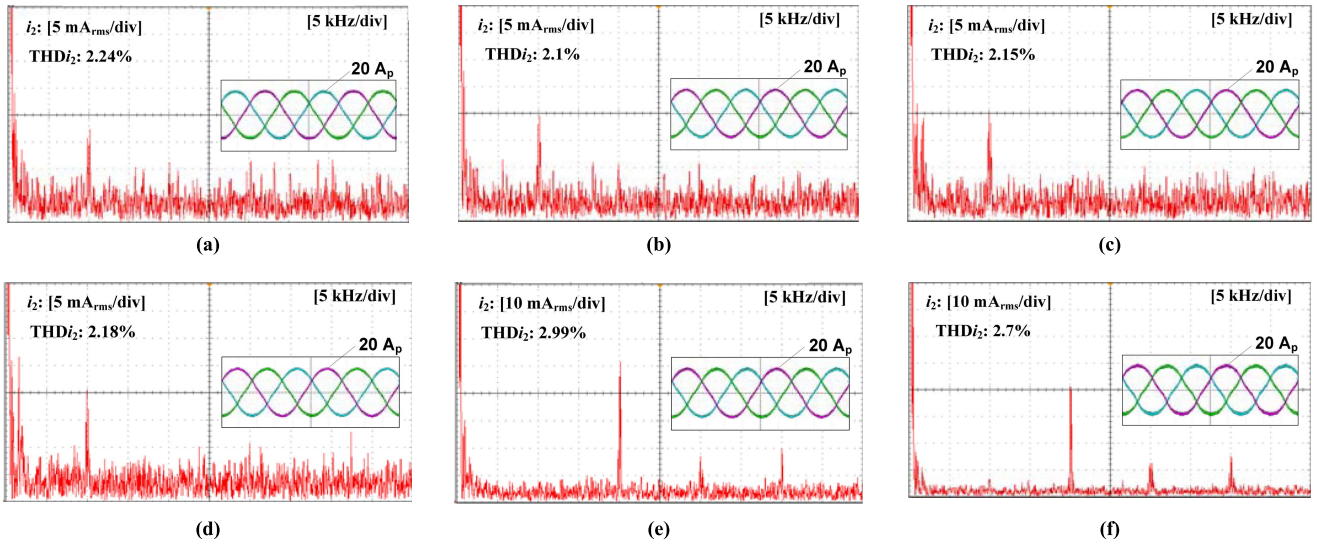


Fig. 12. Harmonic spectrum of the grid current for the selected passive filters topologies. (a) LCL + series R. (b) LCL + shunt RC. (c) LCL + shunt RLC. (d) LCL + series RLC. (e) Trap + shunt RC. (f) 2traps + shunt RC.

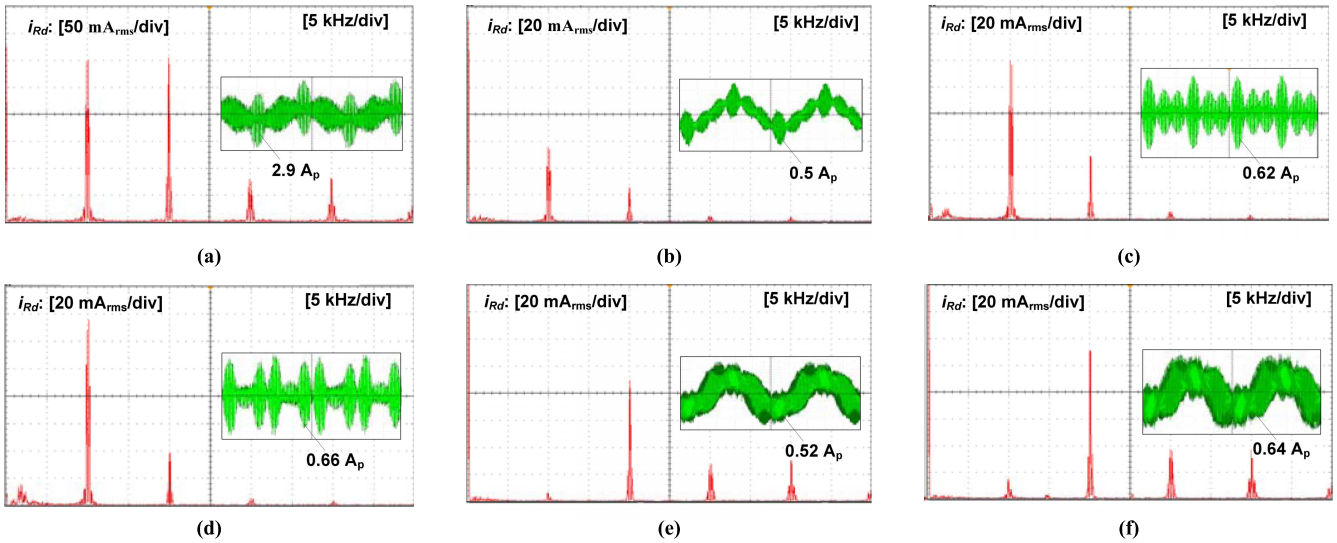


Fig. 13. Harmonic spectrum of the damping current for the selected passive filters topologies. (a) LCL + series R. (b) LCL + shunt RC. (c) LCL + shunt RLC. (d) LCL + series RLC. (e) Trap + shunt RC. (f) 2traps + shunt RC.

The grid current waveform and the corresponding harmonic current spectrum are illustrated in Fig. 12. There is no significant difference in the THD of the grid current for the selected passive filters under rated conditions. In rated conditions, the THD is equal to the total demand distortion (TDD).

The power losses in damping resistor can vary by a factor 10, depending on the filter topology. In Fig. 13, the current in the damping resistor is demonstrated at rated conditions. It can be seen that the fundamental current and high-frequency current is very limited for the shunt and series RLC dampers according to the aforementioned analysis. For the series R and shunt RC dampers, the current in the damping resistor is reflected by the value of capacitance and resistors. If the resistance dominates the shunt impedance of the filter, then the damping current will be more sinusoidal and higher damping loss will occur. The power loss mismatch in the damping resistor between the simulated and the measured values shown in Table IV is related to the damping that exists in the filter and in the grid impedance (more damping exists in the real system than simulated).

TABLE IV
EVALUATION OF SWITCHING HARMONICS ATTENUATION AND POWER LOSS IN DAMPING RESISTOR

Filter Topology	Simulated Power loss (%)	Measured Power loss (%)	Meas. harmonic current, $I_{mf\text{-}2}$ (%)
LCL + series *R*	0.197	0.12	0.144%
LCL + shunt *RC*	0.062	0.045	0.192%
LCL + shunt *RLC*	0.0455	0.028	0.182%
LCL + series *RLC*	0.032	0.011	0.165%
Trap + shunt *RC*	0.0581	0.03	0.048%
2*traps* + shunt *RC*	0.0094	0.03	0.042%

TABLE V
PASSIVE FILTERS COMPONENT RATINGS USED IN EXPERIMENTS (Ap: AMPERE PEAK, Vp: VOLT PEAK, Wp: WATT PEAK)

Filter Topology	Converter Side Inductor		Line Inductor		Filter Capacitors		Damp. Resistor		Damp. Inductor		Damp. Capacitor		Trap Inductors	
	Ap	mH	Ap	mH	Vp	μF	Wp	Ω	Ap	mH	Vp	μF	Ap	mH
LCL + series *R*	22.5	1.5	21	1.5	330	4.7	85	5.5	-	-	-	-	-	-
LCL + shunt *RC*	22.5	1.5	21	1.6	330	2.35	20	41.4	-	-	330	2.15	-	-
LCL + shunt *RLC*	22.5	1.5	21	1.5	330	2.35	14	20	0.35	3.3	330	2.15	-	-
LCL + series *RLC*	22.5	1.5	21	1.5	330	4.7	10	6.2	0.75	0.62	8	5.6	-	-
Trap + shunt *RC*	22.5	1.5	21	0.7	330	2.15	25	20	-	-	330	2.35	3	0.113
2*traps* + shunt *RC*	22.5	1.5	21	0.1	330/380	2.15/0.21	8	5.4	-	-	330	2.35	2.8/1.4	0.113/0.3

TABLE VI
MAIN FEATURES OF PASSIVE FILTERS

Filter Topology	Advantages	Disadvantages	Applications
LCL + series *R*	1) Simple design and implementation	1) Decreased high frequency attenuation 2) High damping loss for high capacitance and/or high resonance damping	Low power
LCL + shunt *RC*	1) Lower damping loss 2) Good high frequency attenuation	1) High damping loss for high capacitance and/or high resonance damping	Low power
LCL + shunt *RLC*	1) Lowest damping loss for high resonance damping 2) Good high frequency attenuation	1) More difficult to implement 2) Requires additional low rated damping inductance (high inductance/low current)	High power
LCL + series *RLC*	1) Lowest damping loss for high resonance damping 2) Good high frequency attenuation	1) More difficult to implement 2) Requires additional low rated damping inductance (low inductance/high current)	High power
Trap + shunt *RC*	1) Low filter size and cost	1) Decreased high frequency attenuation 2) More difficult to implement 3) Increased power loss 4) Susceptible to de-tuning	Low and high power
2*traps* + shunt *RC*	1) Lowest filter size and cost	1) Decreased high frequency attenuation 2) More difficult to implement 3) Highest power loss due to high ripple content 4) Susceptible to de-tuning	Low and high power

By changing the operating mode of the inverter from rated to light-load or no-load conditions, the TDD of the grid current from Fig. 12 will improve slightly depending on the adopted magnetic materials of the filter inductors. The filter inductance will increase by decreasing the output current due to the permeability decrease of magnetic materials [35], which causes less current ripple in light-load conditions. This effect is less significant for high power applications where the operating switching frequencies are relatively low and the laminated steel is most likely to be adopted for the power inductors (in this case, the permeability dependence with dc bias is relatively constant). The passive damping losses will also decrease slightly with decreasing the output current in applications that uses power inductors designed with powder compounds materials.

VII. CONCLUSION

In this paper, several passive filters are reviewed in terms of stored energy in the passive components, damping capability and power loss in the damping circuit. The passive filters are designed to have the same attenuation of the switching harmonic content. The damping circuit is designed to keep about the same resonance attenuation by using the maximum peak criteria (in order to ensure same dynamic performance). Although passive damping itself does not increase the size of the filter significantly, it may increase the power loss in the damping circuit to unacceptable levels, especially in cost/size optimized filters. Therefore, depending on the passive damping solution and the operating conditions, the size and cost of the filter can be much different.

To guarantee low size of the filter and to ensure desired dynamic performance, in the case of the converter current feedback, the ripple inductance is chosen higher than the line inductance, while the capacitance is chosen as minimum as possible in order to limit the damping loss. For the grid current feedback, the filter inductances are kept around the same value while the capacitance value is again limited. The only exceptions are the series and shunt *RLC* damping

circuits, which allow an increased capacitance size in the filter due to close-to-zero damping loss. Such advantages can be obtained from the fact that the series and shunt RLC damping circuits provides more design freedom in the choice of parameters, because of the additional resonant circuit. For example, if more resonance attenuation is required from the filter, then it is possible to configure the filters in such a way to obtain low damping loss, which is not the case with the series R and shunt RC passive dampers. The highest damping loss (around 0.4%) is obtained for low operating switching frequency. With increasing the operating switching frequency, the damping losses hardly exceed 0.1%. A summary of the reviewed passive filters topologies is presented in Table VI.

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