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Pulse Pattern Modulated Strategy for Harmonic Current Components Reduction in Three-Phase AC-DC Converters

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***Abstract* -- Generated harmonic current as a consequence of employing power electronics converter is known as an important power quality issue in distribution networks. From industry point of view complying with international standards is mandatory, however cost and efficiency are two other important features, which need to be considered in order to be competitive in the market. Therefore, having a flexibility to meet various requirements imposed by the standard recommendations or costumer needs is at most desirable. This makes the generated harmonic current mitigation a challenging task especially with three-phase diode bridge rectifier, which still is preferred in many power electronic systems. This paper addresses a novel current modulation strategy using a single-switch boost three-phase diode bridge rectifier. The proposed method can selectively mitigate current harmonics, which makes it suitable for different applications. The obtained results at experimental and simulation levels verify and confirm the robustness of the proposed approach.**

***Index Terms*--Selective harmonic mitigation, three-phase rectifier, current control, modulation, electronic inductor.**

I. INTRODUCTION

AC to DC conversion is an inevitable stage in most power electronic systems, but it is responsible for generating line current harmonics especially if the conventional topologies such as six-pulse diode rectifier are employed. The level of generated current harmonics of this conversion stage is of significant importance as it can easily deteriorate the supply network quality [1]-[6]. Although the power electronics technology has brought new insight in many applications, however controlling their generated harmonics at certain levels is not achievable without additional cost and circuitry.

The basic topology for AC to DC conversion has started by utilizing a diode bridge rectifier due to many reasons such as simplicity, reliability, robustness, and being cost-effective compared to other complex systems such as active front end systems. However, the diode rectifiers impose a higher level of line current harmonics. Over the past years, many approaches have been studied and introduced from absolutely passive up to fully active methods [1], [4]-[10]. A majority of these methods have targeted pure sinusoidal waveform generation, and as a consequence cost and complexity have been significantly increased. Of course having a low Total Harmonic Current Distortion (THD_i) improves the system efficiency but this is of interest for specific applications such as space and airborne industry, where the cost of the power converter is not the main concern. But with most applications such as industrial Adjustable Speed Drives (ASDs), switch mode power supplies, home appliances and etc, the key of success is to perform a trade-off between efficiency and cost since many manufacturers are competing in the market. Therefore, as long as the power electronic system complies with the recommended standards there is no need to obtain a pure sinusoidal current waveform. Moreover, due to the cost, power density and components limited power ratings many of the prior-art approaches are not applicable at medium and high power levels.

With the rapid growth of power electronics applications, the standard recommendations such as IEC61000 are continuously updating and becoming more stringent. In addition, the demands on various power level and costumer needs are extending. These bring the absolute interest of having a flexible system which can be adapted with varied situation as it can reduce the cost of the system significantly.

This paper proposes a novel current modulation strategy to reduce low order harmonic current components. The objective of the proposed method is to address a flexible selective harmonic mitigation technique suitable for various applications. One of the main aims in this study was to apply an active filtering method as an intermediate circuit to the conventional three-phase diode-rectifier. This way, no major modifications is required for the systems which are equipped with the three-phase diode rectifier. Therefore, the proposed current modulation strategy is applied to a single-switch boost topology operating in Continuous Conduction Mode (CCM). Considering this situation its only counterpart harmonic mitigation methods with boost capability which are applied to the conventional diode rectifier are Δ-rectifier and boost converter operating in Discontinuous Conduction Mode (DCM) [5]. The Δ-rectifier principle is based on phase-modular Power Factor Correction (PFC), meaning that three-phase diode rectifiers with boost converter at their DC-links are applied to each phase. Its advantage is ability to significantly improve the input current quality; however the

main drawback of this topology is the presence of high number of power switches, high complexity and lower efficiency comparing with a single-switch boost converter. The DCM single-switch boost converter requires three inductors at the AC-side of the diode rectifier. More importantly this topology suffers from the large EMI (Electromagnetic Interference) filtering effort (i.e., due to the DCM operation) and for effective harmonic mitigation its output voltage should be boosted above 1 kV (i.e., for grid phase voltages of 220 or 230 Vrms) [5].

This paper is structured as follows. Section II provides detailed analysis of selective harmonic mitigation using the proposed current modulation strategy. In Section III, practical design considerations with respect to the boost inductor and modulation signal generation are pointed out. The obtained experimental results that are summarized in Section IV validate the performance of the proposed method. Section V recalls a brief overview on the perspectives of the proposed method in multi-pulse rectifier systems based on comparative numerical simulation results. Finally, concluding remarks are given in Section VI by highlighting the main achievements and providing suggestions for further studies.

II. Proposed Current Modulation Strategy

A. *Principle of the Proposed Method*

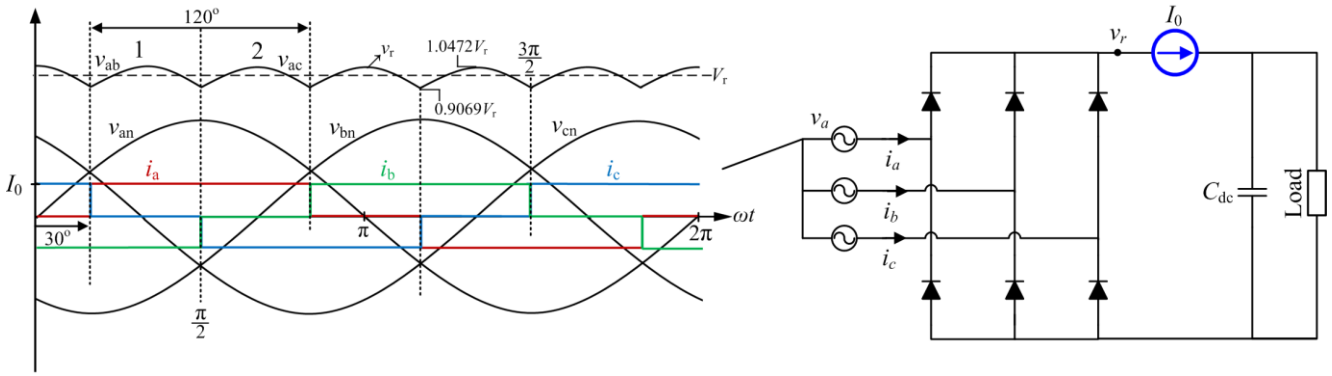
In order to understand the basic principle of the proposed method, let's first consider the circuit diagram depicted in Fig. 1. As it can be seen, the current source at the DC-link side of the rectifier draws a constant current which is equal to I_0. Therefore, the input current will be a square-wave with 120 degrees conduction due to the fact that at each instant of time only two phases conduct and circulate DC-link current through the main supply. Due to the nature of a three-phase system (120° phase shift), the corresponding phase shift for any triple harmonic would be a multiple of 360° and since the currents at each instant are identical with opposite amplitude, the sum of line currents i_a, i_b, and i_c is zero at all instants of time, which makes them to be free from triple harmonics in a balanced system. The currents are also void of even harmonics because of the half-wave symmetry of the waveforms which as a matter of fact makes the most prominent harmonics in this system to be the fifth, seventh, eleventh, and thirteenth [11].

The proposed idea is based on adding (or subtracting) phase-displaced current levels to the square-wave current waveform in order to manipulate the current harmonic components [12], [13]. To keep the above mentioned properties (free of triple and even harmonics) the new added pulse should be repeated 1/6 of the period. For instance, Fig. 1 depicted two sectors of 1 and 2, where at each sector i_a is circulated through one of the other phases current. Now, if the new level is added at sector 1 it should be exactly repeated in sector 2 (see Fig. 2(a)). This means that the frequency of the added pulse at the DC-link should be six times of the fundamental frequency so it can be repeated at each phase current.

Fig. 2(a) illustrates detailed analysis of the proposed idea for only one new level added to a constant square wave. As can be seen the proposed current waveform is comprises of three square-wave signals with different magnitudes and pulse widths. The first current waveform has the magnitude of I_0 with the conduction phase angle of 30°, which is defined based on the normal operating modes of a three-phase diode rectifier and the conduction phase angle cannot be altered. The second current waveform has the magnitude of I_1 with the conduction phase angle of α_1. The third current waveform has the magnitude of I_1 but with a different conduction phase angle (α_{11}). These current waveforms can be analyzed based on a periodic square-wave Fourier series in which the fundamental input current magnitude and its harmonics can be calculated as follows:

$$i_n = \frac{4}{n\pi}\left[I_0\cos(n30) + I_1\cos(n\alpha_1) - I_1\cos(n\alpha_{11})\right] \qquad (1)$$

Equation (1) shows that the fundamental current can be



(a) (b)

Fig. 1. Simplified circuit diagram of a three-phase diode rectifier with a controlled DC-link current, (a) ideal three-phase input currents, (b) systems schematic.

defined by selecting the variables I_0, I_1, α_1 and α_{11} but a main consequence will be on harmonic magnitudes. According to the line current waveform depicted in Fig. 2(a) the following condition should be valid:

$$\alpha_{11} = \frac{\pi}{2} - \beta, \quad where \quad \beta = \alpha_1 - \frac{\pi}{6} \tag{2}$$

Considering (1) and (2) and having α_1 and α_{11} as the switching angles, up to two selected low order harmonics (i_h and i_j) can be cancelled out. The mathematical statement of these conditions can be expressed as (3). This is a system of three transcendental equations with three unknown variables I_0, I_1, α_1:

$$\begin{aligned} i_1 &= \frac{4}{\pi}\left[I_0 \cos\left(\frac{\pi}{6}\right) + I_1 \cos(\alpha_1) - I_1 \cos\left(\frac{2\pi}{3} - \alpha_1\right)\right] = M_a \\ i_h &= \frac{4}{h\pi}\left[I_0 \cos\left(h\frac{\pi}{6}\right) + I_1 \cos(h\alpha_1) - I_1 \cos\left(h\left(\frac{2\pi}{3} - \alpha_1\right)\right)\right] = 0 \\ i_j &= \frac{4}{j\pi}\left[I_0 \cos\left(j\frac{\pi}{6}\right) + I_1 \cos(j\alpha_1) - I_1 \cos\left(j\left(\frac{2\pi}{3} - \alpha_1\right)\right)\right] = 0 \end{aligned} \tag{3}$$

The proposed method can be further extended to a multilevel current waveform. Fig. 2(b) illustrates a generalized pulse modulated current waveform, where m is the number of switching angles. By extending (3) and using Fourier series, the amplitude of any odd n^{th} harmonic of the stepped current waveform can be expressed as:

$$i_n = \frac{4}{\pi}\left(I_0 \cos\left(n\frac{\pi}{6}\right) + \frac{1}{n}\sum_{k=1}^{m}\left[I_k \cos(n\alpha_k) - I_k \cos\left(n\left(\frac{2\pi}{3} - \alpha_k\right)\right)\right]\right) \tag{4}$$

According to Fig. 2(b), α_1 to α_m must satisfy the following condition:

$$\frac{\pi}{6} < \alpha_1 < \alpha_2 < \alpha_3 < \cdots < \alpha_m < \frac{\pi}{2} \tag{5}$$

From (5) it can be seen that the degree of freedom in manipulating the current waveform is only 60^o, which makes the control of the harmonic components a difficult task. Therefore, to give more flexibility to (4) the new added levels should not necessarily have same amplitude. In addition, the amplitude could be positive or negative, which totally depends on the targeted harmonics and the desired modulation index M_a (fundamental harmonic content). As the equations are nonlinear, numerical solutions are required to find proper values for these variables.

B. Optimum Harmonic Reduction

To target more harmonic components the number of the current levels need to be increased, but on the other hand it reduces the feasibility of practical implementation since the new added levels and switching angles depends on the tracking performance of the power electronics unit and its controller. Therefore, in order to keep the number of the added current levels to minimum while obtaining desirable outcome an optimization needs to be performed. The basic principle of the applied optimization is to consider the maximum permissible harmonic levels allowed by the application or the grid code. In other word, instead of fully nullifying, the harmonic components could be reduced to acceptable levels by adding suitable constraints (L_n) to the set of the above mentioned equations. The problem is now described as an optimization function (F_n) that searches a set of α_m and I_m values over the allowable intervals.

$$\begin{aligned} F_1 &= M_a - |i_1| \le L_1 \\ F_n &= \frac{|i_n|}{|i_1|} \le L_n, \quad \text{where} \quad n = 5,7,11,13,\cdots \end{aligned} \tag{6}$$

Based on (6) an objective function needs to be formed to obtain a minimum error. The objective function (F_{obj}) plays an important role in leading the optimization algorithm to the suitable set of solution. Here F_{obj} is formed based on squared error with more flexibility by adding constant weight values

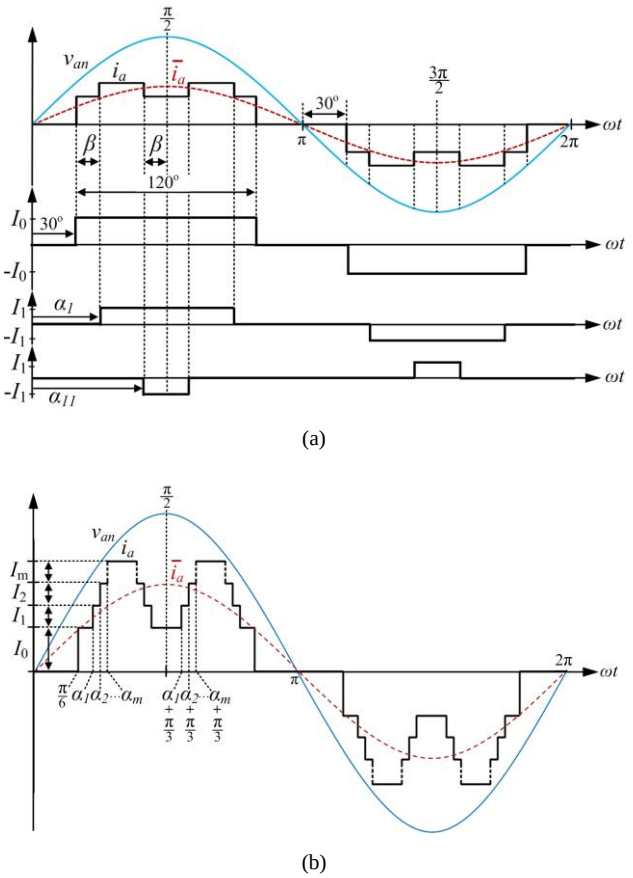


Fig. 2. Detailed analysis of the proposed current modulation technique with: (a) one new added level, (b) generalized *m*-level pulse modulated.

(W_n) to each squared error function [14]. The value of the W_n in the objective function prioritized the included functions as follows:

$$F_{obj} = \sum W_n \cdot \left(F_n - L_n\right)^2, \quad \text{where} \quad n = 1,5,7,11,13,\cdots \quad (7)$$

III. Implementation Details and Hardware Setup

To control the DC-link current shape and magnitude following the waveforms shown in Fig. 2, a boost converter topology based on electronic inductor [12], [13], [15]-[19] concept is employed. Fig. 3 depicts the overall system structure and the implemented hardware setup. Using the conventional boost topology has the advantage of boosting the output DC voltage which is suitable when the DC-link is fed to an inverter. Moreover, as the DC-link current is controlled based on the load power it has the advantage of keeping the THD_i independent of load profile.

Fig. 3(b) shows the implemented prototype. Here, one SEMIKRON-SKD30 was used as a three-phase bridge rectifier and one SEMIKRON-SK60GAL125 IGBT-diode module is employed in the boost topology. A Texas Instrument TMS320F28335 is used for control purposes and LEM current and voltage transducers are used as measurement unit.

To synchronize the current controller with the grid a Second-Order Generalized Integrator (SOGI) based phase locked loop (PLL) system is adopted [20]. As Fig. 3(a) depicted, for the simplicity, one line-to-line voltage is fed to the PLL and therefore the result will have 30° phase shift regarding to the phase voltage, which should be corrected within the reference current generator algorithm. In order to obtain a discrete-time integrator for PLL and PI controller, the trapezoidal discretization method is used.

A. Boost Inductor

Selection of the boost inductor is a challenging task as it contributes to the system loss, power density and current ripple. To better understand this, the inductor current in a steady-state CCM is analyzed. Here the switching frequency is considered to be high enough so that the rectified voltage and output voltage are constant during one switching cycle. Therefore, the inductor value can be calculated as,

$$L_{dc} = \frac{V_o D(1-D)}{f_{sw,avg}\Delta I_{L,pk-pk}} \quad \textit{where} \quad f_{sw,avg} = \frac{1}{T_{sw}} = \frac{1}{T_{on}+T_{off}} \quad (8)$$

where V_o is the output voltage, $f_{sw,avg}$ is the average switching frequency, $\Delta I_{L,pk\text{-}pk}$ is the peak to peak inductor current ripple and D is the steady-state duty cycle of the boost converter. Using (8) the minimum required switching frequency ($f_{sw,avg}$) can be selected by considering the maximum peak to peak inductor current ripple (D = 0.5) as,

$$f_{sw,avg} \geq \frac{V_o}{4L_{dc}\Delta I_{L,pk-pk,\max}} \quad (9)$$

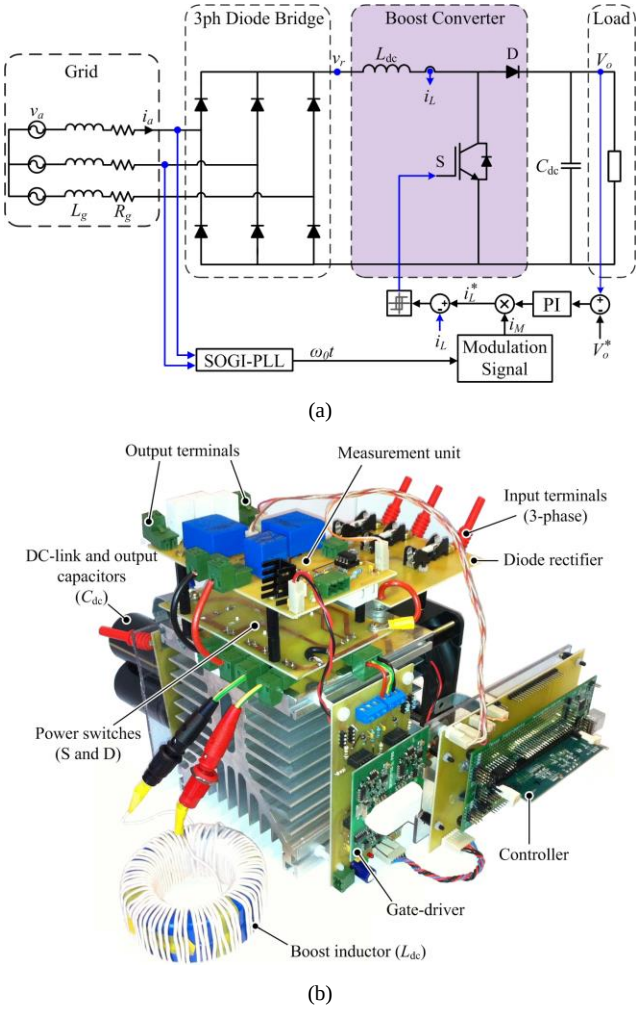


Fig. 3. The implemented three-phase AC-DC system with the proposed selective harmonic elimination method, (a) overal system schematic and control structure, (b) photograph of the implemented hardware setup.

Following (8) and (9) the optimum switching frequency can be selected by making a tradeoff among the system efficiency, size and cost [21]. For example the system efficiency can be optimized by minimizing the switching frequency by allowing more ripple current for high power applications and it will result in lower switching losses.

As mentioned before the THD_i can be independent of the load profile. Equation (10) can be rewritten based on the output average current as

$$L_{dc} = \frac{V_o D(1-D)^2}{f_{sw,avg} k_{ripple} I_{out}} \text{ where } k_{ripple} = \frac{\Delta I_{L,pk-pk}}{I_L} = \frac{\Delta I_{L,pk-pk}(1-D)}{I_{out}} \quad (10)$$

with k_{ripple} being the peak-to-peak ripple factor, I_L the average inductor current and I_{out} the average output current. Hence, keeping the ripple factor as a constant value will make the input current quality independent of the load profile. However, careful selection of the ripple factor is needed as it

has direct impact on the ripple current, which as stated in (9) can affect the inductor size, system efficiency and cost [21].

Depending on the application requirement the converter may operate in partial loading conditions such as in ASD applications. In partial loading condition the DC-link current i_L can become discontinuous which adversely affect the harmonic reduction performance of the proposed method. However, by suitable selection of the converter parameters, the converter can cover wide range of loading conditions. Therefore, in order to guarantee CCM operation of the converter the parameters (i.e., f_{sw}, L_{dc}, ΔI_L) should be calculated based on the minimum intended output power. This condition based on Boundary Condition Mode (BCM) operation ($I_L = \Delta I_{L,pk\text{-}pk}/2$) is,

$$L_{dc} > \frac{D(1-D)^2 V_o^2 K}{2 f_{sw,avg} P_{O\,min}} \quad with \quad K = \begin{cases} \left(1 + r_M - \dfrac{6\beta}{\pi} r_M\right) & \alpha_1 < 60^o \\ 1 & \alpha_1 = 60^o \\ \left(\dfrac{\pi(1 + r_M - 6\beta r_M)}{\pi(1 - r_M)}\right) & \alpha_1 > 60^o \end{cases} \tag{11}$$

with r_M being the ratio between the calculated current levels $r_M = I_1/I_0$, and K a coefficient factor which depends on the applied modulation type as depicted in Fig. 4. As it can be seen from Fig. 4, three different modulations can be considered. The first type is when a new current level is added to the square-wave waveform (i.e., $\alpha_1 < 60^o$). The second type is conventional square-wave (i.e., $\alpha_1 = 60^o$). The third type is when a new current level is subtracted from the square-wave current (i.e., $\alpha_1 > 60^o$). In order to guarantee the CCM operation the minimum applied current level should be considered. This condition is reflected using the calculated K factor in (11). Therefore, considering the minimum intended output power level the converter parameters should be selected based on the applied current modulation type. For instance under same condition, the first and second types of modulation can operate in CCM operation at lower power levels comparing with the third modulation type which the current becomes discontinuous at higher power levels.

B. Modulation Signal

As Fig. 3(a) illustrates, the reference current is formed by multiplying the voltage controller output by a pre-programmed modulation signal. Fig. 5 depicts the basic concept in generating the modulation signal (i.e., i_M) following Fig. 2(a). As it can be seen, i_M can be generated based on the sum of absolute values of three-phase input currents. The illustrated switching parameters (i.e., I_0, I_1 and α_1) at both grid side and DC-link currents helps to better understand this relation. As it can be seen the period of the modulation signal i_M is 1/6 of the input currents i_{abc}. Therefore, the simplest way to generate and synchronize the modulation signal inside the controller is to compare it with a sinusoidal signal (i.e., $|\sin(3\omega_0 t)|$) using the PLL estimated angular frequency (ω_0). Comparing the switching angles with

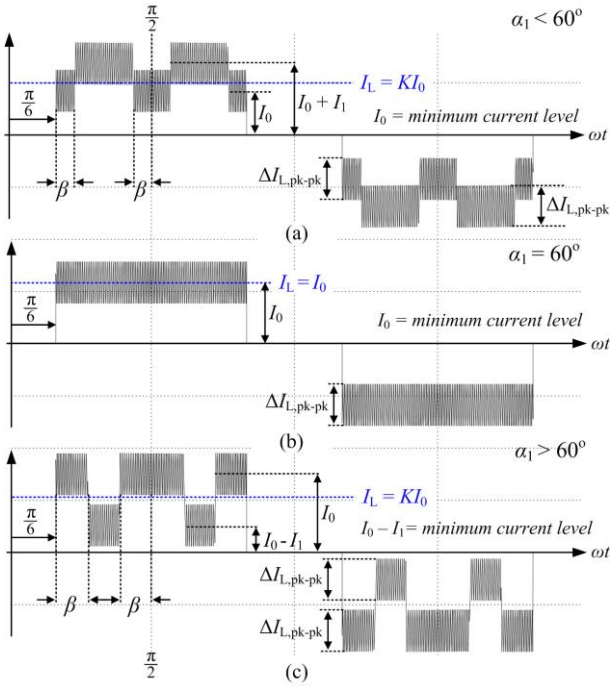


Fig. 4. Detailed analysis of the three different modulation types: (a) proposed current modulation with one new added level, (b) conventional flat current modulation, (c) proposed current modulation with one new subtracted level.

the sinusoidal waveform yields the following simple conditions:

$$\alpha_1 < \alpha_{11}: \begin{cases} if\ (|\sin(3\omega_0 t)| > \sin(3\beta)) \\ i_M = I_0 + I_1 \\ else \\ i_M = I_0 \end{cases}$$
$$\alpha_1 > \alpha_{11}: \begin{cases} if\ (|\sin(3\omega_0 t)| > \sin(3\beta)) \\ i_M = I_0 - I_1 \\ else \\ i_M = I_0 \end{cases} \tag{12}$$

Here, based on the fact that the proposed method is adding or subtracting phase-displaced current levels, two conditions have been considered, which results in different modulation signals. It can be known from Fig. 2(a) that adding a phase-displaced current level requires to have $\alpha_1 < \alpha_{11}$. However to reduce a specific set of harmonic components, phase displaced current level needs to be subtracted. Therefore, for those situations α_1 should be set above α_{11} ($\alpha_1 > \alpha_{11}$). The above equation can easily be extended to multi-level situation by applying (12) to each switching parameters and summing up the corresponding modulation signals.

As it is mentioned, the reference tracking performance of the current controller has an important role in the harmonic mitigation performance. Therefore, the bandwidth of the

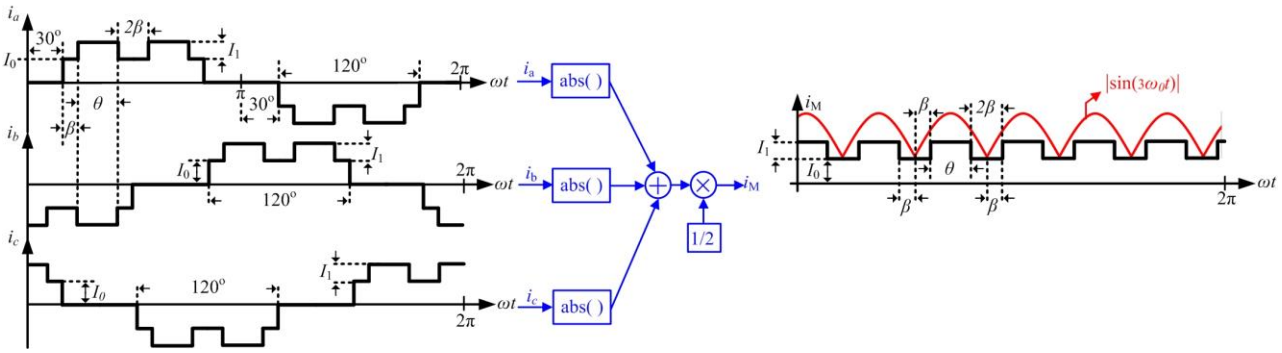


Fig. 5. Synthesis of the modulation signal (i.e., i_M) at the DC-link based on three-phase input currents.

current controller should be high enough to accurately follow the applied multi-pulse pattern modulation. For the traditional PWM-based PI current controller the control loop bandwidth needs to be less than 1/5 of the switching frequency (i.e., in the case of using Tustin or Trapezoidal discretization method). This may result in having a high switching frequency, which can either exceeds the power switching device limits or increase the switching losses. Hence, employing a fast current control method like hysteresis or dead-beat are recommended.

Here, the hysteresis current control method is used. Notably, using the hysteresis current control in the proposed method will not result in a well-known significantly dispersed frequency spectrum as the input voltage is a rectified voltage with a small ripple as shown in Fig. 1 (i.e., $0.9069V_r \le v_r \le 1.0472V_r$). Considering the boost converter CCM operation, steady-state duty cycle D and rectified voltage V_r, the switching frequency is changing within the following range,

$$\frac{(-0.0494+1.0966D)}{L\Delta I}V_r \le f_{sw} \le \frac{(0.0844+0.8225D)}{L\Delta I}V_r \quad (13)$$

To better understand this small variation, the considered system parameters in this paper (Table I) is applied to (8),

$$0.241\frac{V_r}{L\Delta I} \le f_{sw} \le 0.302\frac{V_r}{L\Delta I} \quad (14)$$

IV. Results

In this section the circuit operation and the proposed current modulation scheme are verified through different simulation and experiments using the implemented prototype (Fig. 3(b)). Here the flexibility of the proposed method by targeting different set of harmonic components is illustrated. The system parameters are listed in Table I. Notably, for all of the harmonic reduction cases, simulation results are also carried out to show its close agreement with the measured experimental results.

For the sake of comparison, the conventional square-wave (flat) current modulation has been considered as the first case. Fig. 6 shows both the simulated and obtained measured results along with the harmonic distribution of the input current at phase a.

TABLE I
Parameters of the System

Symbol	Parameter	Value
v_{abc}	Grid phase voltage	220 V_{rms}
f_g	Grid frequency	50 Hz
L_g, R_g	Grid impedance	0.18 mH, 0.1 Ω
L_{dc}	DC link inductor	2 mH
C_{dc}	DC link capacitor	470 µF
V_o	Output voltage	700 V_{dc}
K_p, K_i	PI controller (Boost converter)	0.01, 0.1
HB	Hysteresis band	2 (A)
P_{omax}	Rated output power	= 5 kW

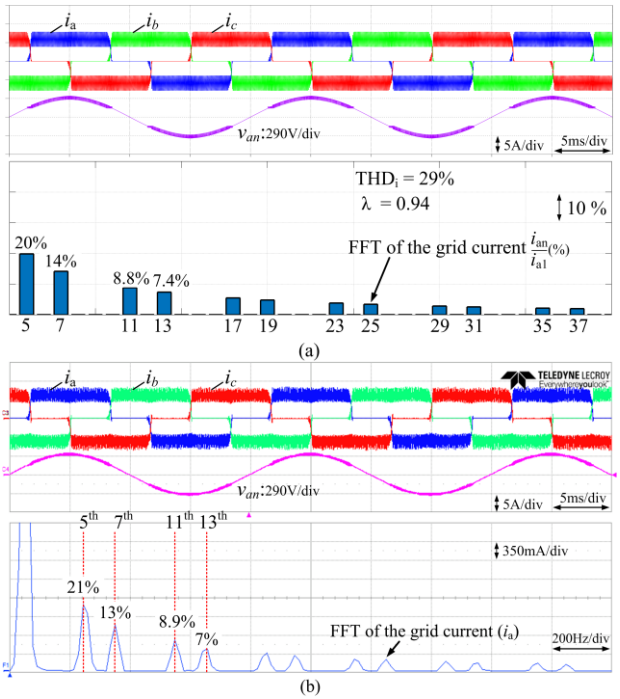


Fig. 6. Obtained results for sqaure-wave modulation using hysteresis current control at V_o = 700 V_{dc} and P_o = 3kW (P_o = 60%): (a) simulation results of three-phase input currents with Fast Fourier Transform (FFT) of the input current (i_a), (b) measured experimental results of three-phase input currents with FFT of the input current (i_a).

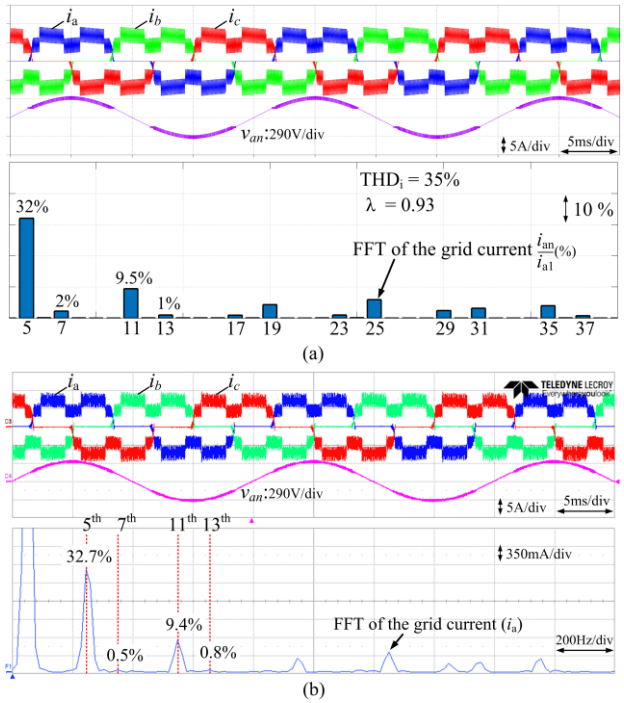


Fig. 7. Obtained results for the proposed 7th and 13th harmonics cancellation using hysteresis current control at V_o = 700 V_{dc} and P_o = 3kW (P_o = 60%): (a) simulation results of three-phase input currents with Fast Fourier Transform (FFT) of the input current (i_a), (b) measured experimental results of three-phase input currents with FFT of the input current (i_a). [with I_0 = 1, I_1 = 0.618, α_1= 42^o].

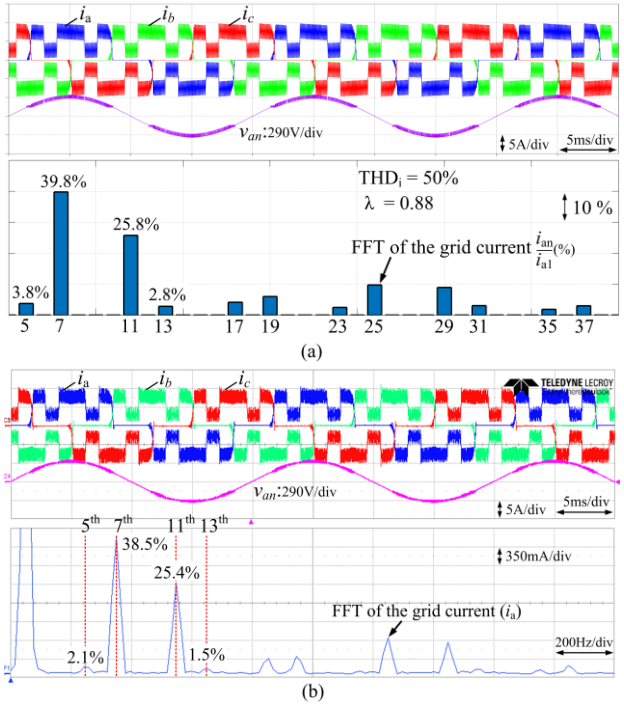


Fig. 8. Obtained results for the proposed 5th and 13th harmonics cancellation using hysteresis current control at V_o = 700 V_{dc} and P_o = 3kW (P_o = 60%): (a) simulation results of three-phase input currents with Fast Fourier Transform (FFT) of the input current (i_a), (b) measured experimental results of three-phase input currents with FFT of the input current (i_a) [with I_0 = 1, I_1 = 0.653, α_1= 70^o].

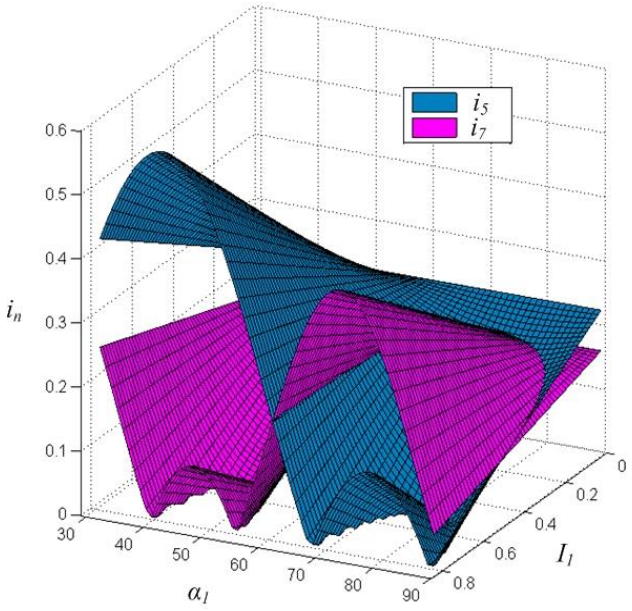


Fig. 9. Calculating input current 5th and 7th harmonics magnitude (normalized with I_0 = 1) versus switching angle α_1 (30^o< α_1 < 90^o), and new added current level I_1 (0 < I_1 < 0.8) for two-level current modulation (i.e., transition between first and third modulation types as illustrated in Fig. 4) at DC-link following (1), where zero magnitudes (i_n = 0) are the possible harmonic elimination solutions.

As the second case, adding one current level to the DC-link current was considered to target two low order harmonics. Hence, the cancellation of 7th and 13th harmonic orders have been considered by solving (3) using MATLAB function – "fsolve". Fig. 7 illustrates the obtained results. As it can be seen from Fig. 7, 7th and 13th harmonic components have been significantly reduced.

In the third case as depicted in Fig. 8, 5th and 13th harmonics have been targeted. However, the obtained results in Figs. 7 and 8 clearly show that the consequence of canceling 7th harmonic is the increase of the 5th harmonic order and vice versa. This results in higher THD$_i$ and power factor (λ) comparing with the conventional square-wave case. To better understand this relation, Fig. 9 illustrates the possible input current magnitudes regarding to both 5th and 7th harmonics orders as a function of switching angle (α_1) and new added current level (I_1) when a two-level current modulation is applied to the DC-link. As can be seen, the solutions for eliminating 5th harmonic attained when the switching angle is within the range 65^o < α_1 < 90^o which is in contrary to 7th harmonic, where 40^o < α_1 < 55^o making it impossible to eliminate these two harmonics at the same time.

A proper selection of the harmonics to be reduced or eliminated depends on the application needs. To exemplified, in the second scenario adding two levels to the square-wave current is considered following (4) and 7th, 11th and 13th harmonic orders are targeted to be half of their values comparing to the square-wave current. Here, following (7) an

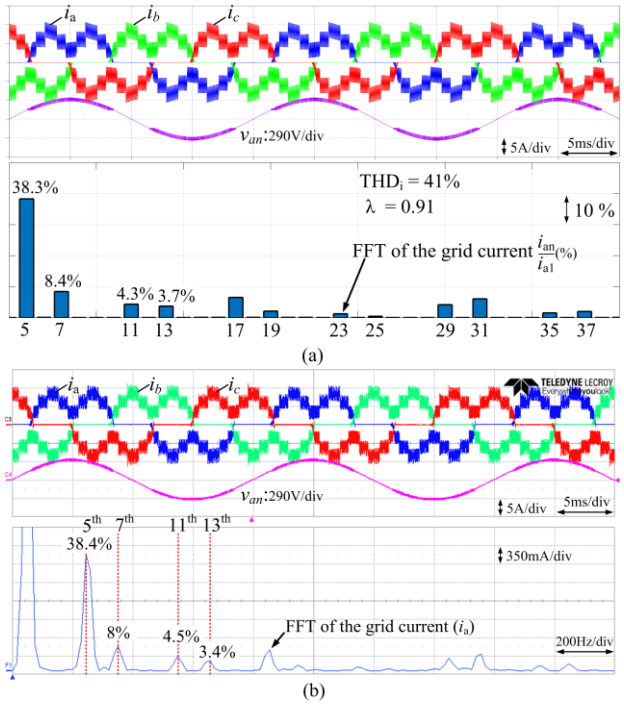


Fig. 10. Obtained results for the proposed 7th , 11th and 13th harmonics cancellation using hysteresis current control at V_o = 700Vdc and P_o = 3kW (P_o = 60%): (a) simulation results of three-phase input currents with Fast Fourier Transform (FFT) of the input current (i_a), (b) measured experimental results of three-phase input currents with FFT of the input current (i_a) [with I_0 = 1, I_1 = 0.7328, α_1= 38.3^o, I_2 = 0.7328, α_2= 51.5^o].

TABLE II
COMPARATIVE EXPERIMENTAL RESULTS AT OUTPUT POWER LEVEL OF 3 KW

Harmonic Mitigation Strategy	**Harmonic Distribution and THD$_i$ (%)**					
	$\frac{i_{a,5}}{i_{a,1}}$	$\frac{i_{a,7}}{i_{a,1}}$	$\frac{i_{a,13}}{i_{a,1}}$	$\frac{i_{a,13}}{i_{a,1}}$	**THD$_i$**	λ
7th, 13th harmonic cancellation (Fig. 7(b))	32.7	0.5	9.4	0.8	35.3	0.93
5th, 13th harmonic cancellation (Fig. 8(b))	2.1	38.5	25.4	1.5	48.6	0.88
7th,11th,13th harmonic cancellation (Fig. 10(b))	38.4	8	4.5	3.4	41.1	0.91
Conventional method (square-wave) (Fig. 6(b))	21	13	8.9	7	29	0.94

optimization needs to be performed, which has been done using a MATLAB genetic optimization algorithm. It is important to apply a suitable restriction following (5) and (6). As Fig. 10 shows the three harmonic orders of 7th, 11th and 13th have been reduced which as explained before results in increase of the 5th harmonic. Table II summarizes the obtained results based on the targeted harmonic orders and THD$_i$ for both the proposed and the conventional square-wave methods. As can be seen for all cases the obtained results slightly differ from what expected which is due to the presence of grid impedance, and consequently affects the calculated angles.

As it was discussed in Section III.A, depending on the

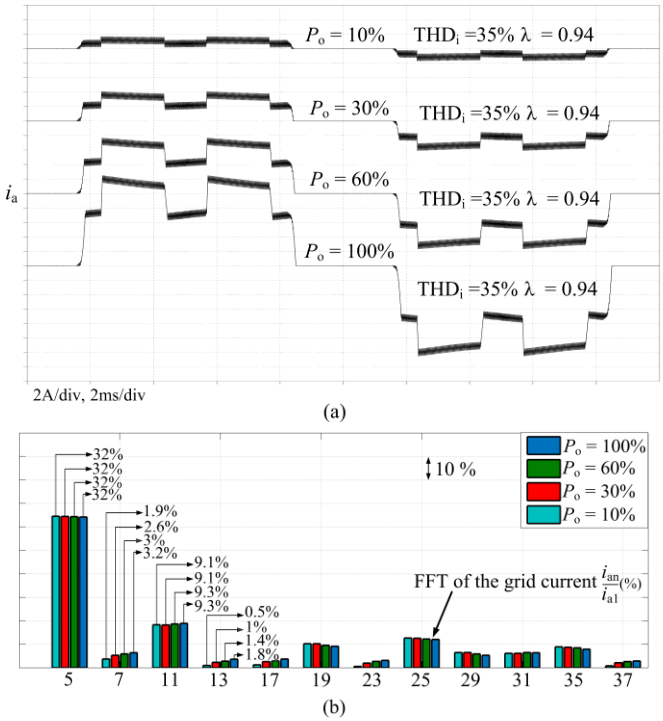


Fig. 11. Simulated input current i_a for the proposed 7th and 13th harmonic reduction at different power levels: (a) input current waveforms with corresponding THD$_i$ and λ (b) FFT of the input current (i_a).

application requirement the converter may operate at different partial power. In fact, this is quite common in applications such as ASD systems [22]. Here, the first modulation type where 7th and 13th harmonic orders are targeted (Fig. 7) is considered when the output power is changed in the range of 10% < P_o < 100%. Notably, following (11) the converter parameters have been re-calculated in order to obtain CCM operation based on the minimum power (i.e., P_o = 10%). Therefore, L_{dc} and *HB* are changed to 4 mH and 0.5 A, respectively. Fig. 11 shows the obtained simulation results of input current at phase-a (i_a) at different power levels along with their corresponding harmonic distribution. As it can be seen from Fig. 11(b), although at all power levels same THD$_i$ is obtained, but notably at lower power levels (i.e., P_o = 10% and P_o = 30%) 7th and 13th harmonics of interest are more reduced. This is due to the fact that in simulation the line impedance is constant and at lower powers the effective line impedance reduces and consequently its effect on the current modulation as a phase-shift error reduces as well.

To further verify the proposed method at different power levels, same condition is applied to the hardware prototype and the obtained experimental results at P_o = 100% and 10% are illustrated in Fig. 12. As it can be seen from both simulation and experimental results, the performance of the system in terms of THD$_i$ and λ is almost constant regardless of the load power.

Finally, the start-up and shut-down dynamic behavior of the implemented system are illustrated in Fig. 13. For the start-up phase of operation, the input voltage is already

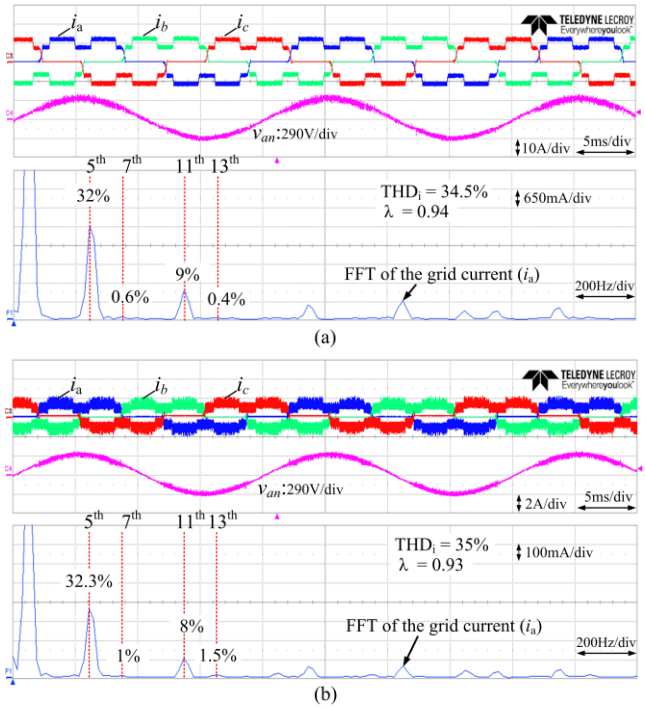


Fig. 12. Experimental results for the proposed 7th and 13th harmonics cancellation at different power levels: (a) measured three-phase input currents with Fast Fourier Transform (FFT) of the input current (i_a) at 100% of rated power (P_o = 5 kW) and (b) measured three-phase input currents with Fast Fourier Transform (FFT) of the input current (i_a) at 10% of rated power (P_o = 500 W). [L_{dc} = 4 mH, HB = 0.5 A]

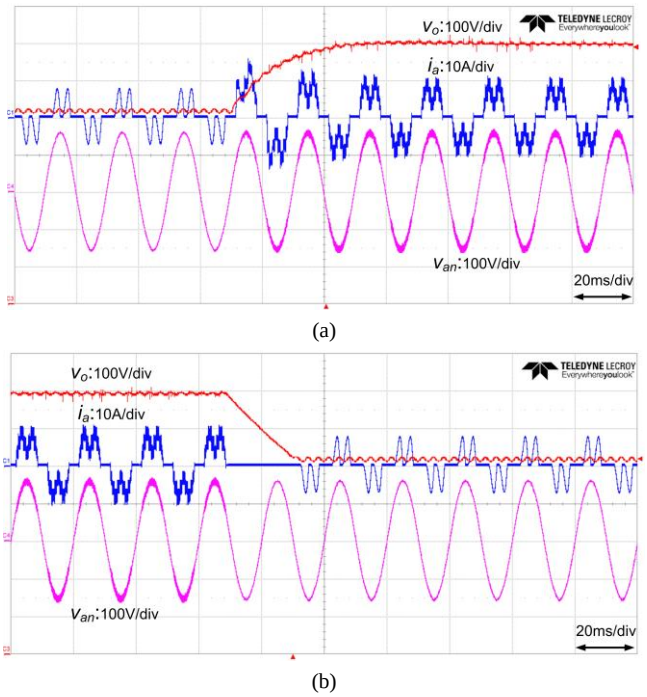


Fig. 13. Measured dynamic behavior of input current i_a and output voltage V_o at (a) startup and (b) shutdown at the nominal operating conditions.

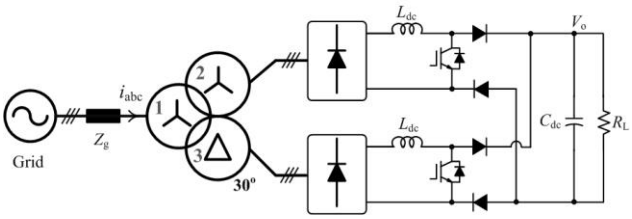


Fig. 14. Extension of conventional 12-pulse rectifier system connected in parallel on DC side applying the proposed current modulation strategy. (The leakage inductances of $L_1 = L_2 = L_3$ = 10 μH, winding resistance of $R_1 = R_2 = R_3$ = 0.1 Ω, and winding ratio of $n_\Delta/n_y = \sqrt{3}$).

applied, the load current is flowing and boost converter is in the off-state. Turning on the DC-DC converter makes the controller to start the pulse pattern modulation as seen from the input current i_a and changes the output voltage V_o from 515 V_{dc} to 700 V_{dc} without any large overshoot (Fig. 13(a)). The symmetrical pulse patterns on the input current after 100 ms validate the PLL settling time. At shut-down phase of operation the control circuit permanently turns off the IGBT switch so it stops the current modulation and the output voltage drops to 515 V_{dc} (Fig. 13(b)).

V. Perspectives

The proposed concept gives the possibility to eliminate various sets of harmonic components in a three-phase diode rectifier based on electronic inductor concept. Therefore, based on the application requirement employing the proposed method can further improve the input current quality by reducing the low order harmonics. However, as stated before, targeting 5th and 7th orders harmonic simultaneously solely based on a single unit system is impossible. In this section, one of the possible solutions based on combination of nonlinear loads [22]-[24] are briefly discussed.

Here, the proposed method is applied to a multi-pulse rectifier system [10]. Fig. 14 illustrates the application of the proposed concept in a 12-pulse rectifier topology with a common DC-bus. The comparative simulation results are shown in Fig. 15. Here, except the output power which is set to 6 kW, same parameters for the system is applied as mentioned in Table I. Fig. 15(a) illustrates the total input current waveform of a conventional 12-pulse rectifier system. Basically, the 12-pulse arrangement eliminates the 5th, 7th, 17th and 19th harmonic orders (see Fig. 15(d)). The improved input current harmonic distortion for a 12-pulse rectifier system depending on the output power level varies between 10% < THD$_i$ < 15%. Hence, employing the proposed method applying a two-level current modulation strategy at the DC-link following (1) and (3) can further improve the input current quality by targeting the remaining 11th, 13th harmonic orders. Notably, here same modulation pattern is applied to each converter. The obtained results in Figs. 15(b) and 15(d) show that the new 12-pulse rectifier system obtained THD$_i$ ≈ 5.7%, which is comparable with a conventional 18-pulse rectifier system.

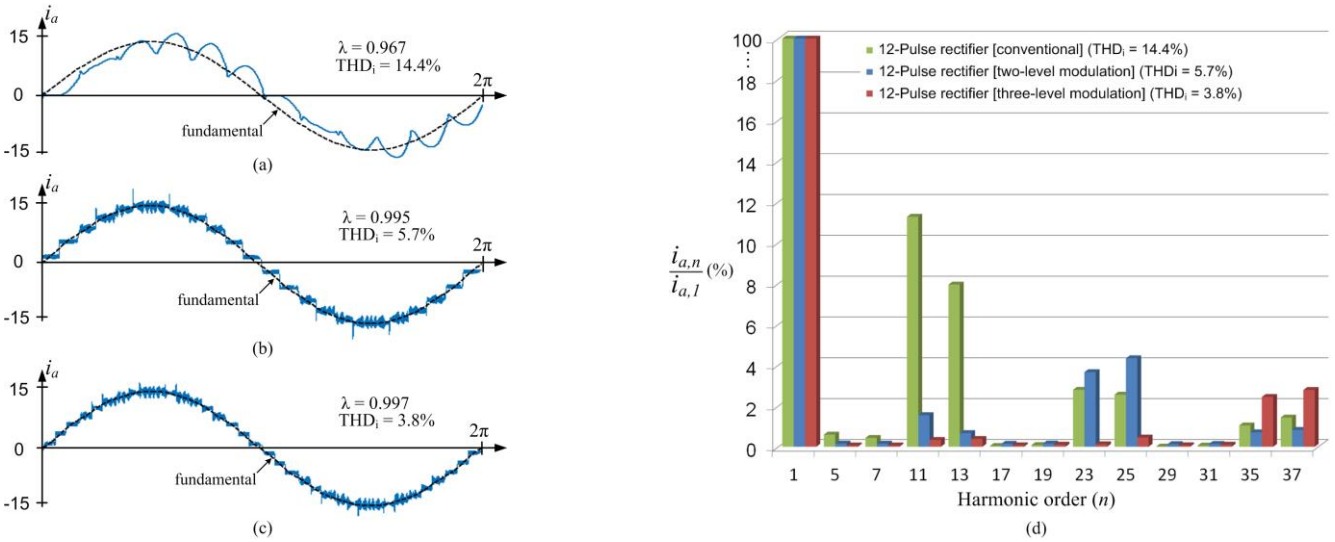


Fig. 15. Comparative simulation results of total input current (i_a) at P_o = 6 kW: (a) conventional 12-pulse rectifier (V_o = 511 V_{dc}), (b) proposed method with two-level current modulation at DC-link targeting 11th and 13th harmonics (V_o = 700 V_{dc}) [with I_0 = 1, I_1 = 1.932, α_1= 45°], (c) proposed method with three-level current modulation at DC-link targeting 11th, 13th, 23th, and 25th harmonics (V_o = 700 V_{dc}) [with I_0 = 1, I_1 = 1.88, α_1= 50°, I_2 = 1.97, α_2= 40°], (d) THD_i of total input current.

As each current level in the proposed technique can contribute to mitigation of two low order harmonics, extending the number of the current level using (4) can target larger number of harmonics. Therefore, employing a three-level current modulation at the DC-link can target two more harmonics of 23th and 25th in addition to 11th and 13th harmonics. The obtained total input current waveform with a unity power factor is depicted in Fig. 15(c) and the harmonic distribution resulting in $THD_i \approx 3.8\%$ is shown Fig. 15(d). In fact, the only remaining 35th and 37th harmonics imply that applying the proposed method with three-level modulation improves the performance of a conventional 12-pulse rectifier system to be comparable with a conventional 24-pulse rectifier system. Moreover, the output voltage can be increased to higher voltage levels using the boost topology; this is beneficial when the DC-link voltage is fed to an inverter. Unlike the conventional multi-pulse rectifier systems which the performance of the system is dependent of the load profile, applying the proposed concept can maintain the input current THD_i and power factor regardless of the output power variation.

VI. Conclusion

In this paper a novel current modulation technique has been proposed for a three-phase rectifier with an electronic inductor at the DC-link side. The proposed method modulates the DC-link current to control the fundamental current and to reduce the selected line current harmonics. Moreover, calculations of the optimum switching patterns have been conducted based on applying the minimum number of current levels. A main advantage of the proposed method is that the relative values of harmonics with respect to the fundamental value remain constant regardless of load profile variation. Applying the proposed method to other configurations such as 12-pulse rectifier can significantly improves THD_i comparative to a 24-pulse rectifier. The performance of the proposed method can be improved by increasing the number of the levels in order to obtain optimum solutions for low order harmonics which completely depends on the switching frequency and inductor size.

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