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Comparison between 9-level hybrid asymmetric and conventional multi-level inverters for medium voltage application

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Comparison between 9-level Hybrid Asymmetric and Conventional Multi-Level Inverters for Medium Voltage Application

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Abstract—**A hybrid asymmetric 2-cell 9-level inverter is analysed and compared with two conventional multilevel inverters: the 9-level cascaded H-bridge and the 3-level diode clamped inverter, when used to drive an induction motor of 4.16kV/500kVA. In this analysis, Total Harmonic Distortion (THD), First Order Distortion Factor (DF1), power semiconductor losses, and efficiency are selected as performance indexes. The results indicate that the hybrid asymmetric topology has a better performance in performance indexes than the other topologies which leads to energy saving, better power quality and reduction in size, weight and volume of the LC-filter.**

Keywords—Multi-level inverters; medium voltage drives; power losses, efficiency

I. INTRODUCTION

There is an increasing demand for multi-level inverter systems capable of providing high output voltage, good spectral performance and easy control. Examples of such systems are medium voltage drives, FACTS devices, HVDC transmission, and active power filters [1], [2]. Currently, medium voltage drives cover a power range of 0.2 MW to 100 MW at voltage level from 2.3 kV up to 13.8 kV [2].

Nevertheless, the design of medium voltage drives is faced with a number of challenges related to the topologies and control of the power line side converter (e.g. power quality, resonance, and power factor) and motor side converter (e.g. *dv/dt*, torque ripples, motor derating caused by generated harmonics and traveling wave reflections), as well as power semiconductor devices (semiconductor losses) [1]. Essential requirements for medium voltage drives are high efficiency, high reliability, low cost, low volume, and in some applications, high dynamic performance and regeneration capability [1].

Due to semiconductor voltage and current rating limitations, it is difficult to connect a single semiconductor device directly to a medium voltage network. To overcome this problem, a family of multi-level inverters have been introduced for medium voltage levels [3].

Multi-level inverters consist of power semiconductor devices and capacitors which generate voltages with stepped waveforms in the output. The DC-link in the input of multi-level inverters comprises of a capacitor, or bank of capacitors. The switching schemes of semiconductor switch devices allow the inverter to generate higher stepped voltages by using more capacitors in the DC-link, however most semiconductor devices cannot withstand high level of voltages to several kVs.

The large number of semiconductors in multi-level inverters has a negative impact on the reliability and overall efficiency. However, using inverters with a low number of semiconductors requires large and expensive *LC*-filters to limit insulation stress of the motor windings, or can only be used in applications with motors that can withstand this stress [4]. As a result, there is significant effort to develop multi-level inverters with the same performance and less power devices.

The best known power circuit multi-level topologies include: the cascaded H-bridge, diode clamped and flying-capacitor multi-level inverters [5]-[7]. These classical solutions are called symmetric multi-level inverters, because they have the same voltage on each of the intermediate-circuit capacitors, and all the power semiconductors have to be capable to block the same voltage in their 'off' state. An asymmetric multi-level inverter has exactly the same circuit topology as the symmetric multi-level inverter - it differs only in the capacitor voltages. However, the properties of asymmetric multi-level inverters are quite different. Specifically, the number of output-voltage levels can be dramatically increased [8], [9]. Since the different cells of asymmetric inverters work with different DC-link voltages and different switching frequencies, it is more efficient to select various semiconductor devices that are appropriate for the conditions of each cell. These inverters are called "hybrid multi-level inverters" [10].

This paper compares a hybrid asymmetric multi-level inverter with diode-clamped and cascaded H-bridge multi-level inverters in terms of harmonic distortion, power losses and efficiency. The paper is organized into the following sections: First, the structure of the multi-level inverter topologies is briefly described. Then, the inverter specifications, modulation techniques and performance indexes are investigated. Finally, the investigated topologies are compared and the results are presented.

II. MULTI-LEVEL INVERTER TOPOLOGIES

A. Cascaded H-bridge Multi-Level Inverter (CHB MI)

A single phase of a 9-level cascaded H-bridge multi-level (9-L CHB ML) inverter is shown in Fig. 1. In this topology power cells are in series and the number of phase voltage levels that can be obtained at the converter terminals is proportional to the number of cells. Simply, the number of phase voltage levels at the converter terminals is $2N + 1$, where N is the number of cells [3]. This topology has excellent input current and output voltage waveforms. The output voltage has smooth steps, so an output filter is usually not needed or in the case needed it can be very small.

B. Diode Clamped Multi-Level Inverter (DC MI)

Fig. 2 shows a single phase of a 3-level diode-clamped multi-level inverter (3-L DC MI). In this topology, semiconductor devices are connected in series and the dc-link is divided by smaller capacitors and connects to the switches by clamping diodes [11]. The clamp diode connections are necessary to block the current and their numbers in each leg are selected in such a way to have the same blocking voltage like the switches. This topology has a simple circuit structure but generates high and steep voltage steps which may impact the life time of the motor windings. An additional filtering stage is therefore needed to reduce the ripple in the inverter output voltage.

C. Hybrid Asymmetric Multi-Level Inverter (HA MI)

Fig. 3 shows the single phase circuit diagram of an asymmetric cascaded two-cell 9-level inverter (9-L HA MI), where the dc voltages for the H-bridge cells are not equal [12].

In the asymmetric topology, a high-voltage (HV) stage, which has a higher voltage rating and operates at low switching frequency, is ideal for GTO/IGCT switches. GTO and IGCT are reliable devices providing a high blocking voltage [13], [14]. On the other hand, the low-voltage (LV) stage, which has a lower voltage rating and operates at high switching frequency, is ideal for IGBTs. IGBTs allow higher switching frequencies together with good performance at lower voltages [15]. By combining IGBT and GTO/IGCT in an asymmetric multi-level inverter, a hybrid inverter could be obtained.
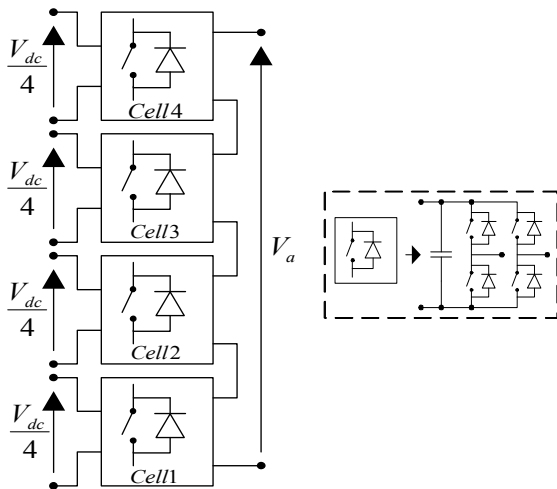

Fig. 1. 9-level Cascaded H-bridge multi-level inverter (9-L CHB MI) power circuit
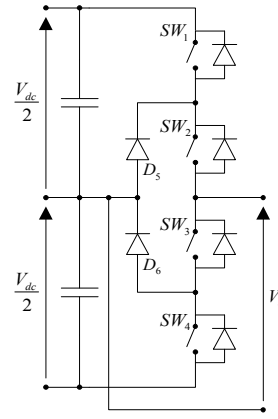

Fig. 2. 3-level Diode-clamped multi-level inverter (3-L DC MI) power circuit
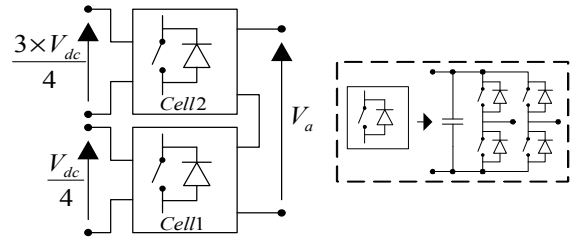

Fig. 3. 9-level Hybrid asymmetric multi-level inverter (9-L HA MI) power circuit

III. INVERTER SPECIFICATIONS

In this section both the inverter rating and specifications are chosen close to that of what is commercially available for medium voltage applications [16], [17]. Some commercial medium voltage drives, their power and voltage ratings and converter topologies with the semiconductor switches applied to them are summarised in Table I. The drive system in this paper is designed to supply an induction motor with line-to-line voltage of 4.16 kV, apparent power of 500 kVA, a frequency of 50 Hz and a power factor 0.85. Table II summarizes the basic inverter data for the design of the main power part components.

TABLE I. COMMERCIAL MEDIUM VOLTAGE DRIVES

Company	Drive Model	Power (MVA)	Voltage (KV)	Topology	Semi-conductor
Robicon	Perfect Harmony	0.3 – 0.31	2.3 – 13.8	CHB MI	LV IGBT
Allen Bradley	Power Flex 7000	0.15 – 6.7	2.3, 3.3, 4.16, 6.6	CSI	IGCT
Siemens	Masterdrive MV	0.66 – 9.1	2.2, 3.3, 4.16, 6.6	3-L Diode Clamped	HV IGBT
	Masterdrive ML2	0.66 – 9.1	3.3	3-L Diode Clamped	IGCT
ABB	ACS 1000	0.3 – 5	2.3, 3.3, 4	3-L Diode Clamped	IGCT
	ACS 5000	5.2 – 2.4	4.16, 6, 6.6, 6.9	Cascaded H-Bridge	IGCT
	ACS 6000	3 – 27	3, 3.3	3-L Diode Clamped	IGCT
Alstom	VDM 5000	1.4 – 7.2	2.3, 3.3, 4.2	2-L VSI	IGBT
	VDM 6000	0.3 – 8	2.3, 3.3, 4.2	3-L Flying Capacitor	IGBT
	VDM 7000	7 – 9.5	3.3	3-L Diode Clamped	GTO
General Electric	Dura-Bilt5 MV	0.3 – 2.4	4.16	3-L Diode Clamped	IGBT
	MV-GP Type H	0.45 – 7.5	3.3, 4.16	Cascaded H-Bridge	IGBT

TABLE II. THE BASIC SPECIFICATIONS OF INVERTER AND INDUCTION MOTOR

Inverter line-to-line voltage(RMS)	4.16 kV
Phase current	60 A
Apparent inverter output power	500 kVA
Power factor of induction motor	0.85
Nominal dc-link voltage	6353 V
Modulation	Optimized PD-PWM
Carrier frequency	450 - 1050 Hz
Maximum junction temperature (IGBT, IGCT, diode)	125ºC

Modulation Technique

The modulation technique employed in this system is Phase Disposition PWM (PD-PWM). The PD-PWM method is one of the carrier-based PWM methods, and implementation is based on a comparison of a reference waveform with vertically shifted carrier waveforms [18]-[21]. This method uses N-1 carrier signals to generate the N-level inverter output voltage. The injection of a 3rd harmonic into the reference waveforms will achieve a 15% increase in modulation index compared to Sinusoidal PWM before over-modulation nonlinearities occur. This is simply because of the reduced height of the three-phase reference envelope that is achieved by third-harmonic injection [22]. In this technique, the 3rd harmonic is cleared in three-phase system. This modulation is named Switching Frequency Optimized PD-PWM (SFO-PD-PWM) and it is shown in Fig. 4.
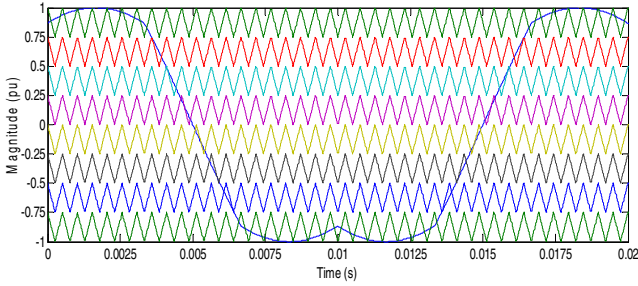

Fig. 4. SFO-PD-PWM technique, reference and carrier signals

A. DC-Link Voltage

The minimum dc-link voltage to achieve an output line-to-line voltage of 4.16 kV using SFO-PWM can be calculated by

$$V_{dc,\min} = \sqrt{2} \times V_{ll,1,rms} = \sqrt{2} \times 4.16\text{kV} = 5883 \text{ V} \tag{1}$$

To determine the nominal dc-link voltage of the inverter, a voltage reserve of 8% is assumed (for the imperfections of the real system, control reserve, device voltage drops, etc.):

$$V_{dc,n} = 1.08 \times V_{dc,\min} = 1.08 \times 5883 = 6353 \text{ V} \tag{2}$$

B. Power Semiconductor Selection

Table III and Table IV summarize the design of the power semiconductors for the 4.16 kV inverter, assuming a carrier frequency of 600 Hz in all topologies. The voltage V$_{com}$ describes the commutation voltage of the corresponding commutation cells. $V_{com@100FIT}$ is an index for the maximum voltage that the semiconductor switch can withstand and is

defined by the nominal voltage of the semiconductor for which it has a cosmic ray withstand capability of 100 FIT (one FIT is equivalent to one failure in 10^9 operation hours). The ratio of $V_{com}/V_{com@100FIT}$ represents a measure of the device voltage utilization for different topologies [23].

TABLE III. INVERTER VOLTAGE AND SEMICONDUCTOR SPECIFICATIONS FOR CONVENTIONAL TOPOLOGIES

Topology	3L-DC MI	9L-CHB MI
Power devices	6.5 kV /200 A FZ200R65KF2 INFINEON	1.7kV/200 A BSM200GB170DLC EUPEC
Nominal dc-link voltage	6353 V	794 V
Rated device voltage	6.5 kV IGBT	1.7 kV IGBT
Commutation voltage	3176 V	794 V
$V_{com@100FIT}$	3600 V	900 V
V_{com} / $V_{com@100FIT}$	0.88	0.88

TABLE IV. INVERTER VOLTAGE AND SEMICONDUCTOR SPECIFICATIONS FOR HYBRID ASYMMETRIC TOPOLOGY

Topology	9L-HA MI	
	Main Inverter (IGCT)	Sub Inverter (IGBT)
Power devices	4.5 kV/340 A 5SHX04D4502 /5SDF03D4502 ABB	1.7 kV/200 A BSM200GB170DLC EUPEC
Nominal dc-link voltage	2382 V	794 V
Rated device voltage	4.5 kV IGCT	1.7 kV IGCT
Commutation voltage	2382 V	794 V
$V_{com@100FIT}$	2700 V	900 V
V_{com} / $V_{com@100FIT}$	0.88	0.88

IV.   PERFORMANCE INDEXES

The performance indexes used in the comparative analysis are: Total Harmonic Distortion (THD), First-order Distortion Factor (DF1), semiconductor power losses (conduction and switching losses) and finally efficiency.

A. THD

The THD of the inverter can be calculated as

$$THD\% = \frac{100}{V_1} \sqrt{\sum_{h=2,3,...}^{\infty} V_h^2} \tag{3}$$

where V_1 is the fundamental harmonic of the signal analyzed, h is the harmonic order, and V_h is the harmonic amount of order h.

B. DF1

In AC motor drive applications, the first-order distortion factor (DF1) which is the Weighted Total Harmonic Distortion (WTHD) is another considerable index. DF1 is defined by

$$DF1\% = \frac{100}{V_1} \sqrt{\sum_{h=2,3,...}^{\infty} \left(\frac{V_h}{h}\right)^2} \tag{4}$$

The output phase and line voltage waveforms and their harmonic spectrum for the 9-level hybrid assymetric multi-level inverter are shown in Fig. 5. It can be seen that the harmonic content, especially in the low level orders are dramatically decreased because of the increase in the number of output voltage levels.
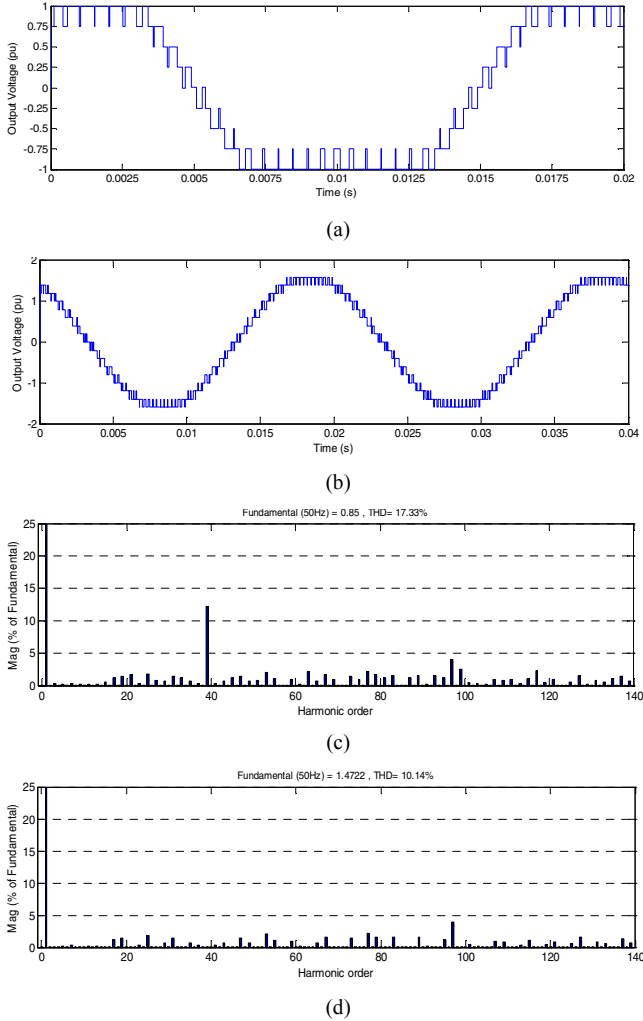

(a)

(b)

(c)

(d)

Fig. 5 Output voltage waveforms and harmonic spectrum: a) Output phase voltage, b) Output line voltage, c) Harmonic spectrum of output phase voltage, d) Harmonic spectrum of output line voltage

C. Semiconductors power losses

The semiconductor power losses can be calculated from the curves ($v_{sat} \times I_{load}$) and ($E \times I_{load}$), given in the datasheet of each device. In these curves the parameters are defined as:

v_{sat}: The on-state saturation voltage (v_{ce} for the IGBT, v_T for the IGCT and v_F for the diode); E: The switching energy losses in one commutation (E_{on} for a turn-on commutation, E_{off} for a turn-off commutation and E_{rec} for reverse recovery process); I_{load} : The load current.

These curves are used in Matlab to calculate power losses. Matlab uses the mathematical models that represent the functions v_{sat} (i_{load}) and E (i_{load}) for semiconductors. These models are obtained by extrapolation of curves extracted from datasheets and using the curve-fitting toolbox (*cftool*).

The semiconductor devices used in the topologies are: IGBT/BSM200GB170DLC [24], IGBT/ FZ200R65KF2 [25], IGCT/5SHX04D4502 [26] and diode 5SDF03D4502 [27].

The mathematical models found for semiconductors curves used in this work are given by

$$v_{ce,IGBT} = (a_1 \cdot e^{a_3 \cdot I_{load}} + a_2 \cdot e^{a_4 \cdot I_{load}}) \tag{5}$$

$$v_{F,IGBT} = (b_1 \cdot e^{b_3 \cdot I_{load}} + b_2 \cdot e^{b_4 \cdot I_{load}}) \tag{6}$$

$$E_{on} = c_1 \cdot I_{load}^2 + c_2 \cdot I_{load} + c_3 \tag{7}$$

$$E_{off} = d_1 \cdot I_{load} + d_2 \tag{8}$$

$$E_{rec} = e_1 \cdot I_{load}^2 + e_2 I_{load} + e_3 \tag{9}$$

$$v_{T,IGCT} = f_1 \cdot I_{load} + f_2 \tag{10}$$

$$v_{F,IGCT} = g_1 \cdot I_{load} + g_2 \tag{11}$$

The numerical values in these mathematical models are presented in Appendix.

Based on these mathematical models, the conduction and switching losses are calculated for each semiconductor device. The sum of switching and conduction power losses gives the total power losses.

1. Conduction losses

The conduction power losses are calculated by (12) for the main switch and by (13) for the diode:

$$P_{cond_{SW}} = \frac{1}{T_{SW}} \int_0^{T_{SW}} v_{sat}(t) \cdot i_{load}(t) \cdot v_{cmd_{SWx}}(t) \cdot dt \tag{12}$$

$$P_{cond_D} = \frac{1}{T_{SW}} \int_0^{T_{SW}} v_F(t) \cdot i_{load}(t) \cdot v_{cmd_{SWx}}(t) \cdot dt \tag{13}$$

Where T_{sw} is the switching cycle and v_{cmd} is the command signal of switch that can be 1 or 0.

The total conduction power losses are calculated by (14):

$$P_{cond_{TOTAL}} = P_{cond_{IGBT/IGCT}} + P_{cond_D} \tag{14}$$

2. Switching losses

The turn on, turn off power losses for the main switch are given by (15) and (16) and reverse recovery power losses for the diode is calculated by (17):

$$P_{on} = \frac{1}{T} \sum E_{on}(i_{load}(t)).f_{SW} \tag{15}$$

$$P_{off} = \frac{1}{T} \sum E_{off}(i_{load}(t)).f_{SW} \tag{16}$$

$$P_{rec} = \frac{1}{T} \sum E_{rec}(i_{load}(t)).f_{SW} \tag{17}$$

The total switching power losses are calculated by (18):

$$P_{SW_{TOTAL}} = P_{on} + P_{off} + P_{rec} \tag{18}$$

Finally, the total power losses are the sum of all conduction and switching power losses and computed by (27):

$$P_{loss} = P_{cond_{TOTAL}} + P_{SW_{TOTAL}} \tag{19}$$

Based on these mathematical models, the conduction and switching losses are calculated for each semiconductor device. The sum of the switching and the conduction power losses gives the total power losses.

V. COMPARISON OF DIFFERENT MULTI-LEVEL INVERTER TOPOLOGIES

The comparison for the drive system explained in the previous section will be made in two methods:

- Comparison in the state of constant carrier frequency (600 Hz)
- Comparison in the state of constant efficiency (99%)

A. Comparison at constant carrier frequency

450-1050Hz range is typical for available industrial medium voltage drives [17]. The carrier frequency is assumed to be 600Hz for the various topologies in this study. The performance indexes are listed in Table V and the power losses distributions for each topology are shown in Fig. 6.

According to Table V, both the hybrid asymmetric and cascaded H-bridge inverters have the same THD for current and voltage, since they generate the same voltage levels. Compared with the other two topologies, the THD for the diode clamped inverter is about 3 times higher for the current and 3.8 times higher for the voltage. The THD of the voltage is higher than current since the load is inductive. Similarly, the DF1 for the diode clamped is larger than the DF1 for the hybrid asymmetric and cascaded H-bridge inverters. This means that at a constant carrier frequency, the harmonics of the output voltage appears at higher frequencies which are more damped by an inductive load. Moreover, power losses for hybrid asymmetric topologies are lower, compared with both the cascaded H-bridge and the diode clamped inverters.

Considering the power rating of inverters, the hybrid asymmetric topology seems to show better performance in saving energy compared to other conventional topologies. As can be seen in Fig. 6a, in the hybrid asymmetric inverter, the IGBT cell has the largest portion of power losses, as this cell operates at a higher switching frequency than IGCT cell, and therefore the switching losses increases. In both of the cells the conduction power losses represent the most significant portion of the total losses. This is due to the fact that the carrier frequency is low and all the switching devices commutate at a low switching frequency. Moreover, the RMS currents over the switches in the IGCT and IGBT inverters are 78 A and 72 A respectively – consequently IGCT inverter has higher conduction losses than the other one.

Fig. 6b shows the power losses distribution in cascaded H-bridge inverter. In this topology, all the cells operate with the same switching frequency and dc link voltages. Therefore, all cells present approximately the same semiconductor power losses. In the diode clamped inverter, Fig. 6c, the power losses are concentrated in switch 1 and switch 4. This occurs because switch 2 in the positive and switch 3 in the negative half cycles do not commutate to generate the zero voltage level. So, the conduction losses are the major of power losses in these switches. In diodes, most of power losses are related to switching losses, since these diodes have the function of blocking the current in all the switches commutations.

TABLE V. COMPARISON OF MULTI-LEVEL INVERTER TOPOLOGIES AT CONSTANT CARRIER FREQUENCY

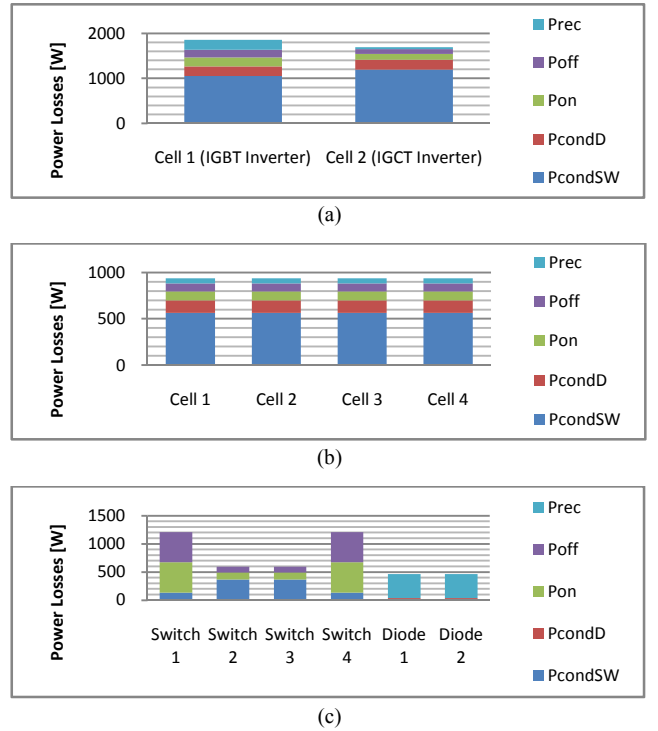| Comparison	Constant Carrier Frequency (600 Hz)		
Topologies	Hybrid Asymmetric 9-Level	Cascaded H-bridge 9-Level	Diode-Clamped 3-Level
Total number of devices/phase	4 IGBT Modules + 4 IGCT/Diodes	16 LV-IGBT Modules	4 HV-IGBT Modules + 2 Diodes
Number of phase-voltage levels	9	9	3
Number of line-voltage levels	17	17	5
THD of phase-current [%]	5.09	5.21	15.36
THD of line-voltage [%]	7.51	7.52	31.6
DF1 of line-voltage [%]	0.47	0.48	10.21
Total power losses [W]	3552	3893	4544
Inverter Efficiency [%]	99.29	99.22	99.09

(a)

(b)

(c)

Fig. 6. Power losses distribution in constant frequency (600 Hz) (a) Hybrid asymmetric 9-level inverter (b) Cascaded H-bridge 9-level inverter (c) Diode clamped 3-level inverter

B. Comparison at constant efficiency

To evaluate the three designed topologies for different applications with demanded efficiency, it is assumed that the inverter efficiencies for all of topologies are about 99% at a constant inverter power of 500 kVA. This efficiency is typical for state-of-the-art medium voltage drives [12]. Since the conduction losses of the switches are dependent on the average values of voltage and current of switches, by controlling the carrier frequencies the efficiency of 99% can

be obtained. The performance indexes for this comparison are listed in Table VI and the power losses distributions are shown in Fig. 7.

Compared to the constant frequency state, with an increase in the carrier frequencies, the THD values of current and voltage do not change significantly. This fact is due to the topologies and the output voltage levels remaining unchanged. Instead, since the frequency of the first harmonic band directly affects the DF1, the first distortion factor is decreased. This can be seen especially in hybrid asymmetric topology that by increasing the carrier frequency to 5400 Hz, DF1 is reduced by 93%. In the cascaded H-bridge with the carrier frequency of 800 Hz and diode-clamped with the carrier frequency of 1150 Hz, the reductions of DF1 are approximately 79% and 48%. These values of DF1 suggest that the output filter of the diode-clamped and cascaded H-bridge inverters will have greater volume, weight, and cost than the filter used in the hybrid asymmetric inverter to obtain the same line voltage distortion.

On the other hand, considering the power losses distribution in hybrid asymmetric topology, the switching losses are the major part of the power losses in cell 1 (IGBT inverter). This increase of switching losses in respect to the previous comparison (carrier frequency of 600 Hz) shows that in the hybrid asymmetric topology the carrier frequency affects the IGBT inverter switching losses more than the IGCT inverter, since it works with higher switching frequency. In addition, in the state of operation in the same efficiency in three topologies, the frequency of carrier signals in the hybrid asymmetric topology is about 6.2 times of cascaded H-bridge and 4.7 times of diode-clamped. It shows more relevance of this topology compared to the switching frequency that in practice limits the increase of carrier frequency up to 1000 Hz.
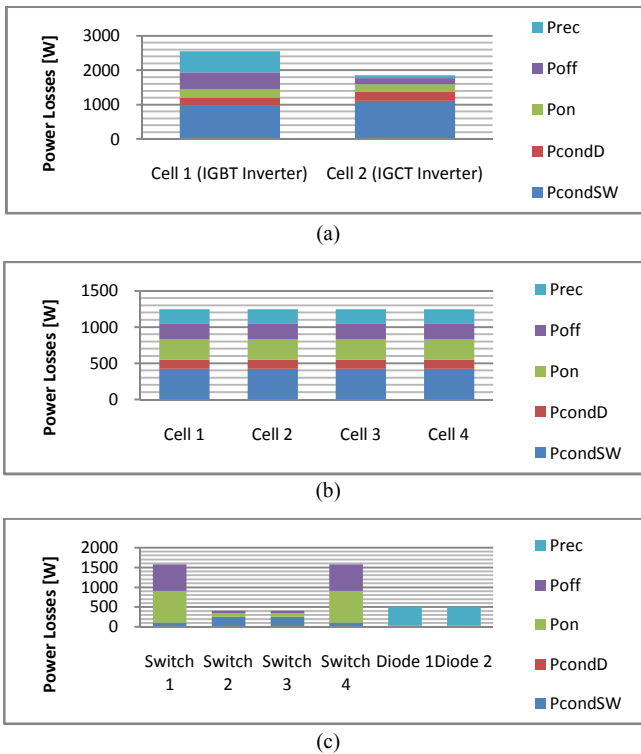

(a)

(b)

(c)

Fig. 7. Power losses distribution in equal efficiency (99%) (a) Hybrid asymmetric 9-level inverter (b) Cascaded H-bridge 9-level inverter (c) Diode clamped 3-level inverter

TABLE VI. COMPARISON OF MULTI-LEVEL INVERTER TOPOLOGIES AT EQUAL EFFICIENCY

Comparison	Equal Efficiency (99%)		
Topologies	Hybrid Asymmetric 9-Level	Cascaded H-bridge 9-Level	Diode-Clamped 3-Level
Total number of devices/phase	4 IGBT Modules + 4 IGCT/Diodes	16 LV-IGBT Modules	4 HV-IGBT Modules + 2 Diodes
Number of phase-voltage levels	9	9	3
Number of line-voltage levels	17	17	5
Carrier frequency [Hz]	5400	860	1150
THD of phase-current [%]	1.73	5.02	15.84
THD of line-voltage [%]	6.6	6.78	32.3
DF1 of line-voltage [%]	0.037	0.102	5.338
Total power losses [W]	4897	4999	4982
Inverter Efficiency [%]	99.01	99.01	99.01

VI. CONCLUSION

A comparison between the 9-level cascaded H-bridge, the 3-level diode clamped, which are the most conventional topologies in the industry, and 9-level hybrid asymmetric has been carried out, with analysis performed in two ways: operating at constant carrier frequency or constant efficiency. The results show that the hybrid asymmetric topology has better performance in both conditions than the conventional multi-level inverters in all the performance indexes, which can lead to energy saving and improvement of power quality and a reduction in size, weight and volume of the *LC* filter.

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APPENDIX
NUMERICAL VALUES FOR POWER LOSSES MATHEMATICAL MODELS

Device Model	IGBT/ BSM200GB170DLC	IGBT/ FZ200R65KF2	IGCT/5SHX04D4502 and diode 5SDF03D4502
a_1	2.197	3.754	-
a_2	-1.822	-2.733	-
a_3	0.001896	0.00183	-
a_4	-0.0223	-0.01589	-
b_1	1.456	2.437	-
b_2	-1.415	-2.176	-
b_3	0.001729	0.00171	-
b_4	-0.03326	-0.04544	-
c_1	$-1.878 \cdot e^{-7}$	$4.347 \cdot e^{-6}$	$-2.311 \cdot e^{-6}$
c_2	0.000358	0.006946	0.004573
c_3	0.0007119	0.1622	0.05617
d_1	0.0003271	0.00593	0.004573
d_2	-0.0008491	-0.003563	0.05617
e_1	$-1.636\,e^{-6}$	$-1.207 \cdot e^{-5}$	$-1.63 \cdot e^{-6}$
e_2	0.0005078	0.00426	0.001659
e_3	0.000305	0.07322	0.226
f_1	-	-	0.004706
f_2	-	-	1.818
g_1	-	-	0.006916
g_2	-	-	2.419