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Thermal Impedance Model of High Power IGBT Modules Considering Heat Coupling Effects

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***Abstract*— Thermal loading of Insulated Gate Bipolar Transistor (IGBT) modules is important for the reliability performance of power electronic systems, thus the thermal information of critical points inside module like junction temperature must be accurately modeled and predicted. Usually in the existing thermal models, only the self-heating effects of the chips are taken into account, while the thermal coupling effects among chips are less considered. This could result in inaccurate temperature estimation, especially in the high power IGBT modules where the chips are allocated closely to each other with large amount of heat generated. In this paper, both the self-heating and heat-coupling effects in the of IGBT module are investigated based on Finite Element Method (FEM) simulation, a new thermal impedance model is thereby proposed to better describe the temperature distribution inside IGBT modules. It is concluded that the heat coupling between IGBT and diode chips strongly influence the temperature distribution inside IGBT module, and this effect can be properly modeled/predicted by the proposed thermal impedance model.**

Keywords—IGBT module; FEM; heat coupling; thermal impedance network

I. INTRODUCTION

Power electronic converters have found wide applications in many industries like renewable energy systems, traction and high power motor drives [1], [2]. IGBT modules as key devices have inevitable role in reliability of high power electronic converters. Extreme thermal cycling or thermal loading may trigger the reliability problems like thermo-mechanical stresses which lead to progressive wear out of the device and catastrophic failures inside the device packaging, e.g. Bond wire lift-off or solder cracking [3]-[5]. There are mathematical models which relate the lifetime of IGBT modules to the thermal cycling [6], [7]. Besides, the device packaging may lead to breakdown if the maximum junction temperature given by manufacturer is violated [6]. Therefore, a precise calculation of temperature inside the device package is important to ensure an accurate life time estimation and cos-effective converter design.

In common operating conditions each chips generates heat that flows through multiple layers inside the package until dissipates in the heatsink. Besides, operation of multiple chips on the same substrate generates cross coupling heat flows between chips [8], [9]. The cross coupling heat flows also occur between different Direct Copper Bonding (DCB) sections on a same substrate which is negligible compared to the same DCB heat flows. The cross coupling heat flows are not fully considered in the design process and this paper investigates this behavior inside the IGBT module package by using Finite Element Method (FEM). The structure of high power IGBT module and the materials used in different layers is explained and. The concept of thermal cross coupling effect is described and the importance of this behavior is shown in the dynamic operation of IGBT module. In the next section, cross coupling thermal resistances between chips will be extracted as a function of distance between chips and location of the chips on the DCB. The extracted coupling thermal impedances will be used in a 3D thermal network which can facilitate the packaging design process from thermal point of view and define the thermal design margins in placement of the chips on the substrate.

II. CONDITIONS AND ENVIRONMENT FOR MODELING

The IGBT module under investigation consists of several IGBT and antiparallel diodes connected in parallel and mounted on the same substrate. The schematic view of the case study is shown in Fig.1. The materials applied in different layers are shown in Fig. 2. The case study IGBT module contains 6 half-bridge converters connecting in parallel consisting 12 IGBT chips and 12 diode chips totally. The schematic diagram of two-level half bridge converter is shown in Fig. 3. The converter specifications are listed in Table. I. The geometries of the model is provided by manufacturer and it is drawn in a commercial FEM software (ANSYS Icepack) to analyze the thermal behavior in static and dynamic operations. The IGBT module can operate for loading currents up to 1000 A and blocking voltage of 1700

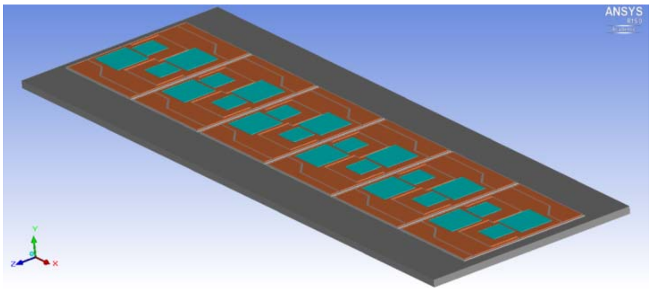

Fig. 1. Graphical view of high power IGBT module developed in ANSYS Icepak.

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volts. The silicon chips are mounted on DCBs and DCBs are placed on baseplate via solder layers. Bond-wires are ignored in this study for simplification due to their low impacts on temperature distribution on the substrate.

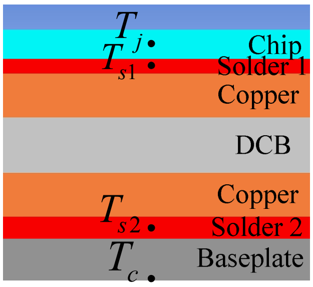

T_j
Chip
T_{s1}
Solder 1
Copper
DCB
Copper
T_{s2}
Solder 2
T_c
Baseplate

Fig. 2. Cross-section layers of IGBT module.

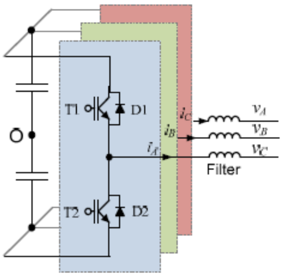

T1
D1
T2
D2
O
i_C
i_B
i_A
v_A
v_B
v_C
Filter

Fig. 3. Two-level voltage source DC-AC converter.

TABLE I. PARAMETERS OF THE POWER CONVERTER SHOWN IN FIG. 2.

Rated output active power P_o	250 kW
Output power factor PF	1.0
DC bus voltage V_{dc}	1050 VDC
*Rated primary side voltage V_p	690 V rms
Rated load current I_{load}	209 A rms
Fundamental frequency f_o	50 Hz
Switching frequency f_c	2 kHz
Filter inductance L_f	1.2 mH (0.2 p.u.)
IGBT module	1700V/1000A

III. THERMAL CROSS COUPLING EFFECTS

Generally, the common approach to calculate temperatures is using the device's datasheet. Manufacturers provide simplified lumped thermal networks which represent the thermal behavior of the device. Two typical thermal networks given in datasheets are Cauer or Foster networks which are equivalent RC networks that can be easily used in any circuit simulator to estimate the junction temperature of the IGBT chips and diode chips. The target thermal network used in this paper is Foster, which is mostly used by IGBT module manufacturers and is shown in Fig. 4. Each IGBT chip and diode chip generates separate heat paths which interconnect in the heatsink, but there are also mutual heat flows which make interference in the self-heat paths. This behavior is not fully covered by thermal models given in the datasheets since the only interconnection between the heat flows is the heatsink.

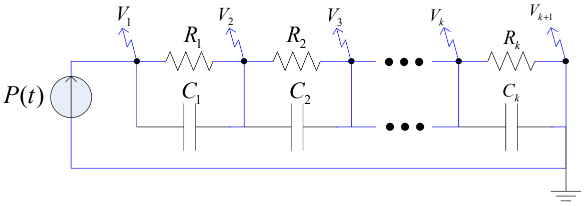

V_1
V_2
V_3
V_k
V_{k+1}
R_1
R_2
R_k
C_1
C_2
C_k
$P(t)$

Fig. 4. Foster network of the power devices in the power module.

For better understanding the importance of the thermal cross coupling effects, an example is given in this section. A loss profile which is generated by the converter shown in Fig. 3 is injected to the IGBT module. The loss profile is shown in Fig. 5. It is assumed that power losses are generated equally in the IGBT chips and diode chips respectively and distributed in the chips volume homogenously. The temperature profile over IGBT module when the IGBT power losses are in the peak value is shown in Fig. 6. As it is highlighted in Fig. 6, IGBT module consists of 6 cells; each cell contains a half-bridge converter including two pairs of IGBTs and antiparallel diodes, which are named as T1/D1 and T2/D2. The pairs of T1/D1 and T2/D2 are excited by the loss profile shown in Fig. 4 alternatively. The temperature on each chip is formed by both the self-heating source of the chip and thermal cross coupling effects from the other chips. It can be observed form Fig. 6 that in each half bridge cell the thermal coupling effects from the other cells are negligible since the interval temperature between cells are the same as the baseplate, as a result the study can be focused on one cell (T1, T2, D1, D2). Furthermore, due to symmetrical position of the pairs of T1/D1 and T2/D2 in the cell, the self-heating and thermal coupling study of each pair can be extended to the other pair.

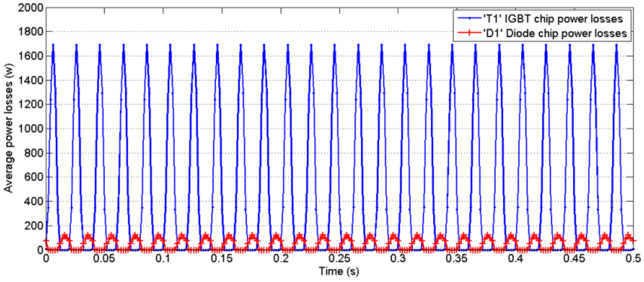


Fig. 5. Average power losses in the IGBT module.

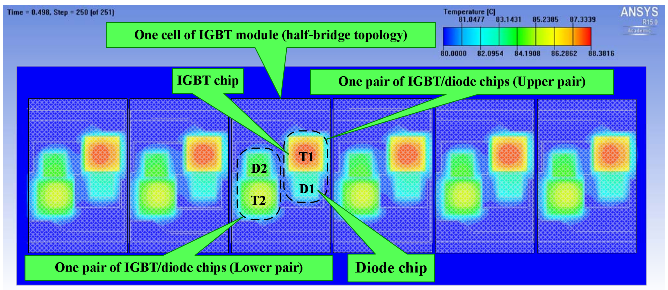

Time = 0.498, Step = 250 (of 251)
Temperature [C]
81.0477
83.1431
85.2385
87.3339
80.0000
82.0954
84.1908
86.2862
88.3816
ANSYS
R15.0
Academic
One cell of IGBT module (half-bridge topology)
IGBT chip
One pair of IGBT/diode chips (Upper pair)
T1
D1
D2
T2
One pair of IGBT/diode chips (Lower pair)
Diode chip

Fig. 6. Temperature distribution in 6 cell IGBT module in a real operating condition.

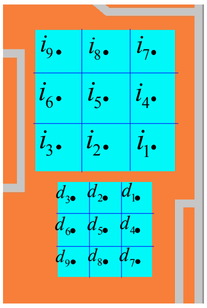


Fig. 7. Temperature monitoring points on IGBT and diode chips.

It can be seen from Fig. 6 that temperature is not uniformly distributed on the substrate, so for a better temperature monitoring on the chip surfaces, nine equally distanced monitoring points are considered on IGBT chip and diode chip areas. These monitoring points are shown in Fig. 7.

The simulations are executed in three distinctive cases: 1. T1 is conducting; 2. D1 is conducting; 3. T1 and D1 are conducting alternatively. The results for 3 the monitoring points of i_2, i_5 and i_8 on the IGBT chip and d_2, d_5 and d_8 on the diode chip are shown in Fig. 8. As it can be seen in Fig. 8 (a), (b) and (c), IGBT chip has very low impact of thermal-coupling from diode chip. On the contrary, in Fig. 8 (d), (e) and (f), the diode chip gets more considerable thermal-coupling impacts from the IGBT chips, especially for the points $(d_1 - d_3)$, which is more closer to the IGBT chip. This un-paired thermal-coupling between IGBT chip and diode chip is mainly due to the smaller size of the diode and much higher losses in the IGBT. From the discussion, it can be concluded that the thermal-coupling impact from diode chip to IGBT chip is negligible and a unidirectional thermal-coupling can be considered from the IGBT chip to the diode chip.

IV. THERMAL COUPLING IMPEDANCES

In this section the concept of thermal-coupling impedance between the chips will be explained. Generally, the temperature rise over a power module is proportional to the power losses generated in the chips. The temperature rise on a location of the device in static conditions can be defined by processing the thermal resistance, R_{th}, between the target location on the device and a reference point. Similarly, in dynamic conditions, the temperature rise can be calculated by processing the transient thermal impedance, $Z_{th}(t)$, between the target point and the reference point. The thermal resistance and the thermal impedance terms can be calculated by (1) and (2) respectively.

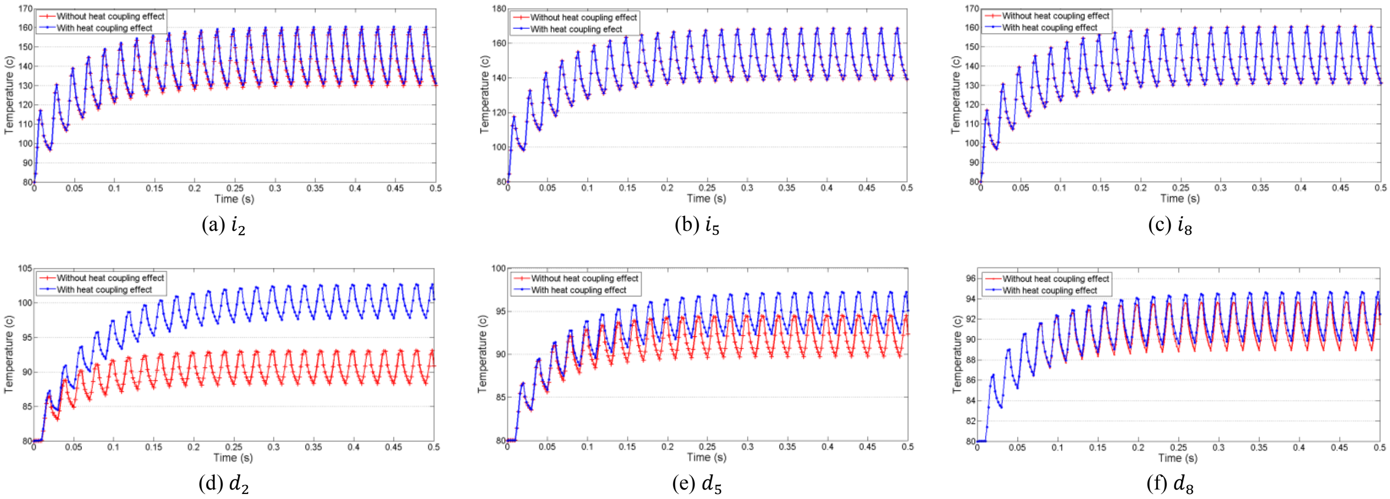
$$R_{th} = \frac{\Delta T}{P} \tag{1}$$

$$Z_{th}(t) = \frac{\Delta T(t)}{P} \tag{2}$$

where ΔT is the temperature rise to a predefined reference point and P is the power loss. As it was discussed in section III, the temperature rise in a chip is originated both from self-heating and cross-coupling heating from other chips. To include this behavior (2) can be extended to (3).

$$\begin{bmatrix} T_1 \\ T_2 \\ \cdots \\ T_m \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1n} \\ Z_{21} & Z_{22} & \cdots & Z_{2n} \\ \cdots & \cdots & & \cdots \\ Z_{m1} & Z_{m2} & \cdots & Z_{mn} \end{bmatrix} \cdot \begin{bmatrix} P_1 \\ P_2 \\ \cdots \\ P_n \end{bmatrix} + \begin{bmatrix} T_{ref1} \\ T_{ref2} \\ \cdots \\ T_{refk} \end{bmatrix} \tag{3}$$

where, T_m is the monitoring point temperature, P_n is the power loss on each chip, T_{refk} is the reference temperature to the monitoring point, Z_{mm} is the self-heating thermal impedance and Z_{mn} is the heat-coupling thermal impedance between the monitoring point and the reference point. The method which is done in this paper is to inject a step power loss to each chip separately and to monitor the temperatures on the same chip and the other chips. To find the self-heating thermal impedance, the temperature difference between the target point in a chip and the reference point (e.g. case temperature) is divided to the power loss generated in the same chip. To calculate the cross-coupling thermal impedance, power loss is injected to a chip, e.g. T1 and the temperature is measured on the other chip, e.g. D1. Then the temperature difference between T1 and D1 will be divided to



(a) i_2 (b) i_5 (c) i_8

(d) d_2 (e) d_5 (f) d_8

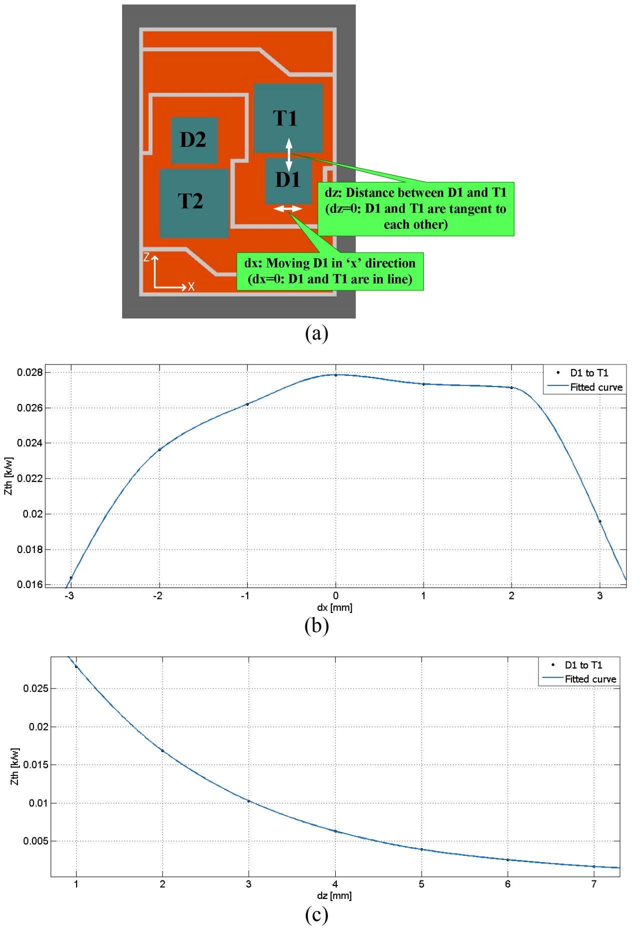
Fig. 8. Transient temperature on selected monitoring points with and without considering the thermal coupling effect.

the power loss generated in T1. This calculation can be done for all 4 chips in one section to find all thermal impedances and fill the thermal impedance matrix in (3).

V. HEAT-COUPLING THERMAL RESISTANCE AND CHIP POSITIONS

Commonly IGBT module manufacturers demand for package design which is compact in size and can withstand higher temperatures and adverse thermal cycling. This design can increase the power density and reliability of power module. On the other hand, there are some constraints in the design of power module packaging. Electrical parasitcs, e.g. stray inductances, is one of the constraints which limit the designer to place the chips far from each other. In addition, the chips cannot be placed that much far from each other to decrease the thermal cross-coupling impedances because it is unlike the compact design of power modules. Therefore, defining the thermal cross-coupling impedances with the chip locations and distances can be useful for power module package designers. In the following, the heat-coupling thermal resistances between the chips of power module, which was explained in section II, are identified with respect to distance between the chips.

In the first simulation, the step power loss is injected to T1 and the heat-coupling thermal resistance is calculated from D1 to T1. T2 and D2 are not conducting to see thermal coupling effect between T1 and D1. D1 is moved vertically and horizontally as it is shown in Fig. 9.a. 'dx' stands for moving D1 horizontally, so dx=0 means D1 and T1 are in line. 'dz' stands for moving D1 vertically, so it means the distance between D1 and T1 and dz=0 means D1 and T1 are tangent to each other. The thermal resistance results are shown in Fig. 9.b and Fig. 9.c. The results show that thermal coupling is higher when both chips are in line and closer to each other.



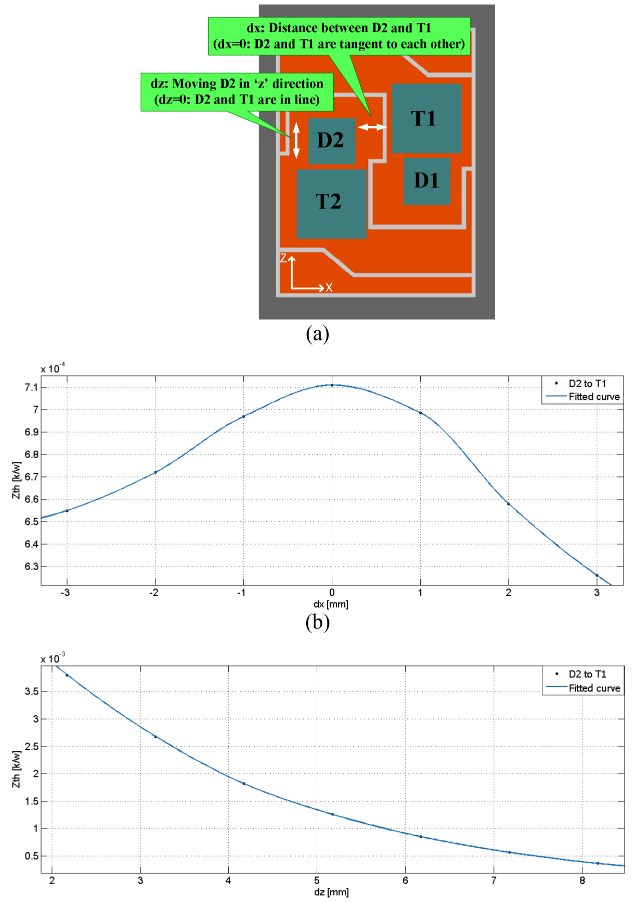
(a)

(b)

(c)

Fig. 9. Heat-coupling thermal resistance between D1 and T1: (a) schematic view; (b) moving D1 in x direction; (c) moving D1 in z direction.

Similarly, the simulation is repeated for T1 and D2. As it is shown in Fig. 10.a, D2 is moved vertically and horizontally to find the heat-coupling thermal resistance between D2 and T1. 'dx' in this figure means distance between D2 and T1, so dx=0 means D2 and T1 are tangent to each other. 'dz' stands for moving D2 vertically, so dz=0 means D2 and T1 are in a line. The step power is injected to T1 and the heat-coupling thermal resistance is calculated from D2 to T1. The results are shown in Fig. 10.b and Fig. 10.c. As it can be seen, the maximum thermal resistance when D2 and T1 are in a line is much less than the case when D1 and T1 are in a line.



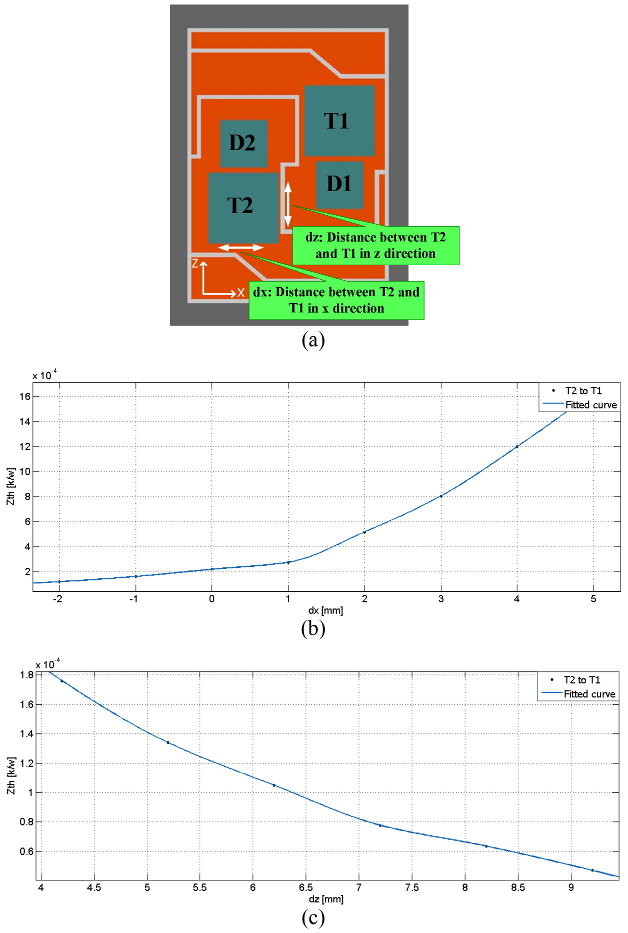
(a)

(b)

(c)

Fig. 10. Heat-coupling thermal resistance between D2 and T1: (a) schematic view; (b) moving D2 in x direction; (c) moving D2 in z direction.

The last simulation is done to find the heat-coupling thermal resistance between T2 and T1. This case is shown in Fig. 11. 'dx' and 'dz' stands for moving T2 horizontally and



(a)

(b)

(c)

Fig. 11. Heat-coupling thermal resistance between T2 and T1: (a) schematic view; (b) moving T2 in x direction; (c) moving T2 in z direction.

vertically, respectively. The simulation results are shown in Fig. 11.b and Fig. 11.c. As it is seen from this figure, the heat-coupling thermal resistance for T2-T1 is much less than two other cases.

VI. SIMPLIFIED 3D THERMAL IMPEDANCE NETWORK

In the previous sections the concept of heat-coupling thermal impedance was explained and the relationship between the heat-coupling thermal impedance and the distance between the chips were identified. In this section, a three dimensional thermal network can be extracted. This thermal network can be used in any circuit simulator in a fast way to find the detailed temperatures on different locations on the chips and solder layers. In addition, this thermal network includes thermal-coupling effects between the chips that can be significant in higher powers and shorter distances between the chips. The thermal network is shown in Fig. 12. In this figure, *j* stands for the junction layer. *S1*stands for the chips solder layer and *s2* stands for the baseplate solder layer. $\mathrm{Z}_{\mathrm{th(a-b)}}^{\mathrm{im}}$ and $\mathrm{Z}_{\mathrm{th(a-b)}}^{\mathrm{dm}}$ are thermal impedances of point m between layer *a* and layer *b* for IGBT chip and diode chip respectively. $\mathrm{Z}_{\mathrm{th(a-b)}}^{\mathrm{(im-coupl)}}$ and $\mathrm{Z}_{\mathrm{th(a-b)}}^{\mathrm{(dm-coupl)}}$ stand for cross-coupling thermal impedance of the points m between the layer *a* and the layer *b* for the IGBT chip and the diode chip respectively.

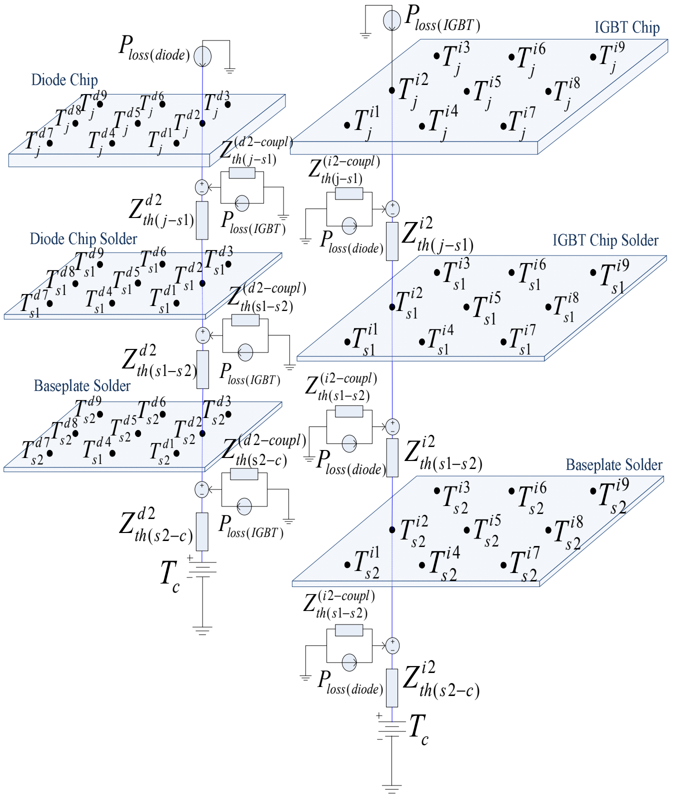

$P_{loss(IGBT)}$
IGBT Chip
$P_{loss(diode)}$
Diode Chip
T_j^{i1} … T_j^{i9}
T_j^{d1} … T_j^{d9}
$Z_{th(j-s1)}^{(d2-coupl)}$
$Z_{th(j-s1)}^{(i2-coupl)}$
$Z_{th(j-s1)}^{d2}$
$Z_{th(j-s1)}^{i2}$
Diode Chip Solder
IGBT Chip Solder
T_{s1}^{i1} … T_{s1}^{i9}
T_{s1}^{d1} … T_{s1}^{d9}
$Z_{th(s1-s2)}^{(d2-coupl)}$
$Z_{th(s1-s2)}^{(i2-coupl)}$
$Z_{th(s1-s2)}^{d2}$
$Z_{th(s1-s2)}^{i2}$
Baseplate Solder
T_{s2}^{i1} … T_{s2}^{i9}
T_{s2}^{d1} … T_{s2}^{d9}
$Z_{th(s2-c)}^{(d2-coupl)}$
$Z_{th(s1-s2)}^{(i2-coupl)}$
$Z_{th(s2-c)}^{d2}$
$Z_{th(s2-c)}^{i2}$
T_c

Fig. 12. 3D thermal impedance network for a pair of IGBT/diode chips (Thermal network is shown for i_2 and d_2; all the other measurement points share the same thermal network configuration).

To extract the thermal impedance between each two layers, in FEM software, step power loss is injected to the IGBT chip or the diode chip and temperatures are monitored between the two layers when the same chip or the other chip is conducting for the self-heating and the cross-coupling heating cases. Then the thermal impedance curves are extracted as it was discussed in section IV. The thermal impeadcne curves are mathematically curve-fitted to tfind an RC equivalent thermal network. The equivalent thermal model which is used in this paper is Foster network. The RC values are extracted using (4). It must be mentioned that (4) is presented for 4 layers of RC pairs and it can be modified to higher level or lower level depending on fitting accuracy of the fitted curve.

$$Z_{th}(t) = R_1.\left(1 - e^{-\left({t}/{R_1.C_1}\right)}\right) + R_2.\left(1 - e^{-\left({t}/{R_2.C_2}\right)}\right) + R_3.\left(1 - e^{-\left({t}/{R_3.C_3}\right)}\right) + R_4.\left(1 - e^{-\left({t}/{R_4.C_4}\right)}\right) \tag{4}$$

where R_i values stand for thermal resistance and C_i values stand for thermal capacitance in each layer. For better clarification of thermal impedance network extraction, Fig. 13 shows a block diagram with whole process.

VII. CONCLUSION

In this paper the heat-coupling effect and its importance in calculation of temperatures in high power modules was

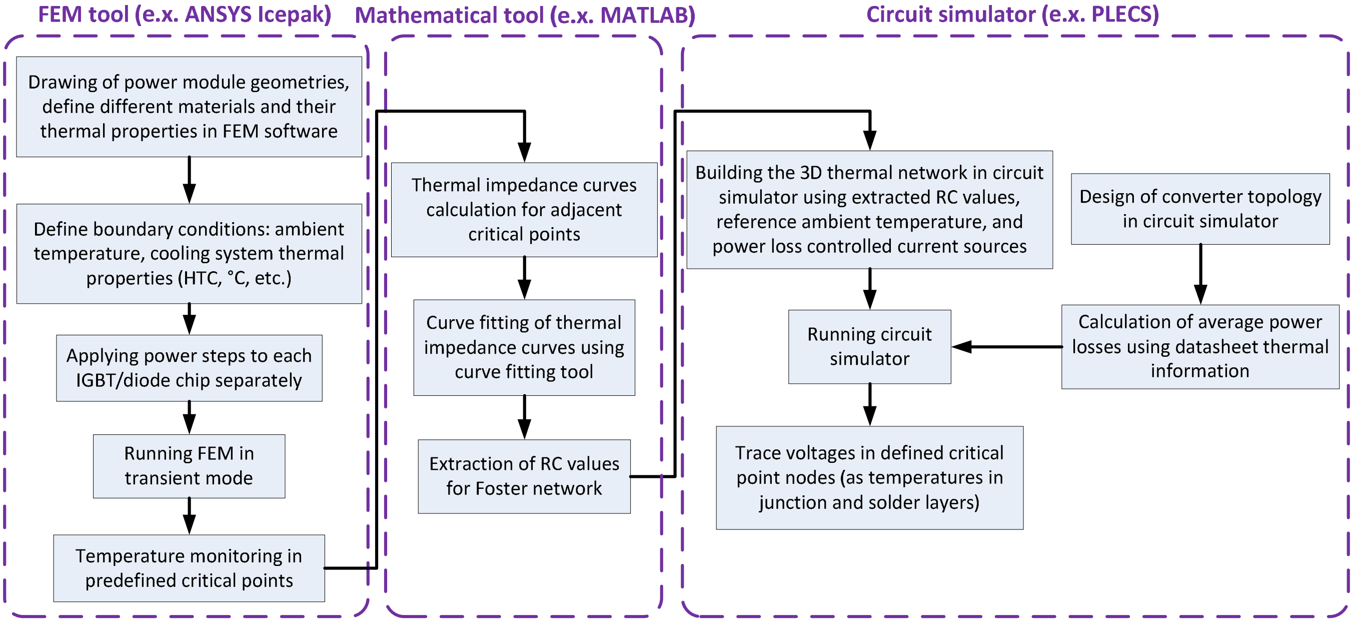

FEM tool (e.x. ANSYS Icepak)
Mathematical tool (e.x. MATLAB)
Circuit simulator (e.x. PLECS)
Drawing of power module geometries, define different materials and their thermal properties in FEM software
Define boundary conditions: ambient temperature, cooling system thermal properties (HTC, °C, etc.)
Applying power steps to each IGBT/diode chip separately
Running FEM in transient mode
Temperature monitoring in predefined critical points
Thermal impedance curves calculation for adjacent critical points
Curve fitting of thermal impedance curves using curve fitting tool
Extraction of RC values for Foster network
Building the 3D thermal network in circuit simulator using extracted RC values, reference ambient temperature, and power loss controlled current sources
Running circuit simulator
Trace voltages in defined critical point nodes (as temperatures in junction and solder layers)
Design of converter topology in circuit simulator
Calculation of average power losses using datasheet thermal information

Fig. 13. Block diagram of thermal impedance network extraction process

discussed. It was shown that temperature calculations by the datasheet may give wrong results if heat-couplings are neglected. In addition, dependency of cross-coupling thermal impedance to the distance between the chips was studied for different distances and a design map was suggested for cross-coupling thermal impedances in respect to the distance between the chips. Finally a simplified 3D thermal network was presented which can be used in any circuit simulator considering the heat-coupling effects. This thermal network can give more accurate temperatures without need to run long FEM simulations for long-term load profiles.

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