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Published in:
Proceedings of the 31st Annual IEEE Applied Power Electronics Conference and Exposition (APEC)

DOI (link to publication from Publisher):
10.1109/APEC.2016.7468292

Publication date:
2016

Document Version
Accepted author manuscript, peer reviewed version

Electrical Parasitics and Thermal Modeling for Optimized Layout Design of High Power SiC Modules

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***Abstract*—The reliability of power modules is closely depended on their electrical and thermal behavior in operation. As power modules are built to operate more integrated and faster, the electrical parasitic and thermal stress issues become more critical. This paper investigates simplified thermal and parasitic inductance models of SiC power modules. These models can replace the models by Finite Element Methods (FEM) to predict temperatures and electrical parasitics of power modules with much faster speed and acceptable errors and will be used for study of real operation of power modules. As a case study, the presented models are verified by a conventional and an optimized power module layout. The optimized layout is designed based on the reduction of stray inductance and temperature in a P-cell and N-cell half-bridge module. The presented models are verified by FEM simulations and also experiment.**

Keywords—Electrical parasitic modeling, thermal modeling, SiC power module, optimization, reliability.

I. INTRODUCTION

In recent years power electronic devices have found wide applications in renewable energy systems, electric drives and automation. Since industries demand for higher power densities and higher efficiencies, power electronic systems need to be designed more integrated and operate at higher switching frequencies [1]. However, SiC power modules as fast growing devices, which can operate in higher frequencies in more dense packages, may be exposed to more reliability problems. Integration of semiconductor chips increases the temperatures due to thermal coupling of the chips that may lead to bond-wire lift-off or solder cracking [2], [3]. Moreover, poor layout design such as distancing the semiconductor chips in the power module increases the parasitic inductances that lead to voltage spikes and ringing with the parasitic capacitances of the device [4]. Therefore, a poor layout design of the power module may lead to severe thermal stress, severe turn-off overvoltage of the chips and electromagnetic interference problems that seriously affect the reliable operation of the power module [5].

In conventional power modules, stray inductances are mainly introduced by power module terminals, copper trace on the upper layer of Direct Copper Bonding (DCB) and chip bond-wires. A lot of efforts have been made to optimize the layout of power module with minimized parasitic inductances. For power module electrodes, laminated busbar structure has been adopted, which will considerably reduce the stray inductance of electrodes [6]. The common approach to reduce the copper trace stray inductance is to widen the trace width and shorten the trace length. Moreover, the typical method to reduce bond-wires stray inductances are shortening the wire length and increase the number and diameter of wires [7]. However, thermal management of power module becomes an important issue as the power module package becomes more compact and the heat spread capability decreases. Therefore, a trade-off should be made in thermal and electrical design of the power module layout [8].

Currently, the optimized layouts for power module are achieved by multidisciplinary design tools which integrate several commercial software tools that in turn demand for high computational time and effort [9]. Some power module design and evaluation tools are based on 3D modeling and Finite Element Analysis (FEA) to extract the electrical parasitics and temperatures of the power module [10]. These tools are usually time-consuming if re-design process is targeted to achieve minimized parasitics and temperature of layout. On the other hand, many analytical and lumped models have been introduced to estimate the temperatures and electrical parasitic parameters in the power modules [11]-[14]. However, there is a lack of effort for multidisciplinary modeling of power modules that can evaluate the optimized layout and electro-thermal parameters in a transient model, which can be used in reliability studies. Some software tools have been developed, which provide simple parasitics and thermal models and are also used for automatic layout design. For example in [8] PowerSynth, a power module layout design tool, is introduced where simplified electrical parasitics models based on micro-strip transmission line structure and thermal models based on a thermal spreading angle approach have been applied to evaluate the layout of the power module. Using a multi-objective optimization such as genetic algorithm, the best solution for minimized switching loop inductance and chip temperatures depending on the application is achieved. Then, by using simplified thermal and parasitics models, a fast evolution of the designed layouts can be implemented for the redesign process.

This paper investigates a simplified geometry-dependent commutation loop inductance index to evaluate a commercial SiC half-bridge power module and the optimized layout. The optimized layout is designed based on P-cell and N-cell layout structure, which is explained in [7] and is optimized by the Non-dominated Sorting Genetic Algorithm II (NSGA-II) procedure [15]. A simplified index to evaluate the stray inductance of both layouts is used and compared for the main switching loops. Then by applying a 3D lumped thermal network that includes the thermal cross coupling effects, the thermal stress on the chips will be identified for steady-state and also dynamic operation. The optimized layout will be validated by FEA as well as experiments.

II. Stray Inductance Evaluation Index

As previously described in [7], P-cell and N-cell structure for phase-leg in inverters has some benefits rather than traditional phase-leg anti-parallel diode structure. Fig. 1 shows the schematics of the two configurations. Under inductive load operation as shown in Fig. 1 (a), the current commutates between S1 and D2when the current direction is from positive DC bus to negative DC bus or between S2 and D1 when the current direction is from negative DC bus to positive DC bus. Traditionally, the anti-parallel diodes are either packaged within the transistors or placed closely in parallel. However, as it is shown in Fig. 1 (b), it is more reasonable to use a P-cell N-cell structure by pairing the upper anti-parallel diodes with lower transistors and lower anti-parallel diodes with higher transistors. So, the load current flows into the N-cell and flows out through the P-cell. The stray inductances exist all over the phase-leg current commutation path as shown in Fig. 1. The closer the devices in each current commutation path are paired together, the lower the stray inductance between the devices. This lower stray inductance reduces the inductive voltage spikes seen across the transistor, while undergoing a turn-off commutation and current overshoot during turn-on.

Usually it may be time-consuming and costly to use FEA software tools for calculation of stray inductances in the complex design of power module layouts. In the design stage of a power module, the designer may try several layouts and calculate the stray inductances by FEA tool, which is too time-consuming. So a simple stray inductance model is needed for fast evaluation of layouts. For simplification, all commutation paths on the substrate are considered as homogenous conductors with similar cross-section area, which is very small compared to the length of conductors. In the power module, the critical commutation paths are open loops, which makes the calculation of their stray inductances more complicated compared to closed loops. Using the principles of partial inductances, the stray inductance in the conductors is calculated by adding a closing path to the open loop [16]. The self-inductance of a single-turn rectangular loop is calculated by

$$L=\frac{\mu_0}{\pi}\left[-2(w+h)+2\sqrt{h^2+w^2}+h\ln\left(\frac{w}{h+\sqrt{h^2+w^2}}\right)\right.$$
$$\left.+w\ln\left(\frac{h}{w+\sqrt{h^2+w^2}}\right)+h\ln(\frac{h}{d})+w\ln(\frac{w}{d})\right]\times10^{-3} \quad (1)$$

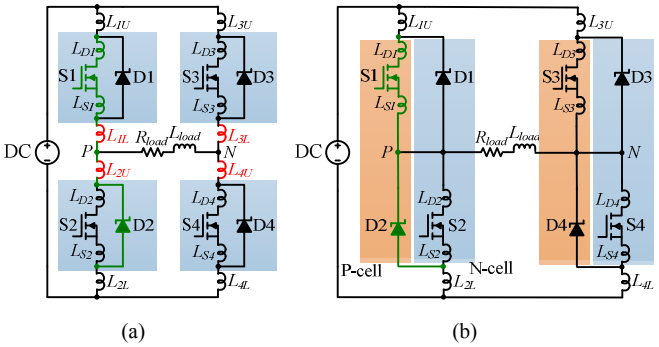


Fig. 1. Circuit schematic showing package parasitics. (a) Conventional inverter, (b) P-cell N-cell phase-leg inverter.

where w and h are the width and height of the rectangular loop in mm, d is the diameter of the loop cross section in mm ($d<<w,h$), μ_0 is the vacuum permeability, and L is the loop inductance in Henry.

The partial self-inductance of a single straight conductor is given by [10]

$$L=\frac{\mu_0 l}{2\pi}\left(\ln\frac{2l}{d}-1\right)\times10^{-3} \quad (2)$$

where l is the length of the conductor in mm, and d is the diameter of the conductor cross section ($d<<l$) both in mm. From eq. (2), and assuming $d<<w,h$, the self-inductance of a rectangular loop is approximated by

$$L\approx\frac{\mu_0}{\pi}(w+h)\cdot\ln(w\cdot h)\times10^{-3}$$
$$=\frac{\mu_0}{2\pi}\cdot C\cdot\ln(S)\cdot10^{-3} \quad (3)$$

where $C=2\cdot(w+h)$ is the perimeter of the loop in mm, and $S=w\cdot h$ is the area of the loop in mm^2. So the self-inductance of the rectangular loop is linearly proportional to $C\cdot\ln(S)$. As derived from eq. (2), and assuming $d<<l$, the self-inductance of a single straight conductor is approximated by

$$L\approx\frac{\mu_0}{2\pi}\cdot l\cdot[\ln(2l)-1]\cdot10^{-3} \quad (4)$$

In order to simplify the model for calculation of the partial inductance of the commutation loop, the shortest closing path, which is a straight line between two ends of the open loop, is chosen [17]. In the presented model, the mutual inductance associated with the path is neglected and only the partial self-inductance is taken into account. Consequently, by subtracting the partial self-impedance from the inductance of the closed commutation loop, the inductance of the open loop between the intended points is achieved. Here, by using eq. (3) and eq. (5), an index is derived to evaluate the inductance of the commutation loop.

$$\alpha=C\cdot\ln(S)-l\cdot[\ln(2l)-1] \quad (5)$$

In a commutation loop, a large value of the index α indicates large stray inductance. So, in the substrate layout design for the power module, the purpose is to minimize the α values of the commutation loops. However, due to the assumptions and approximations adopted, the index α is not used for an accurate stray inductance calculation and it is used as a scale for comparison between the stray inductances of different layout designs.

III. 3D Thermal Modeling

In this paper, both transient and steady-state thermal behaviors are focused for thermal evaluation of the power module. The method for modeling the transient operation is based on 3D thermal network [18]. The 3D thermal network includes 9 temperature monitoring points in the junction layer, die attach layer and substrate attach layer. For simplification, a simplified model including the junction and case layers is shown in Fig. 2. The network extraction method is based on step response analysis, i.e. applying volumetric step power loss to the semiconductor chips in the FEA software and identification of the temperature responses on the monitoring points. Then the transient thermal impedance between the aforementioned layers are identified by

$$Z^{self}_{th(a-b)}(t) = \frac{T_a(t) - T_b(t)}{P_{self}} \tag{6}$$

where $Z^{self}_{th(a-b)}(t)$ is the transient self-thermal impedance between adjacent layer '*a*' and '*b*', T_a and T_b are temperatures in the two aforementioned layers and P_{self} is the power loss generated in the chip. Moreover, the thermal coupling effect is considered in the 3D thermal network. The transient coupling-thermal impedance is given by

$$Z^{coupl}_{th(a-b)}(t) = \frac{T_a(t) - T_b(t)}{P_{coupl}} \tag{7}$$

where $Z^{coupl}_{th(a-b)}(t)$ is the transient coupling-thermal impedance between adjacent layer '*a*' and '*b*' and P_{coupl} is the power loss generated in the neighbor chips. As using FEA simulation is time-consuming for transient long-term studies, circuit simulator is used for temperature calculation. In order to use the 3D thermal network in the circuit simulator, the derived transient thermal impedance curves by eq. (6) and eq. (7) are curve-fitted mathematically using a sum of exponential functions in order to obtain an equivalent lumped RC thermal network in the Foster configuration

$$Z^{self}_{th}(t) = \sum_{i=1}^{n} R^{self}_{th_i} \cdot (1 - e^{-t/R^{self}_{th_i} \cdot C^{self}_{th_i}}) \tag{8}$$

where R^{self}_{thi} is the equivalent thermal resistance and C^{self}_{thi} is the equivalent thermal capacitance when the target chip is powered. Similarly the equivalent mathematical model for the transient coupling-thermal impedance is given by

$$Z^{coupl}_{th}(t) = \sum_{i=1}^{n} R^{coupl}_{th_i} \cdot (1 - e^{-t/R^{coupl}_{th_i} \cdot C^{coupl}_{th_i}}) \tag{9}$$

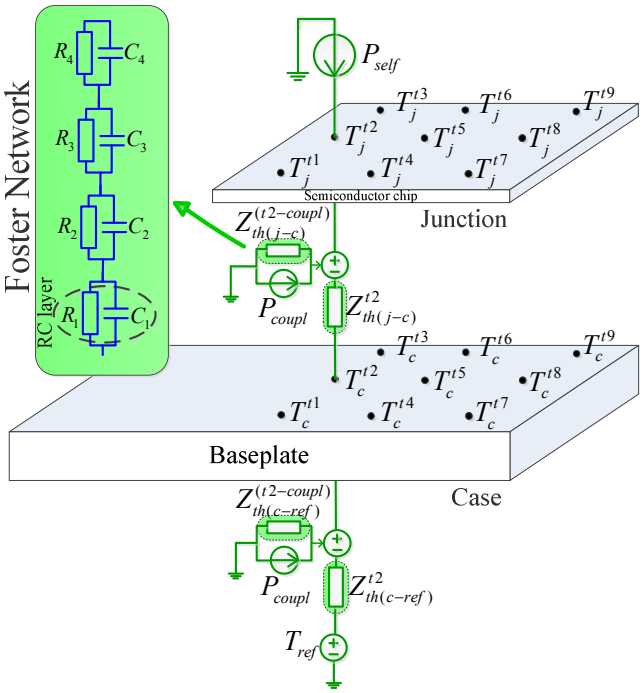


Fig. 2. 3D thermal network structure from chip (junction) to reference (cooling system).

where R^{coupl}_{thi} is the equivalent thermal resistance and C^{coupl}_{thi} is the equivalent thermal capacitance, when the neighbor chips are powered. The equivalent Foster network is highlighted in Fig. 2. In this work, the equivalent thermal impedance curves are fitted by four layers of RC elements for better accuracy. It should be mentioned that all RC elements are flexible by the variation of temperature, power loss and cooling system. By shortening the distance between the chips, thermal coupling effects and thus temperature become higher. So, the thermal coupling impedances are used to evaluate the distance of the chips to each other.

IV. Substrate Layout Design Based on P-cell N-cell Concept

The main optimization objectives for design of the power module layout include minimization of 5 main criteria: loop inductance in the current path from the positive DC terminal to the negative DC terminal, loop inductance from the load terminal to the positive DC terminal, loop inductance from the load terminal to the negative DC terminals, steady-state maximum device temperature and temperature variation of the device. By minimizing the total stray inductances from the positive DC terminal to the negative DC terminal, the inductance of both current commutation paths from load terminal to positive and negative terminals are simultaneously minimized. Therefore, it merges the related optimization criterion to one. Reducing the steady-state maximum temperature and dynamic temperature variation are also helpful in terms of increasing the reliability and thermal stability of the power module. Generally, the lower the operating temperature of the devices, the lower thermal expansion and Coefficient of

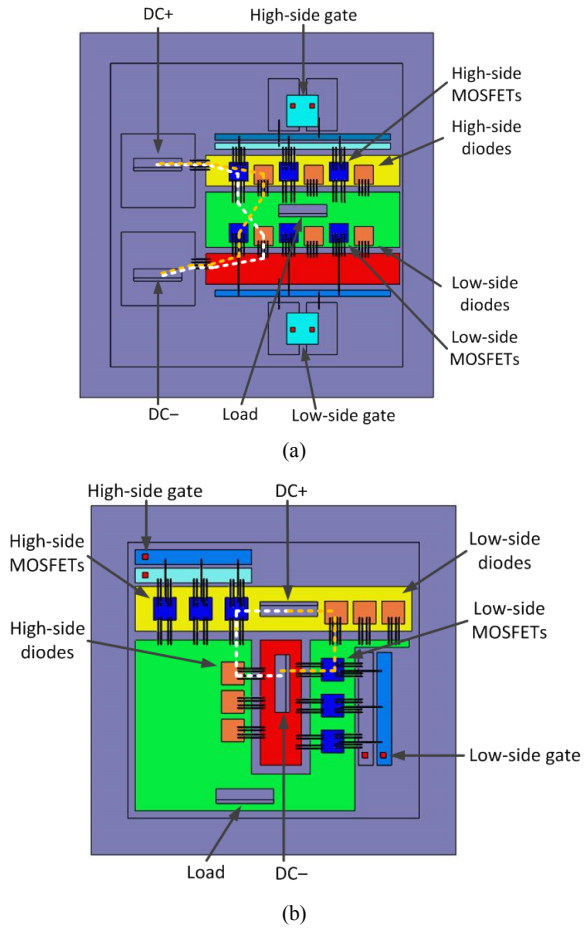


Fig. 3. Substrate layout designs for a 1200V/100A module. (a) conventional module, (b) P-cell N-cell based module

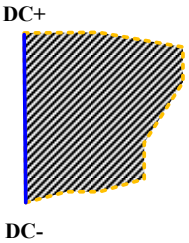
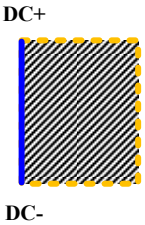
Thermal Expansion (CTE) mismatch between the device and sub-layers.

In this section, two different substrate layout designs for a 1200V/100A (at 25 °C) SiC half-bridge inverter module with separate anti-parallel diodes are studied: one conventional layout and one adopting P-cell N-cell layout. Adding anti-parallel diodes separately to the MOSFET chip allows for reduction of stray inductance in the package using the P-cell N-cell technique. Conventionally the anti-parallel diode is either embedded within the MOSFET packages or placed closely with them. In the P-cell N-cell technique, the stray inductance of the main current commutation loop in a module is reduced. This technique is performed by pairing the upper MOSFETs with the lower anti-parallel diodes and vice-versa. The closer these devices are paired together, the lower the stray inductance in the current commutation loop. This lower inductance reduces the voltage spikes across the MOSFET during a turn-off event and current overshoot during the turn-on event.

A. Electrical Parasitics Evaluation

The power module under study includes a total of 6 MOSFETs and 6 anti-parallel diodes in the design (3 pairs for the high side of the phase-leg and 3 pairs for the low side of the

TABLE I. COMMUTATION LOOPS AND STRAY INDUCTANCE OF CONVENTIOANL MODULE AND P-CELL N-CELL BASED MODULE.

Module Layout	**Conventional Layout**	**P-cell N-cell layout**
DC+ to DC- commutation loop		
DC+ to DC- loop dimensions	S=267.88 mm^2 C=66.8 mm l=18.48 mm	S=53.23mm^2 C=29.2 mm l=7.3 mm
Stray inductance index (α)	α =325.21	α=103.77
Extracted stray inductances (L)	12.8 nH	9 nH

phase-leg). As the module is a half-bridge topology, only a single phase-leg inverter is implemented. The MOSFETs used in the design are CREE CPM2-1200-0080B and the diodes are CPW4-1200S020B. The power MOSFET chips and Schottky diode chips used for the half-bridge modules have the ratings of 1200V/36A and 1200V/20A respectively. The baseplate and substrate dimensions are constrained to a fixed size. ANSYS Q3D is used to initially design the layout of the P-cell N-cell based layout. Then, by using the NSGA-II optimization procedure used in the power module design tool, PowerSynth, the optimization of the layout in terms of device placement, trace widths/lengths are performed. In the optimization procedure, the position of the chips, size and dimension of traces are changed in order to get the best solution. Fig. 3 shows two layouts designed based on the conventional device pairing and the optimized P-cell N-cell based device pairing. The critical commutation paths of two designed layouts are highlighted with dashed lines of different colors on the layout. To form the commutation paths, soldering positions of the terminals and chips on the substrate have been denoted. The current commutation loops including the closing paths, the geometrical dimensions and the related inductance index α are given in Table I. Both the designed layouts have been imported in the ANSYS Q3D Extractor to calculate the stray inductances in the switching loops. As a high critical frequency of turn-off current for the present SiC MOSFET, the simulations have been implemented by using a 50 MHz AC excitation [17].

It can be seen in Table I that the positive correlation between the index α and the stray inductances is valid. Moreover, the DC+ terminal to DC- terminal stray inductance values confirm that the lowest overall loop inductance is the P-cell N-cell layout. In the P-cell N-cell layout, the actual commutation devices (S1/D2 and S2/D1) are placed closer to

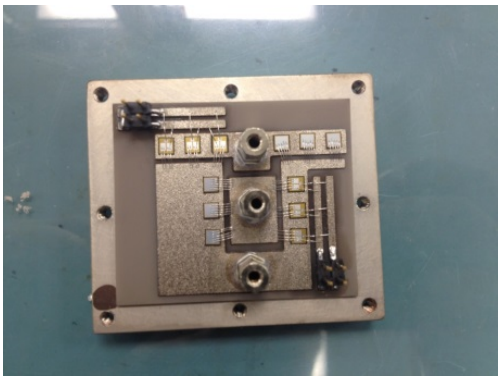


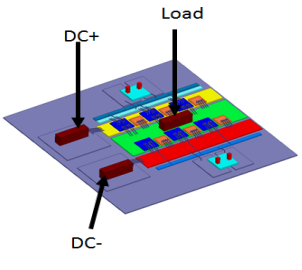
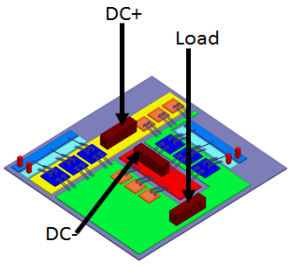
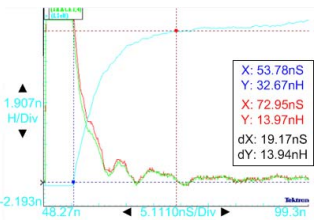
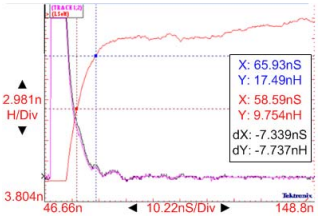
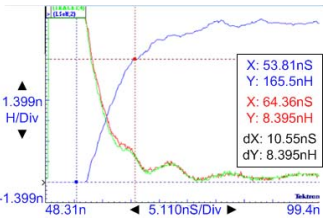
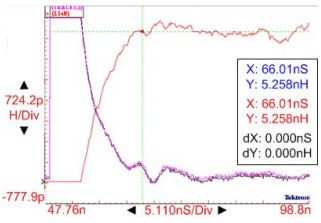
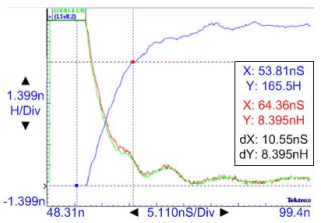
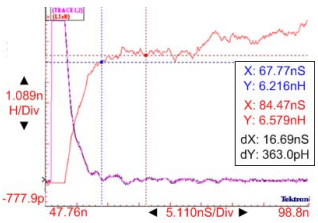
Fig. 4. Optimized SiC power module layout based on P-cell N-cell techniques.

Fig. 5. Experimental measurement setup; Oscilloscope 11801B connected to SD-24 sampling head, terminated with 50Ω impedance and PC (loaded with IPA310 software) interfaced with oscilloscope.

each other. So the P-cell N-cell layout configuration significantly reduces the loop inductance rather than the conventional layout. Moreover, to confirm for the other current loops, the stray inductance values for DC+ terminal loop to the load terminal and DC- terminal to the load terminal are listed.

For verification, a sample module designed by the studied layout has been fabricated that is shown in Fig. 4. Tests of the switching characteristics of the MOSFETs have been done upon the sample modules in a Time Domain Reflectometer (TDR) test bed. The experimental setup is shown in Fig. 5. Parasitics are extracted for the power modules using the TDR method in the form of differential inductance waveforms, from which the absolute parasitic values are computed using IPA310 software. The TDR method involves propagation of a high frequency step signal (incident signal) through the Region of Interest (ROI) in Device under Test (DUT) and capturing the reflected signal. The captured incident, reflected, shorted waveforms are monitored and the corresponding resultant impedance and parasitic inductance waveforms. The frequency in the level of 50 MHz is used for the measurement. High frequency is critical for the small inductance to get measurable impedance. So when a current is applied to the stray inductance, a decent amount of voltage is provided and the accuracy of the measurement is ensured [7]. Moreover, since the wires with alligator probe introduce inductances that are comparable to the parasitic inductance in the module, a pin probe is adopted in the measurement. The parasitics with this

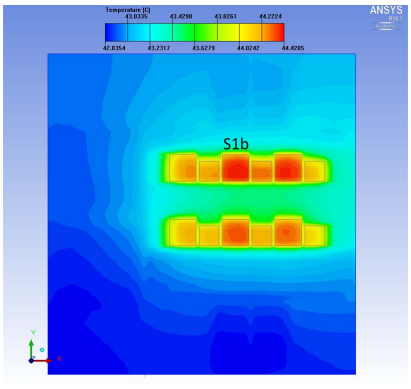
TABLE II. COMMUTATION LOOPS AND MEASURED STRAY INDUCTANCE OF CONVENTIONAL MODULE AND P-CELL N-CELL BASED MODULE.

Conventional Module	**P-cell N-cell Based Module**
	
	
L(DC+ to DC-)=13.9 nH	L(DC+ to DC-)=9.7 nH
	
L(Load to DC-)=8.3 nH	L(Load to DC-)=5.2 nH
	
L(Load to DC-)=8.3 nH	L(Load to DC-)=6.5 nH

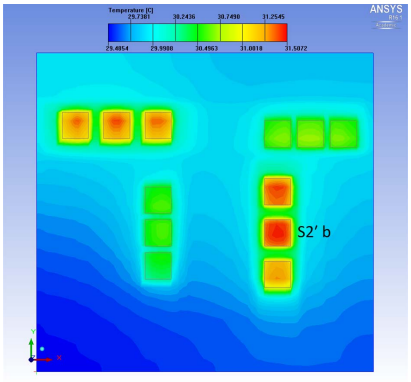
probe are small and are compensated through the calibration process. The TDR responses of the traces of three switching conditions (DC+ to DC-, load to DC+, and load to DC-) in the two layouts are shown in Table II. It can be seen from the test results that in the new layout design, the stray inductances are reduced significantly compared to the conventional layout.

B. Steady-state thermal evaluation

For thermal evaluation, the module is assumed to operate at an ambient temperature of 25 °C and at a switching frequency of 20 kHz. The bottom face of the baseplate is mounted on a heat transfer coefficient (h) of 100 W/m^2·K. The equivalent heat transfer coefficient is a measure, which stands for the amount of heat, which is transferred by convection between a



(a)



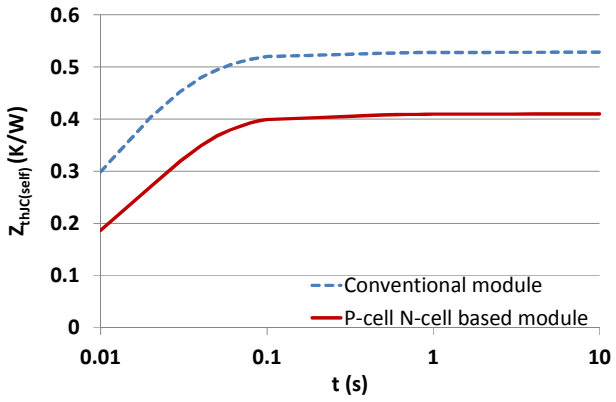
(b)

Fig. 6. Steady-state temperature profile on power modules. (a) conventional layout, (b) P-cell N-cell based layout.

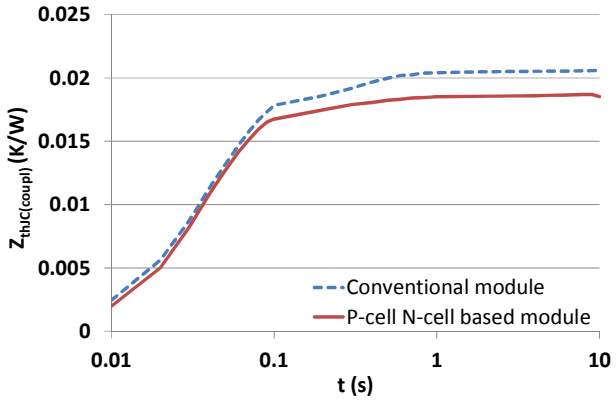
solid and a fluid [19]. So, to simplify the real cooling system, its equivalent *h* is used. Each MOSFET is estimated to dissipate 4 Watts of heat flow and each diode 2 Watts of heat flow. Both the designed layouts are imported in the ANSYS Icepak to calculate the temperatures in static condition. All materials used in the models are selected to be temperature dependent. The selected materials are: SiC for the MOSFET chips and diode chips, SAC305 for the die-attach and substrate-attach, Al_2O_3 for the DCB and Copper for the baseplate and traces. The steady-state temperatures are shown in Fig. 7. It is shown that the maximum temperature on the conventional layout is 44.4 °C, but the maximum temperature on the P-cell N-cell based layout is 31.5 °C that shows about 13°C temperature reduction. Moreover, it is seen that in the conventional layout, all chips are concentrated in the middle of the substrate that leads to an increase of temperature due to thermal coupling effects. However, in the P-cell N-cell layout, MOSFETs and diodes are dispersed and placed in positions further to each other. This enables to reduce the thermal coupling effects among the chips and to use larger area of the substrate for heat spreading. Using the P-cell N-cell layout will reduce the cooling requirements of the module, while maintaining the power density of the module.

C. *Transient thermal evaluation*

As explained in section III, for transient thermal evaluation, a 3D thermal network is used. In order to extract the thermal



(a)



(b)

Fig. 7. Extracted transient thermal impedance curves for conventional module (point S1b in Fig. 6(a)) and P-cell N-cell based module (point S2′b in Fig. 6(b)). (a) self-thermal impedance, (b) Coupling-thermal impedance.

TABALE III. THERMAL RC ELEMENTS FOR THE HOTTEST CHIP IN THE CONVENTIONAL (POINT S1B) AND P-CELL N-CELL (POINT S2′B) MODULES

Layout	Conventional module		P-cell N-cell module	
RC elements in Foster network	Self-thermal impedance (j-c)	Coupling-thermal impedance (j-c)	Self-thermal impedance (j-c)	Coupling-thermal impedance (j-c)
R1 (Ω)	0.1182	0.02049	0.2125	0.01856
C1 (F)	0.3059	2.373	0.07604	2.34
R2 (Ω)	0.07548	0	0.09747	0
C2 (F)	0.1693	0	0.4379	0
R3(Ω)	0.1645	0	0.04612	0
C3 (F)	0.007741	0	0.08218	0
R4 (Ω)	0.1697	0	0.05328	0
C4 (f)	0.03413	0	0.3016	0
Total R (Ω)	0.52788	0.02049	0.40937	0.01856

network elements, a step response analysis is implemented and the junction to case transient thermal impedance curves are extracted for the hottest chips in two layouts, which are *S1b* in the conventional module and *S2'b* in the P-cell N-cell based layout (see Fig. 6). The same conditions as the steady-state FEA simulation are applied to models. To extract the transient self-thermal impedance curves, 4 W is applied to the chips *S1b*

TABLE IV. PARAMETERS OF THE PV CONVERTER USING THE DESIGNED MODULE

Rated power P_o	40 kW
Rated load current I_{load}	80 A
DC bus voltage V_{dc}	400 V
Switching frequency f_{sw}	20 kHz
Fundamental frequency f_o	50 Hz
Grid-side power factor	1.0
Filter inductor L_1	0.35 mH
Power module	SiC MOSFET/diode 1200V/100A

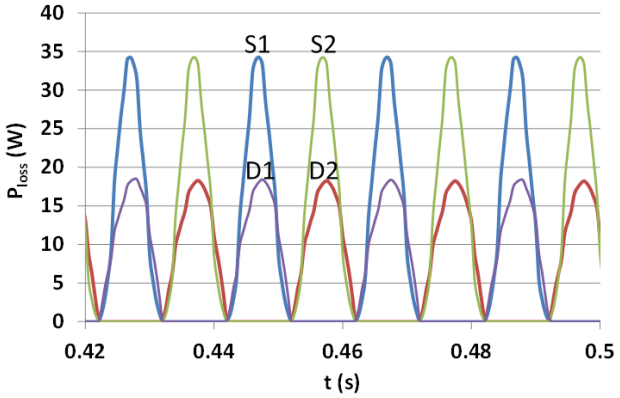


Fig. 8. Average power losses of the MOSFET chips (S1 and S2) and diode chips (D1 and D2) in the phase-leg module. For a PV-converter at 40 kW production.

and *S2'b* and the other chips are not powered. To extract the transient coupling-thermal impedance curves, *S1b* and *S2'b* are not powered, 4 W is applied to all other MOSFETs and 2 W is applied to all other diodes. By a step response analysis, the transient thermal impedance curves are extracted for a monitoring point at the center of the chip and it is shown in Fig. 7. As it is seen, by using the new layout design, it reduces the transient thermal impedance curves. In the new layout, the substrate area is used efficiently to place chips. In the new design, larger Copper traces are used that increase the heat spreading on the surface of the substrate. Moreover, since the chips are placed further, the thermal coupling effect is reduced. Depending on the different operating conditions of the power module (grid-side or converter-side devices) high-side or low-side devices experience different power losses. So, by a decrease of the thermal coupling between the chips, the thermal stress on the devices will be less and the device thermal behavior will be more independent from other devices.

In order to use 3D thermal network in a circuit simulator for fast transient thermal evaluation, RC elements in the Foster networks are extracted for both self-thermal impedances and coupling-thermal impedances (see Fig. 2). Curve-fitting of transient thermal impedance is implemented by using *cftool* in MATLAB. The extracted RC elements are shown in Table IV.

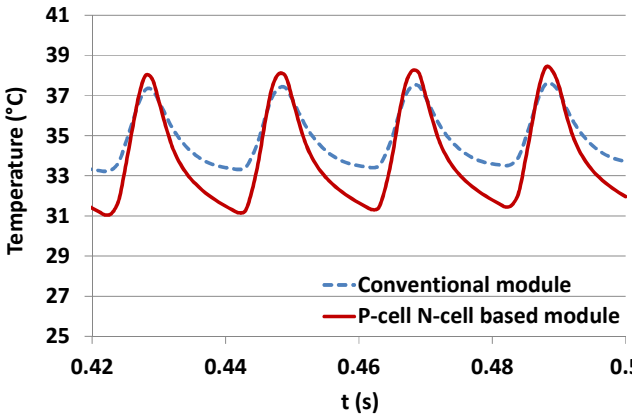


Fig. 9. Dynamic temperature profiles in the center of hottest chips in the conventional module (point S1b in Fig. 6(a)) and P-cell N-cell based module (point S2′b in Fig. 6(b)).

D. Thermal dynamic evaluation in converter application

For the transient thermal evaluation, the designed power modules are used as a phase-leg in a 40 kW grid-connected three-phase PV inverter. The parameters of the inverter are listed in Table IV. The average power losses of devices are calculated by using the datasheet of the power MOSFETs and Schottky diodes. For more accurate power loss calculations, temperature-dependent output characteristics and switching losses of the devices are imported as look-up tables in PLECS. Then by the method explained in [20], the power losses of devices are calculated. The calculated loss profiles for each high side and each low side devices are presented in Fig. 8. Although the power loss of the devices also depends on stray inductances of the main circuit and module layout design, the preliminary power loss results are helpful for the thermal evaluation of the module layout.

Using the proposed 3D thermal model, dynamic thermal behavior of the devices can be studied very fast. For this reason, the extracted RC networks are used in a circuit simulator; S1 power loss is applied as P_{self} and a summation of S2, D1 and D2 are applied as P_{coupl}. T_{ref} is defined as 25°C and the thermal network for case to reference is derived based on heat transfer coefficient of 100 W/m^2·K. Extraction of the cooling system thermal impedance curve ($Z_{th(c\text{-}ref)}$) follows the same instructions of module thermal impedance. The dynamic temperature profiles for the hottest chips in both layouts are shown in Fig. 9. This confirms both the minimum and average temperature in the device have been reduced in the P-cell N-cell module.

V. CONCLUSIONS

In this paper, simple thermal and electrical models to evaluate SiC power modules have been studied. The thermal model is based on 3D Foster network and can estimate the transient temperature of the devices accurately in a circuit simulator. Moreover, a simplified index has been used for evaluation of the stray inductances in the power module. To verify the presented models, an optimized SiC power module based on P-cell N-cell configuration has been compared with conventional module. The optimized layout shows better performance compared to the conventional module by

shortening the switching loops and distancing the chips verified by both parasitic inductance model and transient thermal model. Measured stray inductances of the conventional and optimized layouts confirm the validity of the stray inductance model. The presented methods can be used for fast pre-design evaluation of multi-chip power modules and also reliability studies in real operating conditions.

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