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Predictive Pulse Pattern Current Modulation Scheme for Harmonic Reduction in Three-Phase Multi-Drive Systems

Pooya Davari, *Member, IEEE,* Yongheng Yang, *Member, IEEE,* Firuz Zare, *Senior Member, IEEE,* and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—The majority of the industrial motor drive systems are equipped with the conventional line-commutated front-end rectifiers, and being one of the main sources of harmonics in the power line. While a parallel combination of these drive units elevates current quality issues, a proper arrangement of them can lead to the cancellation of specific harmonics. This paper proposes a new cost-effective harmonic mitigation solution for multi-drive systems using a predictive pulse pattern current modulation control strategy. The proposed technique applies suitable interaction among parallel drive units at the rectification stage to synthesize sinusoidal input currents. The input voltage sensing is avoided in order to minimize the number of required sensors, and the grid synchronization also has been implemented based on a common Phase-Locked-Loop (PLL) using the DC-link capacitor voltage ripple. Experimental results validate the effectiveness of the proposed strategy.**

***Index Terms*—Harmonic mitigation, predictive current control, motor drive, three-phase AC-DC power converters.**

I. INTRODUCTION

INHERENT switching behavior of power electronics converters has being witnessed as one of the main reasons for power quality issues. Over the years, vast of harmonic mitigation techniques have been developed and applied in conjunction with the power converters [1]-[4]. Although recent technological progresses in both power semiconductor and Digital Signal Processor (DSP) industries have changed the perception of using the active methods, the total cost and complexity are still the main obstacles in employing the prior-art active harmonic mitigation techniques.

Additionally, passive filtering methods are in effect in many applications [5]-[7]. Despite the fact that they are simple and cost-effective at low power, they are bulky, worsen the system dynamic, and may introduce resonance in the entire power system [7]-[8]. Nevertheless, coping with international standards which are continuously getting more stringent will eventually rule out their effectiveness.

Currently, according to IEC 610003-2&12 Standards [9], current harmonics and the Total Harmonic Distortion (THD_i) values generated by power electronics systems should be controlled below certain limits. The limits depend on the device specification and short circuit ratio (R_{sce}) of the system. Three-phase power electronics systems with a new specification (according to IEC 61000-3-12 [9], Tables 4 and 5) can even generate more harmonic currents to improve power quality of grids at medium voltage levels. For example, for R_{sce} = 120 and based on Table 4 in IEC61000-3-12, THD_i and the fifth current harmonic should be below 48% and 40%, respectively [9].

Nowadays, many industrial drives are equipped with three-phase line-commuted rectifiers such as diode-rectifier and Silicon-Controlled Rectifiers (SCR) with passive filtering due to their simplicity and cost-effectiveness. SCRs have revolutionized the course of power electronics technology since the invention of the thyristor on 1957. After the energy crisis of 1973, development of Adjustable Speed Drive (ASD) systems is rapidly growing by employing SCR based converters [10]. SCR has been used in many topologies for drive systems such as Current Source Inverter (CSI) and Load-Commutated Inverter (LCI) at both front-end and rear-end. Also SCR can be arranged to provide soft starting function [11]-[12].

As one of the major global electricity consumers, industrial drives are gaining considerable attention due to their high level of input current harmonics generation. Hence, the applied harmonic reduction filtering, mainly based on AC or DC inductor, needs to be improved [7], [8], [13], [14]. This problem becomes significant, when a large number of frequency converters are connected to the Point of Common Coupling (PCC).

In many applications, it is a common practice to employ parallel-connected drive units (e.g., multi-pump arrangement) as it is exemplified in Fig. 1. In this situation the application demand is met using multiple modestly sized motor units rather than one single large unit. Hence, depending on the applied control strategy such as multi-follower or multi-master the load can be shared among the drive units evenly or unevenly, respectively [15], [16]. The configuration can satisfy partial load conditions more efficiently by keeping majority of the units in standby mode. Furthermore, in order to have a

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smooth starting and decreasing stress on the electrical and mechanical parts, multi-drive configurations are commonly in use. In other words, the multi-drive arrangement can improve the system redundancy [15], [16].

Although multi-drive configuration has many advantages, but as stated above, the combination of their nonlinear characteristics can yet deteriorate the grid current quality. However, by implementing a suitable interaction among the rectification stages, it is possible to synthesize sinusoidal input currents with a high quality [17].

This paper thus tackles the aforementioned problems by introducing electronically phase-shifted input currents at each SCR unit. Moreover, a pulse pattern current modulation scheme is employed at the DC-link to further improve the input current quality by mitigating specific low order harmonics. Fig. 1 illustrates a multi-drive system arrangement, where the pulse pattern current modulation is implemented by placing a DC-DC converter at the DC-link following the electronic inductor concept [1], [2], [18]-[22]. The basic idea of electronic inductor is to replace the bulky DC-side inductor with a relatively small inductor which by incorporation of a DC-DC converter it emulates the behavior of an ideal infinite inductor. Furthermore, the performance of the current controller in tracking the preprogrammed switching angles can significantly affect the harmonic mitigation capability of the system. In order to achieve a simple but fast tracking performance, a predictive valley current control (i.e., deadbeat) method has been adopted [23], [24]. Besides its fast dynamic and simplicity, the deadbeat current control has some limitations, especially when it is applied to a SCR unit. In this paper those issues with a possible solution have been addressed. Finally, the current modulator is synchronized with the grid based on a common Phase-Locked-Loop (PLL) applied to the output voltage ripple. The proposed concept illustrates that the synchronization can be obtained without using any additional sensor and only based on the DC-link capacitor voltage ripple rather than sensing grid voltages.

It is significantly important to highlight that there is no single solution for any power electronics applications and there are many factors such as quality, reliability, cost and regulations which can affect the system design and topology. One of the main aims in this study was to apply an active filtering method as an intermediate circuit to the three-phase line-commutated rectifier systems. This way, no major modifications is required for the systems which are equipped with the three-phase line-commutated rectifier. Therefore, the proposed current modulation strategy is applied to a single-switch boost topology (i.e., DC-DC converter) operating in Continuous Conduction Mode (CCM). Notably, medium and high power drives have SCR circuits in their rectifier side in order to control the inrush current which is a very reliable and a robust solution. These drives have been used in industry for many years. Therefore the utilization of SCRs for the proposed topology has no extra cost while they can be used to improve the overall system performance. Considering this situation the proposed method counterpart harmonic mitigation methods with boost capability which are applied to the conventional

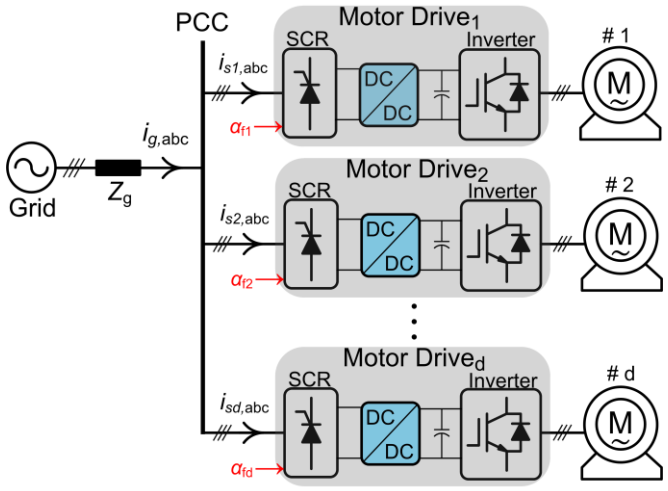

Fig. 1. Schematic of a multi-drive system applying a pulse pattern current modulation strategy at DC link employing a DC-DC converter.

rectifier systems are Δ-rectifier and boost converter operating in Discontinuous Conduction Mode (DCM) [1]. The Δ-rectifier principle is based on phase-modular Power Factor Correction (PFC), meaning that three-phase diode rectifiers with boost converter at their DC-links are applied to each phase. Its advantage is ability to significantly improve the input current quality; however the main drawback of this topology is the presence of high number of power switches, high complexity and lower efficiency comparing with a single-switch boost converter. The DCM single-switch boost converter requires three inductors at the AC-side of the diode rectifier. More importantly this topology suffers from the large EMI (Electromagnetic Interference) filtering effort (i.e., due to the DCM operation) and for effective harmonic mitigation its output voltage should be boosted above 1 kV (i.e., for grid phase voltages of 220 or 230 Vrms) [1].

This paper is structured as follows. Section II describes the proposed harmonic mitigation strategy using a pulse pattern current modulation at the DC-link. A modified version of the predictive valley current control method considering the SCR requirement is introduced in Section III. Section IV is dedicated to the proposed grid synchronization technique by analyzing the DC-link capacitor voltage ripple. In Section V, experimental results are presented to substantiate the effectiveness of the proposed strategy. Finally, conclusions are drawn in Section VI.

II. Proposed Harmonic Mitigation Formulation

A. Multilevel Phase-Shifted Currents

Fig. 2 demonstrates a possible configuration of pulse pattern phased-shifted currents for five parallel-connected motor drive systems. As it can be seen in Fig. 2, a multi-level grid current (i_g) has been constructed based on a proper combination of the controlled rectifier (i.e., SCR) input currents for an improved current quality [25], [26]. Here, following Fig. 1, each current waveform i_{sd} represents the input current of the corresponding

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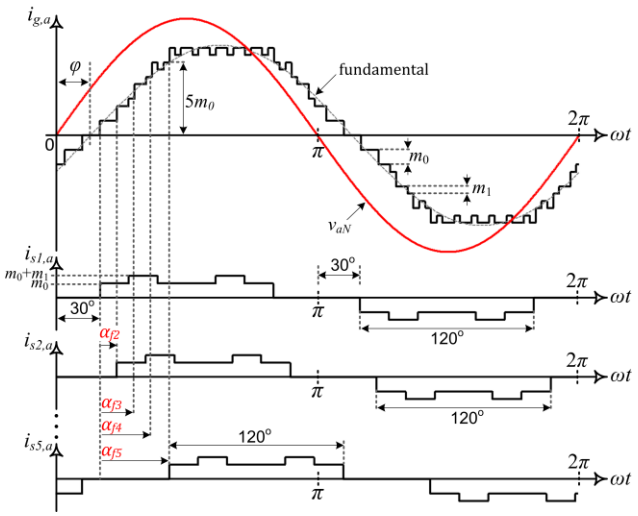

Fig. 2. Typical waveforms of the phase-a currents in a multi-drive system (i.e., d = 5 units) with the proposed harmonic mitigation methodology.

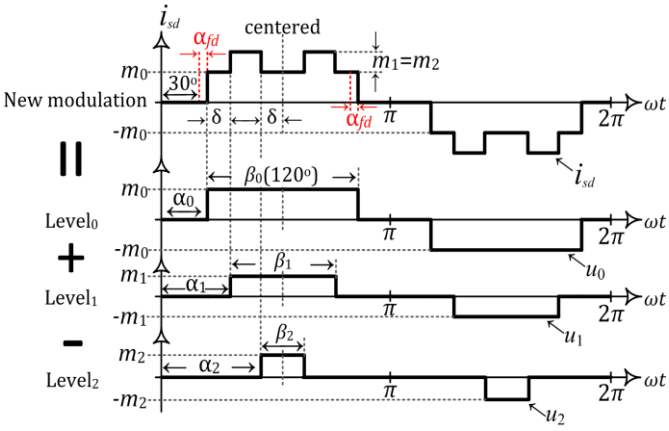

Fig. 3. Conceptual illustrations of the applied modulation (i_{sd} = u_0 + u_1 − u_2) scheme for harmonic elimination (d: number of the parallel-connected drive units).

dth motor drive unit applying different firing angles (α_{fd}) starting with α_{f1} = 0^o at the first unit. Notably, the same pulse pattern is applied to each DC-DC converter (see Fig. 2). However, in reality the pulse pattern switching angles and the firing angle (α_{fd}) of each unit could be different. The situation highly depends on the application requirements, such as:

- Number of the connected motor drive systems (d)
- Input current Total Harmonic Distortion (THD$_i$)
- Input current displacement factor (cos(φ))
- Eliminating specific harmonic order/s
- Load profile of each motor drive unit

Taking into account the above requirements, multitude transcendental equations with unknown variables can be formed, which will result in a set of complicated nonlinear equations. However, the requirement can be easily met by applying an optimization algorithm, which will be addressed in part C of this section.

B. Pulse Pattern Modulation

In order to better understand the essence of the applied harmonic mitigation method, the harmonic distribution of the current modulation method need to be analyzed. The current modulation method is based on the calculation of a pre-programmed switching pattern for the DC-link current to achieve elimination of those specific harmonics in the grid currents [19], [20]. In this approach, a DC-link current modulation scheme i_{sd} is generated by adding or subtracting the phase-displaced current levels. Fig. 3 illustrates the principle of this modulation scheme (i_{sd} = u_0 + u_1 − u_2), where the modulation patterns are synchronized in respect to the grid phase voltage (e.g., v_{aN}) for simplicity.

As it is shown in Fig. 3, the new modulation signal i_{sd} consists of flat signals u_0, u_1, and u_2 with a conduction angle of β_0 (120^o), β_1, and β_2, a phase-shift of α_0, α_1, and α_2 and a magnitude of m_0, m_1, and m_2, correspondingly. Hence, following the Fourier series, the harmonic components of the flat modulation signals (i.e., u_0, u_1, and u_2) can be expressed as,

$$u_i^h(t) = a_i^h \cos(h\omega t) + b_i^h \sin(h\omega t) \tag{1}$$

in which, i = 0, 1, 2, and h = 1, 3, 5, 7, … is the harmonic order, ω the fundamental grid angular frequency, a_i^h and b_i^h are the Fourier coefficients that are given by,

$$\begin{cases} a_i^h = \dfrac{2m_i}{h\pi}\left[-\sin(h\alpha_i) + \sin(\mathrm{h}\,\alpha_i + h\beta_i)\right] \\ b_i^h = \dfrac{2m_i}{h\pi}\left[\cos(h\alpha_i) - \cos(\mathrm{h}\,\alpha_i + h\beta_i)\right] \end{cases} \tag{2}$$

Subsequently, according to the superposition principle and Fig. 3, the harmonic components ($i_{sd}^h(t)$) of the modulation signal (i.e., i_{sd}) can be obtained as,

$$\begin{aligned} i_{sd,a}^h(t) &= (a_0^h + a_1^h - a_2^h)\cos(hwt) + (b_0^h + b_1^h - b_2^h)\sin(hwt) \\ i_{sd,b}^h(t) &= (a_0^h + a_1^h - a_2^h)\cos\left(h\left(\omega t - 120^o\right)\right) \\ &\quad + (b_0^h + b_1^h - b_2^h)\sin\left(h\left(\omega t - 120^o\right)\right) \\ i_{sd,c}^h(t) &= (a_0^h + a_1^h - a_2^h)\cos\left(h\left(\omega t + 120^o\right)\right) \\ &\quad + (b_0^h + b_1^h - b_2^h)\sin\left(h\left(\omega t + 120^o\right)\right) \end{aligned} \tag{3}$$

As a result, the h-order harmonic magnitude (I_{sd}^h) of the resultant DC-link modulation scheme can be expressed as,

$$I_{sd}^h = \left[\left(a_0^h + a_1^h - a_2^h\right)^2 + \left(b_0^h + b_1^h - b_2^h\right)^2\right]^{1/2} \tag{4}$$

Hereafter, it is possible to achieve harmonic cancellation by solving $I_{sd}^h = 0\,(h \neq 1)$ and $I_{sd}^1 = M$ with M being the desired modulation index. However, it should be noted that up to two low-order harmonics (e.g, h = 7 and h = 13) in a single drive system can be cancelled out using the current modulation

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technique, since the following conditions should hold,

$$\begin{cases} \beta_0 = \beta_1 + \beta_2 = 120^o \\ \alpha_1 + \alpha_2 = 2\alpha_0 + 60^o \\ \alpha_0 < \alpha_1 < \alpha_2 < \alpha_0 + 60^o \end{cases} \quad (5)$$

Applying these conditions will guarantee that the input currents in a three-phase system are free of even and tripled-order harmonics. It is worth mentioning that the shortcoming of considering these conditions for the employed current modulation technique is the inability of targeting both 5th and 7th order harmonics for cancellation at the same time. The solution for eliminating the 5th order harmonic ($I_{sd}^5 = 0$) assuming a firing angle α_f = 0 (α_0 = 30°) is achievable when 60°<α_1<90° while applying same situation the solution for eliminating the 7th order harmonic is obtainable when 34°<α_1<60°. This clearly shows that the solution for the 5th and 7th order harmonics does not have any overlap.

Yet, it can be observed in Fig. 2 that applying multiple signals with adjustable firing angles in the new modulation scheme can obtain further reduction of certain harmonics beyond the solely two low-order harmonics (e.g., h = 7 and h = 13). In that case, the resultant total harmonics of the grid current ($i_{g,abc}^h(t)$) for d parallel-connected drives will become,

$$i_{g,abc}^h(t) = \sum_{j=1}^{d} i_{sj,abc}^h(t) \quad (6)$$

C. Optimizing the Modulation

The above analysis illustrates the impact on the input current harmonics by selecting proper modulation parameters (e.g., m_i, α_i and α_{fd}) for the modulation scheme. A suitable solution with high flexibility (i.e., application requirements) can be obtained through an optimization process. The following demonstrates the harmonic optimization solution considering the maximum allowable harmonic level defined by the application or by the grid code. In other words, instead of fully nullifying the distortions, the harmonics could be reduced to acceptable levels by adding suitable constraints (L_h). Then, an optimization problem (Obj_h) that searches a set of α_i, m_i and α_{fd} values over the allowable intervals can be defined as [27],

$$\begin{cases} Obj_1 = M - I_g^1 \le L_1 \\ Obj_h = \dfrac{I_g^h}{I_g^1} \le L_h \\ Obj_{THD_i} = THD_i \le L_{THD_i} \end{cases} \quad (7)$$

Following (7), an objective function F_{obj} has to be formed to minimize the error. The objective function plays an important role in leading the optimization algorithm to a suitable solution set and is calculated as,

$$F_{obj} = \sum \left[w_h . \left(Obj_h - L_h \right)^2 + w_{THD_i} . \left(Obj_{THD_i} - L_{THD_i} \right)^2 \right] \quad (8)$$

implying that, F_{obj} is formed based on a squared error with more flexibility by adding constant weight values (w_h) to each squared error function in order to prioritize different objectives (e.g. THD_i).

Notably, apart from the optimization constraint L_h, the conditions on switching angles (5) has to be included as well in order to ensure a proper rectification operation.

It should be noted that, the performance of harmonic reduction is dependent on the loading conditions (i.e., output power ratio) of drive units. For instance, in the case of two drive units, the maximum harmonic reduction can be attained when both rectifier units draw equal level of current from the grid. The reason behind this issue is the dependency of the SCR unit rectified voltage on the firing angle. Considering the firing angle of the first unit equal to zero α_f = 0 (e.g., using diode rectifier), the average rectified voltage of both units can be given as,

$$V_{rec\_2} = V_{rec\_1} \cos\left(\alpha_f\right) \quad (9)$$

where V_{rec_1} and V_{rec_2} are the average rectified voltages of the first unit (e.g., diode rectifier) and second unit (SCR), respectively. Therefore, as the firing angle increases the average voltage reduces and in return the boost converter draw more current in order to adjust the output voltage at a constant value. Now, ignoring the power losses on the DC-DC converters at the DC-link, following can be obtained:

$$\frac{P_{o2}}{P_{o1}} = \frac{V_{o2} I_{o2}}{V_{o1} I_{o1}} \approx \frac{V_{rec\_2} I_{L2}}{V_{rec\_1} I_{L1}} \quad (10)$$

with P_{o1} and P_{o2} being the output power of the first and second units, and I_{o1} and I_{o2} being the average output current of each rectifier. Substituting (9) in (10) gives the condition which makes both rectifiers draw equal current levels (i.e., $I_{L1} = I_{L2}$)

$$\frac{P_{o2}}{P_{o1}} = \cos\left(\alpha_f\right) \quad (11)$$

Therefore, as long as the above condition holds, the maximum harmonic elimination can be obtained. However, depending on the application each drive unit may run at different power conditions. Generally, the multi-drive applications can be divided into two different types. The First type is the one where the load is shared between multiple drives such as multi-pump applications [16]. In this situation normally the load is equally shared between the drives (i.e., multi-follower control [16]) and therefore the harmonic reduction performance of the system will not be affected significantly. In the second type, the drives operate independently and having different loading conditions at each rectifier units, resulting in unequal input current levels and consequently incomplete cancellation of the harmonics of interest. Therefore, to achieve the maximum harmonic reduction, the loading condition of (11) should be included in the optimization process (7) which leads to different optimized parameters for each operating points and can be applied using a lookup table. Notably, applying different parameters corresponding with their operating points require having a communication between drive units. In Section V, the

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harmonic performance of the system is simulated when drives have different loading conditions.

III. Predictive Current Control

Fig. 4 illustrates the control structure of the implemented setup for multi-parallel connected rectifier systems, where resistive loads have been considered instead of motors as load. In order to control the DC-link current shape and magnitude following the applied modulation scheme a boost converter topology has been selected as the DC-DC converter in Fig. 1. The adopted boost converter can not only perform the desired current modulation scheme, but has also the advantage of boosting the output DC voltage to a suitable level, when it is fed into an inverter. Furthermore, the Proportional Integrator (PI) controller parameters need to be selected in order to have a suitable dynamic response by looking into the boost converter transfer function and the loading conditions. This has been well studied in the literature [28], [29].

The performance of the system in harmonic mitigation can significantly be affected by the current controller tracking capability. Hence, a fast current controller such as hysteresis controller is a good candidate for such applications. However, beyond its simplicity, digital implementation of hysteresis controller requires high sampling frequency [30]. Moreover, it has a variable switching frequency nature. Alternatively, a predictive current control strategy with a fixed switching frequency can be employed. Vast development of predictive current control strategies emphasizes the high performance possibilities of this control technique [23], [24], [30]-[33]. In this paper, a simple predictive valley current control is employed to effectively follow the pre-calculated switching angles for harmonic elimination.

A. Valley Current Control

The predictive valley current control strategy is a well-known control strategy, which has been applied for multitude applications (e.g. power factor correction circuits) [23], [24]. The controller uses trailing edge modulation and it is based on the sampled inductor current, output voltage and input rectified voltage. Following Fig. 4 and assuming that $v_{rec\_d}[n-1] \approx v_{rec\_d}[n]$, finding the sampled inductor current as a function of the previous sampled value can be expressed as [23],

$$i_{Ld}[n+1] = i_{Ld}[n-1] + 2\frac{v_{rec\_d}[n-1]}{L_{dc} f_{sw}} - \frac{v_{od} D'[n]}{L_{dc} f_{sw}} - \frac{v_{od} D'[n+1]}{L_{dc} f_{sw}} \quad (12)$$

denoting n as the sample number, d as the rectifier unit number (drive), $D = 1 - D'$ as the duty cycle, $i_{Ld}[n-1]$ as the sampled inductor current ($i_{Ld}[n]$) and $i_{Ld}[n+1]$ as the current reference ($i^*_{Ld}[n]$), which is equal to the voltage controller output multiplied with the applied modulation signal (u_{msd}). The predicted duty cycle now can be found by rearranging (12) as,

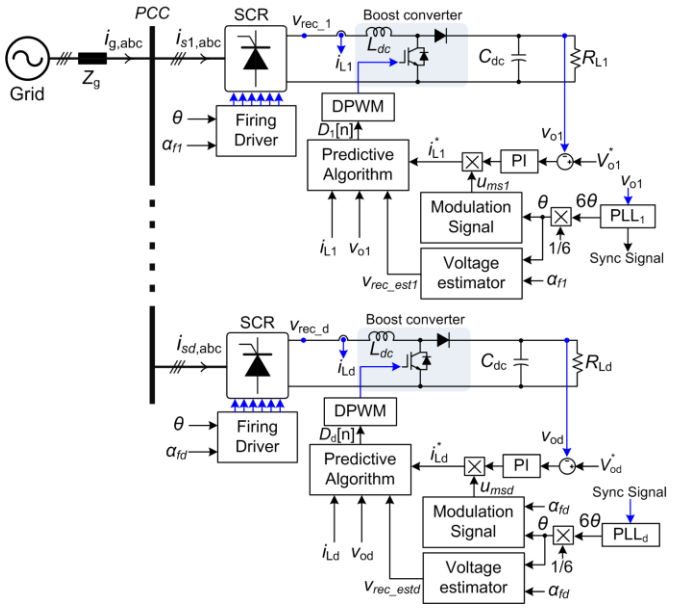

Fig. 4. Block diagram of the overall control structure implemented for the multi-rectifier system using predictive current control.

$$D_d[n+1] = 2 - D_d[n] - \frac{L_{dc} f_{sw}}{v_{od}}\left[i_{Ld}[n] - i^*_{Ld}[n]\right] - 2\frac{v_{rec\_d}[n-1]}{v_{od}} \quad (13)$$

B. Compensation

The calculated control law in (13) has been made on an assumption that the rectified voltage is slowly varying compared to the sampling time so that it can be considered constant between two samples [23], [24]. However, this assumption cannot hold when it comes to the rectified voltage of the SCR unit. Fig. 5 illustrates the rectified voltage of a SCR unit for different values of firing angle (α_f). As it can be seen when $\alpha_f > 0^o$ there is a sudden change in the $v_{rec\_2}[n-1]$ and $v_{rec\_2}[n]$ at the point of commutation. Therefore, applying (13) in this condition will result in an unstable situation, as at the point of commutation the two consecutive rectified voltage samples cannot be considered to be constant. The AC ripple (Δv_{rec_d}) of the rectified voltage which increases correspondingly with the increase of firing angle suddenly appears across the inductor forcing the current to ramp up (i.e., spikes appear) that deteriorates the current. The imposed voltage change can be expressed as,

$$\Delta v_{rec\_d} = \sqrt{6} V_{Ph} \sin(\alpha_{fd}) \quad (14)$$

Fig. 6 exemplifies the inductor current (i_{Ld}) when the firing angle is selected as $\alpha_f = 30^o$, where the commutation happens at the [n-1]th sample. As it can be seen, applying (13) results in an unstable situation (dashed-line). Which is due to inherent two-sample delay presented in the control law (13), and therefore the duty cycle at the [n-1]th sample ($D_d[n]$) will not include the effect of the rectified voltage change for the next two samples. It is at the $D_d[n+2]$ where the increased rectified voltage has been included in the predicted duty cycle, which results in an increase of turn-off time. However, since the imposed change is quite large, the controller cannot maintain

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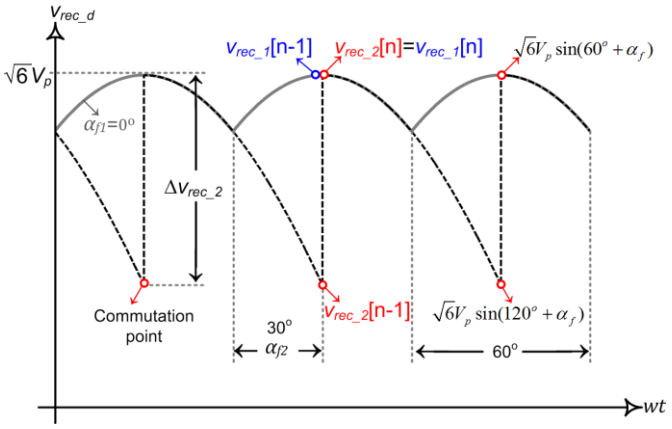

Fig. 5. Rectified voltage (v_{rec_d}) of a SCR unit for two firing angles of 0^o and 30^o degrees.

its performance in the next two samples. Notably, for the smaller firing angles, the inductor current can reach the reference current in a fewer sampling points.

Following the above discussion, the sudden voltage change at the commutation point cannot be treated as a random small perturbation. Therefore, prior-art compensation techniques are not applicable especially for large firing angles. One solution is to apply a variable switching frequency current control method such as hysteresis control. In order to prevent from a variable switching frequency with a high sampling rate, this paper aims at employing a simple modified version of the valley predictive control.

The proposed solution is based on enabling the controller to observe two samples ahead of the rectified voltage. Therefore, by using an estimation of the rectified voltage (v_{rec_estd}) and considering that the two consecutive rectified voltage samples are not equal the control law in (13) can be rewritten as,

$$D_d[n+1] = 2 - D_d[n] - \frac{L_{dc} f_{sw}}{v_{od}}\left[i_{Ld}[n] - i^*_{Ld}[n]\right] - \frac{(v_{rec\_estd}[n] + v_{rec\_estd}[n+1])}{v_{od}} \quad (15)$$

Fig. 6 also illustrates the compensated inductor current (bold line) applying (15). As it can be seen, at the [n-1]th sample the controller is adapted with the voltage change by reducing the turn-on time. The estimated voltage v_{rec_estd} can be made based on the calculated phase angle for the PLL. Employing a PLL is mandatory since the modulated current has to be synchronized with the grid. Therefore the estimated rectified voltage is generated within the controller as,

$$v_{rec\_estd}(t) = \begin{cases} \sqrt{6}V_{Ph}\sin(\theta') & if\ \sin(\theta' - \alpha_{fd}) > 0 \\ \sqrt{6}V_{Ph}\sin(\theta' - 120^o) & if\ \sin(\theta' - 120^o - \alpha_{fd}) > 0 \\ \sqrt{6}V_{Ph}\sin\theta' + 120^o) & if\ \sin(\theta' + 120^o - \alpha_{fd}) > 0 \end{cases} \quad (16)$$

with

$$\theta' = \theta + \Delta\theta + 30^o$$

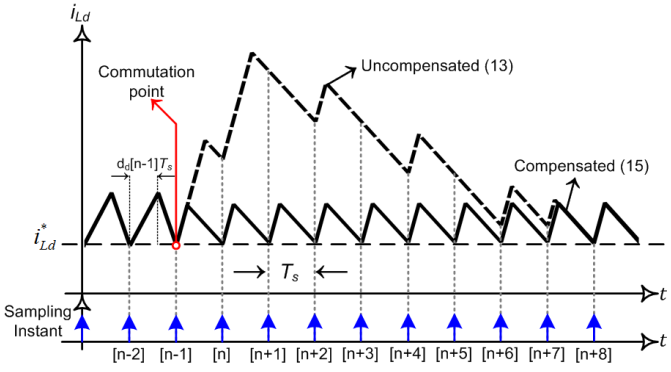

Fig. 6. Inductor current and sampling instant using predictive current control with and without compensation at firing angle 30^o.

where V_{ph} is the Root-Mean-Square (RMS) value of the grid phase voltage, θ is the PLL calculated angular frequency and θ' is the compensated angular frequency. In (16) $\Delta\theta$ is the shifted samples, which is given as,

$$\Delta\theta = \frac{360^o \times f_g}{f_{sw}} n \quad (17)$$

with f_g being the grid frequency, f_{sw} being the sampling frequency (here also switching frequency) and n being the number of the shifting samples.

IV. Grid Synchronization Using Output Voltage Ripple

The modulated current of each unit has to be synchronized with the grid voltage. Generally, the grid synchronization in three-phase systems is performed by employing a PLL system based on the synchronous reference frame [34]-[36]. This requires three voltage sensors to measure three-phase voltages. In this paper, in order to come with a cost-effective system, no additional sensor has been employed for the grid synchronization. The proposed method is based on measuring the output voltage of the DC-DC converter, which as discussed in the previous section has a voltage sensor for the voltage control objective. Hence, in order to illustrate the proposed synchronization concept, the voltage ripple across the DC-link capacitor is firstly analyzed.

A. DC-Link Capacitor Voltage Ripple

Here, the ripple voltage calculation has been conducted based on calculating the input instantaneous power as,

$$p^h_{in}(t) = p^h_a(t) + p^h_b(t) + p^h_c(t)$$
$$\begin{cases} p^h_a(t) = v_{aN}(t) i^h_{s1,a}(t) \\ p^h_b(t) = v_{bN}(t) i^h_{s1,b}(t) \\ p^h_c(t) = v_{cN}(t) i^h_{s1,c}(t) \end{cases} \quad (18)$$

For simplicity, the input power is calculated for the first rectifier unit by setting $\alpha_0 = 30^o$ ($\alpha_f = 0^o$, e.g., diode rectifier). Doing so gives a simplified form of (3) as,

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$$\begin{cases} i_{s1,a}^{h}(t) = c_0^h \sin(h\omega t) \\ i_{s1,b}^{h}(t) = c_0^h \sin\left(h\left(\omega t - 120^o\right)\right) \\ i_{s1,c}^{h}(t) = c_0^h \sin\left(h\left(\omega t + 120^o\right)\right) \end{cases} \quad (19)$$

with i_{s1}^{h} being the modulated input current for the rectifier system, and c_0^h being the Fourier coefficient that can be calculated by,

$$c_0^h = \frac{4}{h\pi}\left[m_0 \cos\left(h30^o\right) + m_1 \cos\left(h\alpha_1\right) - m_1 \cos\left(h\alpha_2\right)\right] \quad (20)$$

The phase voltages with an initial phase of θ_v and V_{ph} as the RMS value of the grid phase voltage are,

$$v_{aN}(t) = \sqrt{2}V_{ph}\sin(\omega t + \theta_v), v_{bN}(t) = \sqrt{2}V_{ph}\sin(\omega t + \theta_v - 120^o)$$
$$v_{cN}(t) = \sqrt{2}V_{ph}\sin(\omega t + \theta_v + 120^o) \quad (21)$$

When using trigonometric identities, the total instantaneous input power ($p_{in}^{h}(t)$) can be given as,

$$p_{in}^{h}(t) = \sqrt{2}V_{Ph}c_0^h\left[\cos\left((h-1)(120^o)\right)\cos\left((h-1)(\omega t + \theta_v)\right) + 0.5\cos\left((h-1)(\omega t + \theta_v)\right) - 0.5\cos\left((h+1)(\omega t + \theta_v)\right) - \cos\left((h+1)(120^o)\right)\cos\left((h+1)(\omega t + \theta_v)\right)\right] \quad (22)$$

Now finding the input instantaneous power for the first five harmonic orders (h = 1, 5, 7, 11, 13) gives,

$$\begin{cases} p_{in}^{1}(t) = \dfrac{3\sqrt{2}}{2}V_{ph}c_0^1 \\ p_{in}^{5}(t) = -\dfrac{3\sqrt{2}}{2}V_{ph}c_0^5\cos\left(6(\omega t + \theta_v)\right) \\ p_{in}^{7}(t) = \dfrac{3\sqrt{2}}{2}V_{ph}c_0^7\cos\left(6(\omega t + \theta_v)\right) \\ p_{in}^{11}(t) = -\dfrac{3\sqrt{2}}{2}V_{ph}c_0^{11}\cos\left(12(\omega t + \theta_v)\right) \\ p_{in}^{13}(t) = \dfrac{3\sqrt{2}}{2}V_{ph}c_0^{13}\cos\left(12(\omega t + \theta_v)\right) \end{cases} \quad (23)$$

Considering the above equations and defining a new harmonic order (k = 6, 12, 18, …) shows that each load current harmonic k produces harmonics k-1 and k+1 on the input current. Therefore, (22) can be rewritten as,

$$p_{in}^{k}(t) = \frac{3\sqrt{6}}{\pi}V_{ph}\left[m_0 + 2c_1^k\frac{\cos\left(k(\omega t + \theta_v)\right)}{k^2 - 1}\right] \quad (24)$$

with c_1^k being the Fourier coefficients that can be calculated as,

$$c_1^k = m_0 + m_1(k+1)\sin(k-1)(60^o - \alpha_1) + m_1(k-1)\sin(k+1)(60^o - \alpha_1) \quad (25)$$

Equation (24) depicts that the input instantaneous power is the sum of an active power plus a pulsating power with the frequency starting from six times of the line frequency.

In order to estimate the output voltage ripple, the instantaneous output power can be calculated as [37],

$$p_o(t) = \left(V_o + v_o\right)I_o + C_{dc}\frac{dv_o}{dt}\left(V_o + v_o\right) \cong V_o I_o + C_{dc}\frac{dv_o}{dt}V_o \quad (26)$$

Notably, the power associated with the ripple voltage and ripple current is neglected. Assuming a lossless system with a high switching frequency, the instantaneous input power is approximately equal to the output power,

$$P_o = V_o I_o = P_{in} = \frac{3\sqrt{6}}{\pi}V_{ph}m_0$$
$$C_{dc}\frac{dv_o}{dt}V_o = 2P_o c_1^k\frac{\cos\left(k(\omega t + \theta_v)\right)}{m_0(k^2 - 1)} \quad (27)$$

Solving the above equation gives the ripple voltage,

$$v_o(t) = \frac{2P_o c_1^k}{k\omega C_{dc}V_o}\frac{\sin\left(k(\omega t + \theta_v)\right)}{m_0(k^2 - 1)} \quad (28)$$

The above equation shows that the fundamental frequency of the output voltage ripple is six times of the line frequency including the initial phase voltage (θ_v). Notably, (28) can be used in sizing the DC-link capacitor considering the desired output ripple voltage.

B. Applying Phase-Locked-Loop (PLL) using the Ripple Voltage

It is known that the output ripple voltage of (28) contains information regarding the line frequency and initial phase. Thus, a PLL using the ripple voltage can extract the information for synchronization. In this paper, since it is assumed that the multi-drive configurations are placed close to each other so only a PLL on the first unit senses the output voltage. Then, it will generate a synchronization signal for the rest of the units.

Fig. 7 shows the structure of the implemented PLL. As it can be seen, the PLL at the first unit is based on a Second Order Generalized Integrator (SOGI) [34]-[36]. The SOGI generates a clean sinusoidal signal with the same frequency and phase of the input voltage. The generated sinusoidal waveform before feeding to the PLL block is changed to a pulse waveform with the amplitude between 0 and 1 using a comparator. The reason behind this is because it can easily be sent to other digital-controlled units for the synchronization. Secondly, the PLL parameters can simply be tuned as the input voltage amplitude is normalized to be 1 [36]. Here, ω_c is the initial angular frequency ($2\pi f_g$) and K_f is the filtering factor. The PI controller of the PLL can be set as a function of the settling time as [36],

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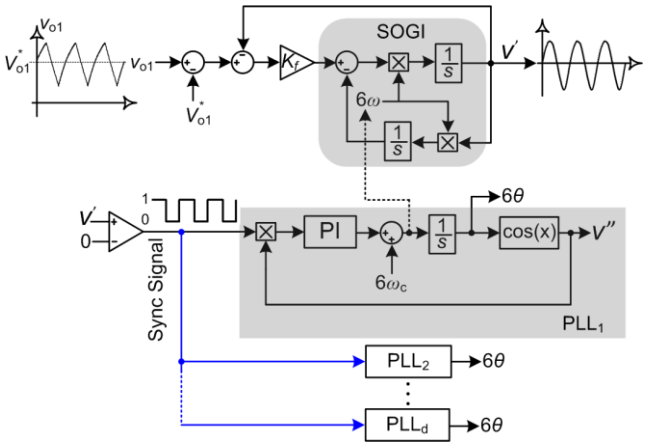

Fig. 7. Structure of the implemented PLL for grid synchronization in the multi-system configuration based on only sensing the output voltage ripple.

$$K_{p_{PLLd}} = \frac{9.2}{t_s}, \qquad K_{i_{PLLd}} = K_{p_{PLLd}} \times \frac{2.3}{t_s \xi^2} \tag{29}$$

where t_s is the settling time and ξ is the damping factor.

V. Results

In order to verify the effectiveness of the proposed harmonic mitigation method along with the applied current modulation scheme, different experiments and simulations have been conducted. As stated before, since the firing angle of the first rectifier unit is always zero $\alpha_f = 0$ ($\alpha_0 = 30^o$), a three-phase diode rectifier which resembles a SCR unit with $\alpha_f = 0$ has been selected. The multi-rectifier system parameters are listed in Table I. The grid impedance has been set using a grid simulator. In practice, to avoid SCR unit failure and reduce the overvoltage to a reasonable limit an RC snubber branch is connected across each thyristor. However, the presence of the snubber circuit causes significant current spikes. In order to damp the current spikes, small AC-side inductors are placed in series prior to the SCR unit. Fig. 8 shows the prototype of the multi-rectifier units following the system structure shown in Fig. 4 with the employed module as summarized in Table II. In order to obtain different objectives a MATLAB function – "fmincon" has been used for optimization of the angles.

Firstly, to better understand the concept of the proposed harmonic mitigation technique, two low-order harmonics of 7th and 11th have been targeted in a rectifier system by setting the corresponding limits in (7) equal to zero. The measured input currents along with the harmonics distribution are shown in Fig. 9. The presence of the grid impedance can be explained as the main reason that the targeted harmonic orders are not fully nullified. As it can be seen, the 7th and 11th harmonics are significantly reduced while in return the 5th harmonic is increased. If the same current shape is applied to another rectifier unit connected in parallel but with a phase shift of $\alpha_f = 36^o$ it will generate the 5th harmonic with 180^o (5x36^o) phase shift in respect to the first unit. Therefore, the first three low order harmonics of 5th, 7th, and 11th will be reduced. Fig. 10 shows the experimental results for two parallel-connected units where the THD_{ig} of the grid current is reduced to 10.5%.

In order to demonstrate the effect of the applied compensation method discussed in Section III.B, the same situation as mentioned above was applied but without any compensation. As it can be seen in Fig. 11, since the predictive controller cannot see the sudden voltage change at the point of commutation, the current has a high rise which deteriorate the current harmonic distribution (THD_{ig} = 35.6%).

Nevertheless, reducing the first three or four low order harmonics is generally demanded, but depending on the application requirement or grid code recommendations, different harmonic distributions would be required. In order to further examine the proposed harmonic mitigation technique, the 5th, 7th, 11th, and 13th order harmonics of the input current

TABLE I
Parameters of the Multi-Rectifier System (Fig. 4)

Symbol	Parameter	Value
$v_{g,abc}$	Grid phase voltage	220 V_{rms}
f_g	Grid frequency	50 Hz
Z_g (L_g, R_g)	Grid impedance	0.1 mH, 0.01 Ω
L_{dc}	DC link inductor	2 mH
C_{dc}	DC link capacitor	470 µF
V_o	Output voltage	700 V_{dc}
K_p, K_i	PI controller (Boost converter)	0.01, 0.1
K_f, t_s, ξ	PLL parameters	0.8, 0.2 s, $\sqrt{2}$
f_{sw}	Switching frequency	25 kHz
P_{o_total}	Total output power	≈5.5 kW

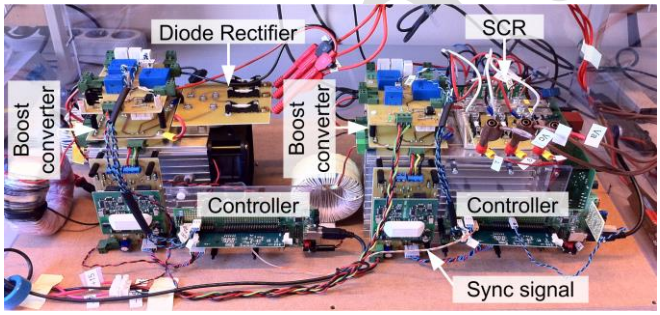

Fig. 8. Photograph of the implemented prototype for two parallel three-phase rectifier units, each equipped with a boost converter at the DC-link side.

TABLE II
Employed Modules in the Implemented Prototype (Fig. 8)

Module	Part-Number	Qty
Three-phase diode rectifier	SKD30	1
Three-phase SCR	SKKT 106/16	3
IGBT-diode	SK60GAL125	2
IGBT gate drive	Skyper 32-pro	2
SCR triggering circuit	RT380T	1
Current measurement	HX-15	2
Voltage measurement	LV25-P	2
SCR snubber branch	R_{snub} = 100 Ω, C_{snub} = 0.1 µF	6
SCR AC-side filter	L_{fscr} = 180 µH	3
Controller	TMS320F28335	2

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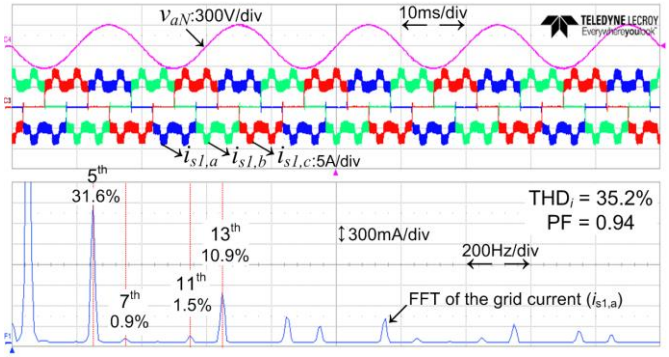

Fig. 9. Experimental results (phase a) of a rectifier unit with the proposed compensated predictive current modulation control at $P_o \approx$ 3 kW, targeting at eliminating 7th and 11th harmonic orders: grid phase voltage v_{aN} [300 V/div], diode rectifier input currents $i_{s1,abc}$ [5A/div] and Fast Fourier Transform (FFT) analysis of the diode rectifier input current $i_{s1,a}$ [300 mA/div].

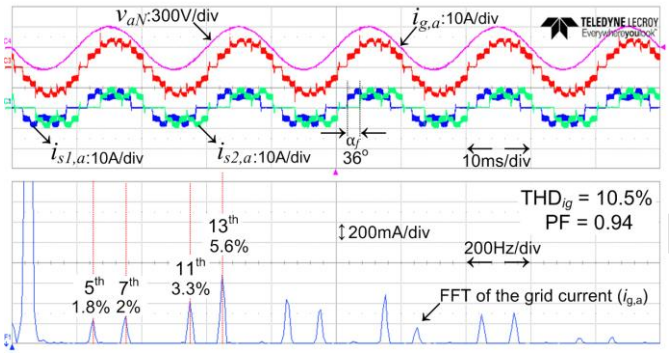

Fig. 10. Experimental results (phase a) of the multi-rectifier system with the proposed compensated predictive current modulation control **targeting at minimizing 5th, 7th and 11th harmonic orders**: grid current $i_{g,a}$ [10 A/div], grid phase voltage v_{aN} [200 V/div], diode rectifier input current $i_{s1,a}$ [10A/div], SCR unit input current i_{s2a} [10 A/div], and Fast Fourier Transform (FFT) analysis of the grid current [200 mA/div].

(i_g) have been targeted to be less than 5% using the optimization given in (7) and (8). As Fig. 12(a) illustrates, although the first four low order harmonics are controlled to be below 5%, the overall THD$_{ig}$ = 11% has been slightly increased in comparison with Fig. 10. Moreover, Fig. 12(b) shows the measured rectified and output voltages of both units. Notably, the amplitude of the output voltage ripple can be adjusted according to (29).

Figs. 10 and 12(a) illustrate the possibility to improve the grid current quality for different objectives. However, selecting the firing angle of above 30° will result in having a Power Factor (PF) of less than 0.95. In order to further demonstrate the flexibility of the proposed approach, another test has been carried out where PF in addition to THD$_{ig}$ has been included in the optimization process. Fig. 13 presents the results, which show that increasing the PF has adversely affected the THD$_{ig}$. Although, a trade-off among different demands is inevitable, this effect can be reduced by increasing the number of connected drive units. However, this is out of the scope of this paper.

In general, the experimental results have illustrated that with

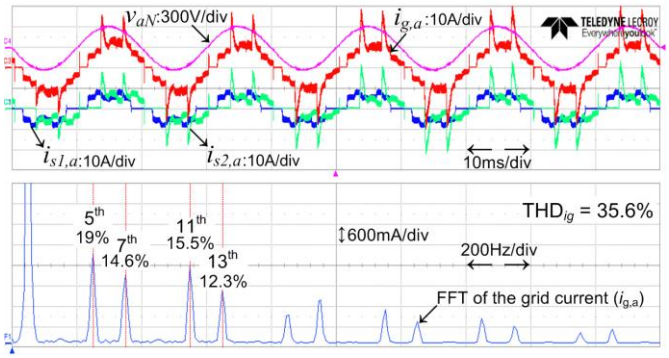

Fig. 11. Experimental results **without including the compensation** in the predictive controller for the case targeting at minimizing 5th, 7th and 11th harmonic orders: grid current i_g [10 A/div], grid phase voltage v_{aN} [300 V/div], diode rectifier input current $i_{s1,a}$ [10 A/div], SCR unit input current $i_{s2,a}$ [5 A/div], and Fast Fourier Transform (FFT) analysis of the grid current [600 mA/div].

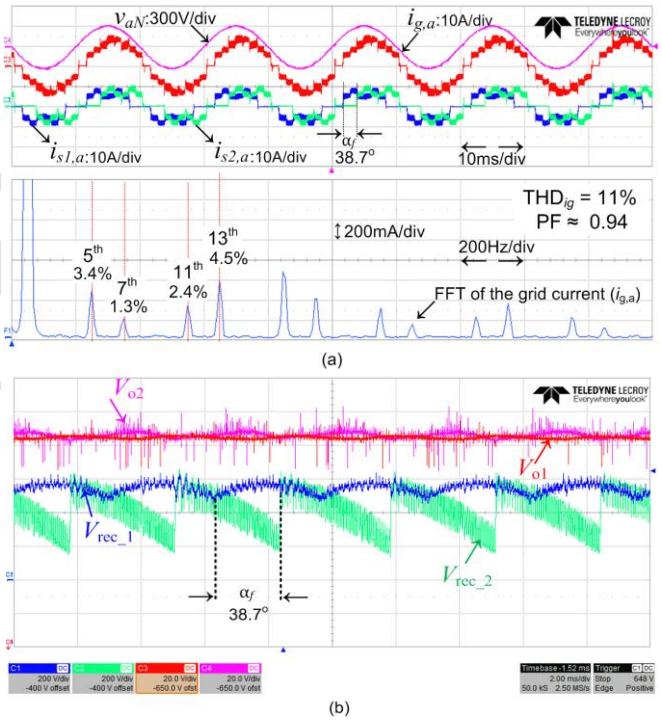

Fig. 12. Experimental results of the multi-drive system with the proposed compensated predictive current modulation control **targeting at minimizing 5th, 7th, 11th and 13th harmonic orders**: (a) grid current i_g [10 A/div], grid phase voltage v_{aN} [200 V/div], diode rectifier input current i_{sa1} [10 A/div], SCR unit input current i_{sa2} [10 A/div], and Fast Fourier Transform (FFT) analysis of the grid current [200 mA/div] and (b) rectified and output voltages of both units.

the compensation method, the controller can maintain its performance even when the firing angle increases. The results have shown that the inductor current ramps down for a small portion of the time. In fact, the predictive controller observes more than two samples ahead of the input voltage, and therefore it starts to increase the turn-off time slightly sooner that it should be. This is due to the presence of small errors always appearing as a result of discretization. Increasing the sampling frequency can resolve this issue as it increases the estimated voltage resolution. Nevertheless, the measured

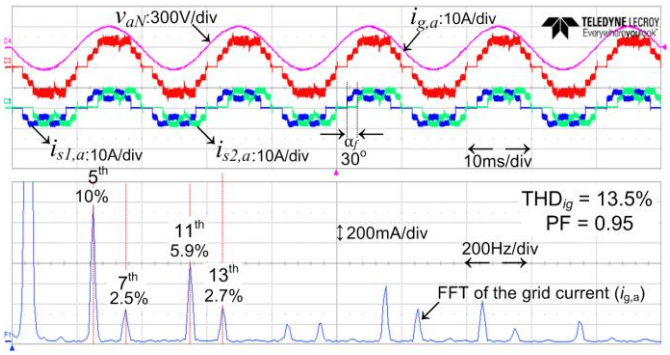

Fig. 13. Experimental results (phase a) of the multi-drive system with the proposed compensated predictive current modulation control **targeting at a minimized THD$_{ig}$ and improved PF**: grid current i_g [10 A/div], grid phase voltage v_{aN} [200 V/div], diode rectifier input current i_{sa1} [10 A/div], SCR unit input current i_{sa2} [10 A/div], and Fast Fourier Transform (FFT) analysis of the grid current [200 mA/div].

TABLE III
HARMONIC DISTRIBUTION OF DIFFERENT PRACTICAL EXPERIMENTS WITH CORRESPONDING CURRENT MODULATION PARAMETERS

Mitigation Objective	Harmonic Distribution and THD$_{ig}$ (%)					Selected Parameters
	$\frac{I_g^5}{I_g^1}$	$\frac{I_g^7}{I_g^1}$	$\frac{I_g^{11}}{I_g^1}$	$\frac{I_g^{13}}{I_g^1}$	THD	$[m_1, m_2]$ $[\alpha_1, \alpha_f]^o$
5th, 7th, and 11th harmonics (Fig. 10)	1.8	2	3.3	5.6	10.5	[1, 0.532] [50, 36]^o
5th, 7th, and 11th harmonics without compensation (Fig. 11)	19	14.6	15.5	12.3	35.6	[1, 0.532] [50, 36]^o
5th, 7th, 11th, and 13th harmonics (Fig. 12(a))	3.4	1.3	2.4	4.5	11	[1, 0.49] [50, 38.7]^o
Improving PF with minimum THD$_{ig}$ (Fig. 13)	10	2.5	5.9	2.7	13.5	[1, 0.637] [45, 30]^o

harmonic distribution have depicted that with the proposed compensation method, the desirable objectives can be achieved. Table III further summarizes the detailed harmonic contents of the conducted test results along with their corresponding phase-shift angle and pre-calculated parameters for the applied current modulation at the DC-link.

Finally, as it is mentioned in Section II, the loading condition of drive units can affect the harmonic performance of the system. Here, the second case of harmonic reduction (Fig. 12(a)) is considered. Assuming that the each drive unit can be operated from 50% up to 100% of its rated power, the power ratio between the rectifier units P_{o1}/P_{o2} can change in the range of 0.5 to 2. Fig. 14 illustrates the obtained simulation results. As it can be seen, two different situations are considered. First, the optimized parameters are applied under ideal condition (both units draw equal level of currents) as in Table III. Secondly, the parameters are optimized regarding to each operating point (i.e., power ratio). As it can be seen from Fig. 14, the maximum THD$_{ig}$ of 18.25% is obtained when the phase-shifted unit (second unit) is operating at higher power

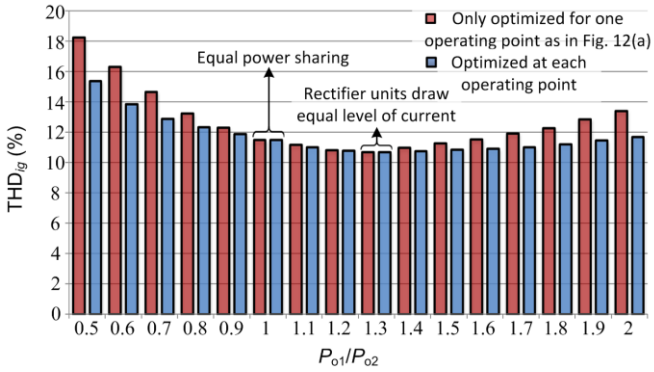

Fig. 14. Simulated results of performance comparison of the two drive system at different loading conditions.

level and the minimum THD$_{ig}$ is obtained when both units draw equal current level from the grid ($P_{o1}/P_{o2} \approx 1.3$). Notably, the output power increase of the first unit does not significantly affect the THD$_{ig}$. Moreover, for applications where the load is equally shared between units ($P_{o1}/P_{o2} = 1$) THD$_{ig}$ is slightly changed (0.6%). Finally, the effect of applying optimized parameters at each operating point (i.e., including (11) in the optimization process) is illustrated as well. For instance, applying optimization for each operating point can effectively improve the THD$_{ig}$ of 18.25% (when $P_{o1}/P_{o2} = 0.5$) down to 15.4%. Therefore, for the applications where the power is not equally shared among the drives pre-programmed optimized parameters can be included as a lookup table and applied to each drive unit. Notably, for this case having a communication between drives is mandatory.

VI. CONCLUSION

This paper has proposed a new harmonic mitigation methodology suitable for multi- drive systems. It has been shown that by phase-shifting rectifiers input currents along with a pulse pattern current modulation scheme at the DC-link can improve the input current quality significantly. A modified predictive current controller in tracking pre-estimated switching angles have been carried out in this paper. In addition, a cost-effective system is implemented, which avoids sensing the input voltage and line voltage for the predictive controller and the PLL, respectively. The experimental results have verified that the proposed method can effectively reduce low order harmonics. Moreover, the flexibility of the proposed concept can be extended by increasing the number of connected units and modulating the DC-link current with a higher number of levels.

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