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Optimal Interleaving Angle Determination in Multi Paralleled Converters Considering the DC Current Ripple and Grid Current THD

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***Abstract* — A typical application for parallel connected converters is in multi megawatt wind turbine systems. Manipulating the interleaving angle between the Pulse Width Modulated (PWM) carrier waves of each converter can result in reduced grid and DC link current ripple, thus the passive components from the DC link and grid filter can be minimized. In previous studies the optimization of the interleaving angle for either the grid current Total Harmonic Distortion (THD) or the DC link current ripple has been made. In this study a compromise is made in order to maintain a THD of the grid current in a level that complies with the standards, while in the DC link the current ripple is reduced. The dependency of the grid current THD and the DC link current ripple on the interleaving angle were determined by simulations. The results were also validated on a hardware setup.**

Keywords—parallel converters, optimal interleaving angle, renewable energy

I. INTRODUCTION

The penetration of the renewable energy in the electrical energy generation has seen a huge increase in the last decade. Wind turbines have the highest installed capacity within the last years. In order to meet the ever increasing grid standards, these wind turbines use full converters to process the power which is injected into the grid [1]. The use of Voltage Source Converters (VSC) is an accepted method to process the injected power into the grid. Moreover, the switching frequency of these converters is also limited, due to the high power [2].

The generators used in these systems are typically low voltage generators (690 V). To be able to achieve MW range powers, these converter modules are often paralleled [3],[4]. Besides sharing the load, the parallel converters have also other advantages[5]. First of all, due to the modular design, it is easy to modify the power rating of a converter by inserting or removing converter modules. Moreover, this topology allows a flexible number of converters; therefore the reliability of the whole converter system is increased. In case of failure of a converter module this can be easily disconnected and the other converters can remain in operation, but reducing the overall power rating [6]. Another advantage is that when the produced instantaneous power is below a certain level, not all converters need to be connected; therefore the lifetime of the whole system can be increased and the losses may be reduced [7]. Besides its advantages the paralleled converters also have their disadvantages, such as: due to the increased number of converters the overall system cost is higher compared to the case of a single converters. There is a requirement that all the carriers of the converter have to be synchronized, otherwise, circulating currents can appear between the modules, which lead to increase in the semiconductor losses and can saturate the filter inductors.

Previous studies showed that the grid codes can be met, even with reduced impedance of the output filter, by optimizing the interleaving angle between the Pulse Width Modulated (PWM) carrier waves [5]. The interleaving angle refers to the phase shift between the carriers of each converter module. When carrier interleaving is applied to a parallel converter system, it affects both the AC and DC side of the converter [8],[9].

Furthermore, if carrier interleaving is used, a high frequency circulating current will appear between the modules of the converters. The circulating current occurs because of the opposite zero vector generation, caused by the modulation and the interleaving. To suppress this high frequency circulating current an additional Common Mode (CM) impedance is required[5].

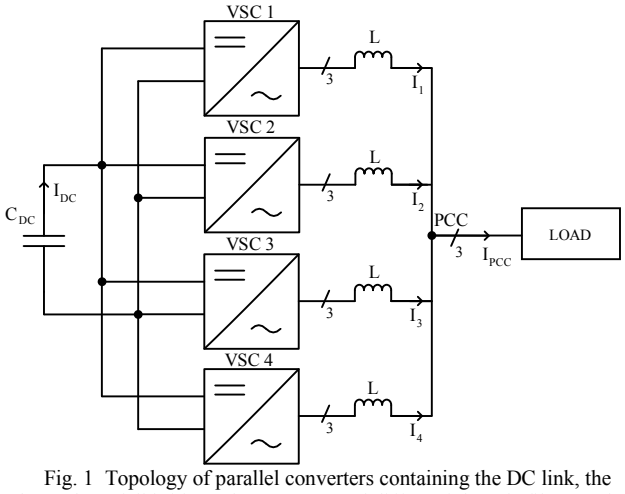

Fig. 1 Topology of parallel converters containing the DC link, the three-phase full bridges, the common and differential mode filters and the connection to the grid.

The wind turbine converter has two converters connected in a back-to-back configuration. One side of the converter is connected to the grid, another side is connected to the generator. Typically, to be able to push energy to the grid, the DC link voltage level is kept

constant. The grid side converter is operated with a modulation index of around 1. On the other hand, the modulation index of the generator side converter depends on the power coming from the wind, thus having a huge fluctuation.

The topology of *4* parallel connected converters is depicted by Fig. 1. In this topology the VSCs are sharing the same DC link. For filtering purposes at the output of each converter a single phase inductor is connected. The single phase inductor offers both differential and common mode filtering. The differential mode filter is used to reduce the harmonic components of the differential mode current caused by the modulation, while the common mode filter is used to suppress the circulating current between the modules, which appears due to interleaving [10].

Several other methods exist for suppressing the circulating current. The first method is to use a three phase differential mode inductor and a three phase common mode inductor at the output of each converter [5] [11]. Another method is to use coupled inductors (CI) between the corresponding phases of every converter [ref]. However, by using the CI the modularity of the system is compromised, since the CI is only effective if both of the converters are operated with the same power. In the case of the CM the modularity can be maintained because the filtering does not depend on the other converter. In this article, since the modularity is a driving factor the solution with the CM is used.

In this paper the authors, investigate the effect of the modulation index and the interleaving angle on the total current Total Harmonic Distortion (THD) and on the Root Mean Square (RMS) value of the DC link current. Moreover, a graphical explanation is presented for different interleaving angles, which will explain the findings of the study.

A simulation model has been created for a converter system with 4 modules in parallel. To validate the simulation results, an experimental setup has been implemented, having the same parameters as the simulation one.

II. Interleaved Modulation of the Parallel Converters

A. System Description

For the simulation study a 6.9kVA converter with 4 parallel modules sharing the same DC link was considered (Fig. 1). To avoid additional harmonics the DC power was supplied by a DC power source. Three single phase inductors (L) have been used as an output filter for each of the converter modules. The use of single phase inductors is justified, because it offers both common mode and differential mode filtering. As mentioned previously, the common mode inductance is required to limit the circulating current, while the differential mode inductance is used for shaping the current flowing out from the converter. The value of the inductors was considered to be 7.1%. The value can be calculated as follows:

$$L = \frac{V_{ph} \bullet \frac{7.1}{100}}{I_{ph} \bullet 2\pi \bullet f_{fund}} [H] \quad (1)$$

where, V_{ph} is the RMS value of the phase voltage and I_{ph} is the RMS value of the individual converters' phase current, f_{fund} is the fundamental frequency, in this case 50 Hz. The inductance value is specified in percentage, in this way the analysis can be applied for different power levels by using the same inductance value in percentage.

In the study the authors would like to evaluate the effect of the interleaving for the full modulation range, thus the converters are connected to a load resistor. Another method would be to connect the converter to the grid, but if the modulation index has to be varied from 0.1 to 1.15 then the DC link voltage has to be changed. For very small modulation indices it may happen that the DC link voltage would be too high and it would not be a feasible solution.

B. Carrier interleaving

The interleaving angle (θ) refers to the shift between the carriers and its maximum can be calculated as:

$$\theta = \frac{2\pi}{n} [rad] \quad (2)$$

where, n refers to the number of paralleled converters.

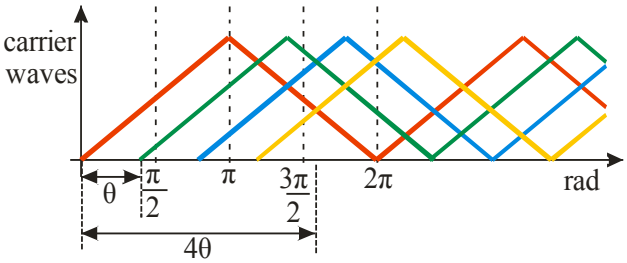

Fig. 2 Interleaved carriers for 4 converters

Fig. 2 shows the phase shifted PWM carriers for the case of 4 converters.

When the carrier of each converter is in phase the harmonics caused by the modulation are also going to be in phase, thus at the PCC the amplitude of these harmonics will be n times larger.

The interleaving of the carrier signals helps to eliminate certain harmonics from the resultant current. This depends on the number of modules and on the interleaving angle [12]. On the other hand, due to interleaving the current drawn from the DC link will occur at different time intervals. Because the stress on the DC link capacitor is dependent on the current drawn from it, using interleaving this stress can be reduced.

C. Modulation of the interleaved parallel converter

There are different modulation strategies used in parallel converters such as Space Vector Modulation (SVM), Sine PWM, and several Discontinuous PWM methods (DPWM) [8, 10],[13, 14]. In this study for modulation the SVM technique will be used.

By using SVM 6 active (v_{100} –v_{101}) and 2 zero vectors (v_{00}, v_{111}) can be generated. During one modulation period any arbitrary voltage vector can be generated by the sum

of two active and two zero vectors. In Fig. 3(a) φ denotes the angle between the generated voltage vector (V) and the α axis, while d_1 and d_2 are the duty cycles. For the specific case illustrated by Fig. 3 (b) V will be generated by applying v_{100} and v_{110} for the times specified by d_1 and d_2.

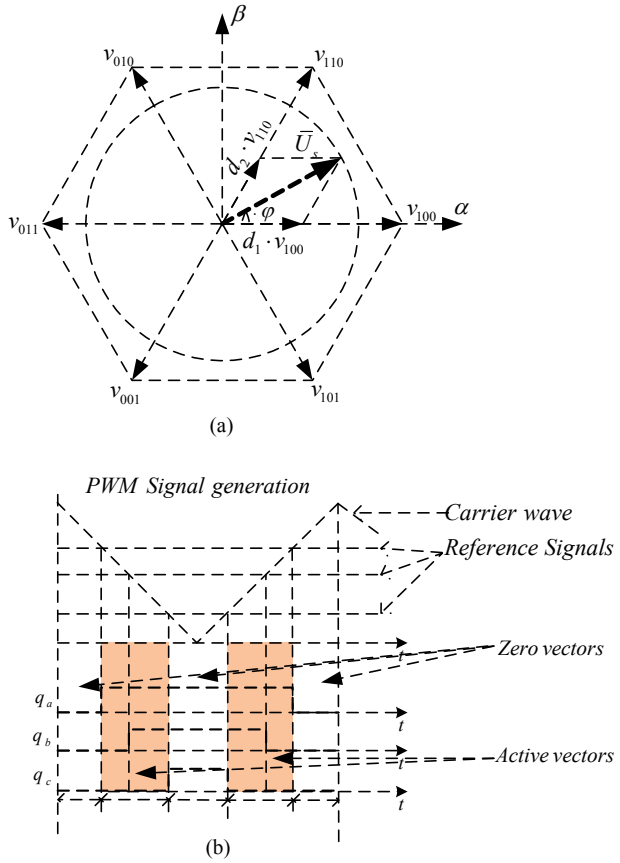

Fig. 3 Example of generation of a space vector

One can observe that the generation of these active vectors is done in the following order: zero vector, active vector 1, active vector 2, zero vector, active vector 2, active vector 1 and zero vector. The ripple current is a consequence of this switching sequence.

When no carrier interleaving is used, the same voltage vectors are applied to all converter at any given time. On the other hand, when carrier interleaving is applied, the generated voltage vectors will be shifted compared to the other converters. In other words, if the carriers of two converters are phase shifted by 180º, the applied voltage vectors will be in opposition. This means that i.e. the top switch of the first converter could be connected to the positive DC bus, and the bottom switch of the same phase could be connected to the negative DC bus. Doing so, the positive and negative terminals of the DC link will be short circuited through the single phase inductors, thus a circulating current appears between the modules. The frequency of this circulating current is equal to the switching frequency.

III. Optimal Interleaving Angle Determination

Using PLECS and MATLAB-SIMULINK a series of simulations have been carried out. The modulation index and the interleaving angle has been swapped and the total current THD (I_{PCC}) and the RMS value of the DC link capacitor current (I_{DC}) have been observed. For a fair comparison the output current was maintained constant for all the modulation indices. This is required in order to ensure that the filter (L) offers the same filtering for all the cases. To ensure the constant output current, the load resistance was changed for every modulation index. The value of the load resistance can be calculated as follows:

$$R_{Load} = \frac{mV_{dc}}{2I_{\mathrm{PCC},p}} \tag{3}$$

where, R_{load} is the load resistance, V_{dc} is the DC link voltage and $I_{PCC,p}$ is the peak value of the total current and m is the modulation index.

The interleaving angle has been swept from 0 to 90º. This range was selected due to the fact that in the range of 90º to 180º the results are in reflection symmetry, while in the case of the modulation index a sweep between 0.1 and 1.15 has been made with steps of 0.05.

A. DC link ripple Current RMS

The variation of the RMS value of the DC link current ripple, in function of modulation index and interleaving angle, is depicted by Fig. 4. It can be observed that the RMS value changes in function of the modulation index and interleaving angle. Even though the I_{PCC} current is considered to be more or less constant, the reason why the RMS value of the DC link current is changing is because the output voltage of the converter is dependent on the modulation index hence, the delivered is constant for all the modulation indices.

As mentioned previously, the circulating current appears due to the opposite zero vector generation during modulation. This phenomena is explained in details in the following sections.

For a better understanding Fig. 6(bottom) depicts the minimum of the RMS value of the DC link current for a modulation index of 1.

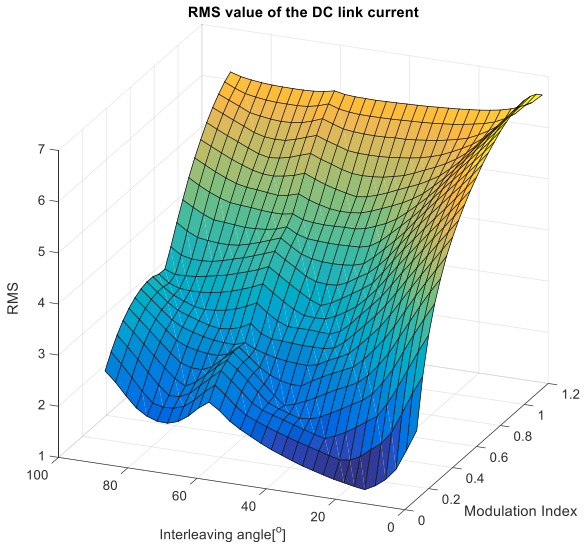

Fig. 4 RMS value of the DC link current in function of Modulation index and interleaving angle

It can be observed that the voltage ripple has its minimum around the interleaving angle of 45°.

B. Total Current THD

In the case of total current THD, just like for the previous case, the value depends both on the interleaving angle and on the modulation index. However, in this case the effect of the interleaving angle is more predominant. It has to be noted that the total current THD has multiple local minimum points.

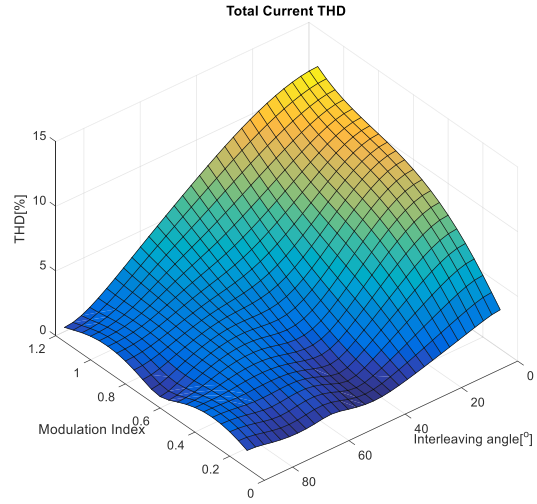

Fig. 5 Total current THD variation based on the Modulation Index and on the Interleaving Angle

From, Fig. 5 it can be seen that the THD is decreasing with the increase of the interleaving angle. For better visualization Fig. 6 (top) shows the minimum value of the THD for a modulation index of 1.

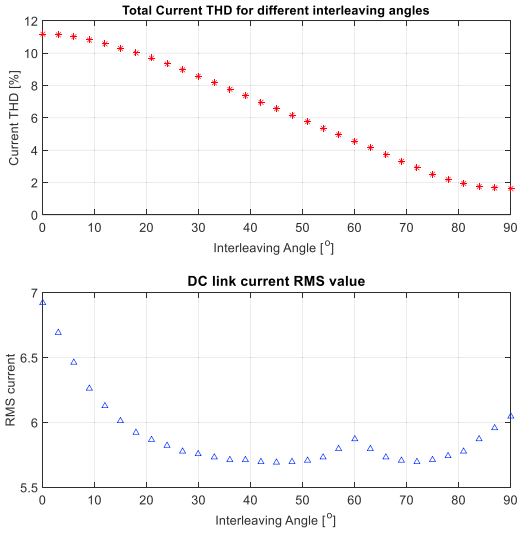

Fig. 6 Top figure: Variation of the total current THD with the interleaving angle for M=1; Bottom figure: Variation of the RMS value of the DC link current with the interleaving angle for M=1

When looking at the total current THD it is essential to have a harmonic content that satisfies the EN60001-3-12 standard, which states that the total current THD has to be below 5%, for a renewable application. On the other hand, from the DC link capacitor point of view it is essential to maintain the voltage ripple at a minimum. Decreasing the stress on the DC link capacitor can result in reduced DC link capacitor value. Moreover, the lifetime of the capacitors can be increased, and hence the reliability of the system can be improved.

For grid connected applications the modulation index is usually kept around 1. For this situation, based on the above simulations, the following conclusions can be drawn:

- The grid side current THD has its minimum at an interleaving angle of 90°
- The RMS value for the DC-link capacitor voltage ripple has the minimum value at an interleaving angle of 45°.

From the overall system point of view the optimal interleaving should be between 45° and 90°. When selecting the optimal interleaving angle the most important driving factor is that the produced current has to satisfy the standard. In this case it is essential that the THD value of the total current is below 5%. On the other hand, from capacitor point of view there are no such restrictions. Here the driving factor can be the lifetime of the capacitor.

For a grid connected application where M is usually 1, in this case according to Fig. 6, the optimal interleaving angle would be between 70° and 90°.

Based on the simulation results it was concluded that the optimal interleaving angle is different for the total current THD and for the RMS value of DC link capacitor current. In the next section this phenomenon explained.

IV. Voltage Vector Generation for Different Interleaving Angles

Fig. 7 and Fig. 8 depict the switching instant where different voltage vectors are generated for 4 converters in parallel with an interleaving angle of 45°, and 90°, respectively. For both of the cases the desired voltage vector is V (Fig. 3). This voltage vector will be generated by applying the active vectors V_1 (d_1*v_{100}) and V_2 (d_2*v_{110}) for the same amount of time. It has to be noted that V is considered for the ideal case when φ=30°.

When the interleaving angle is 90° the carriers of converter one and converter three are interleaved by 180°, so when converter one is generating V_1, converter three will generate V_2. The same is true for converter two and four. This means that the resultant voltage vector, seen at the PCC, will be V; hence the produced current ripple will be minimal. On the other hand, if the φ≠30° the generated voltage vector will not be V hence an increase in the error voltage vector will happen, depending on how far the generated voltage vector from φ=30° is.

In the other case when the interleaving angle is not 90°, the carriers of the individual converters will not be in opposite symmetry. Consequently the magnitude of the error voltage vector will increase.

The error voltage vector can be observed in Fig. 7(c) for an interleaving angle of 45°, while Fig. 8(c) shows it for an interleaving angle of 90°. For both cases the average value of the error voltage vector is 0. However, for the case with

an interleaving angle of 45º the ripple in error voltage vector is not 0 as it is in the case for interleaving angle of 90º.

At the plot of Fig. 7 (d) and Fig. 8 (d), the energy taken from the DC link is shown for an interleaving angle of 45º and 90º, respectively. The average value of the energy taken from the DC link is the same for both of the interleaving angles. On the other hand, there is a difference between the two currents drawn from the DC link. It can be observed that with an interleaving angle of 45º between the carrier waves of the converters, the deviation from the mean value in the energy amplitude is half as big as with the interleaving angle of 90º. This results in a smoother current in the DC link, thus having smaller ripple which makes it possible to use a smaller DC link capacitor.

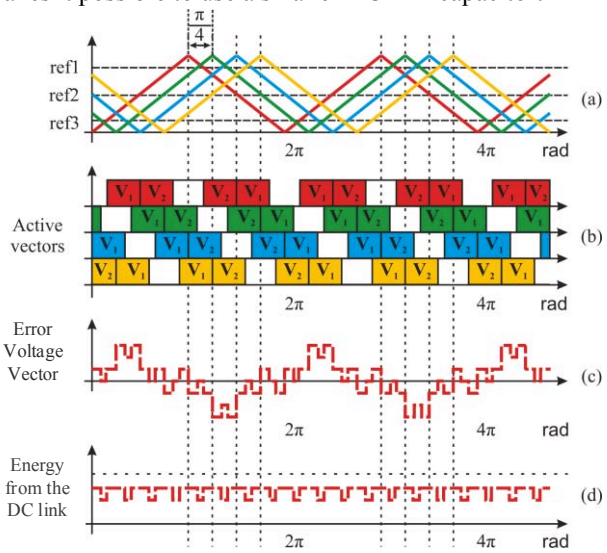

Fig. 7 Voltage vectors and error voltage vector for an interleaving angle of π/4 rad; (a) 4 carrier signals shifted by π/4; (b) the duration of the active voltage vectors; (c) error voltage vector; (d) Energy taken from the DC link .

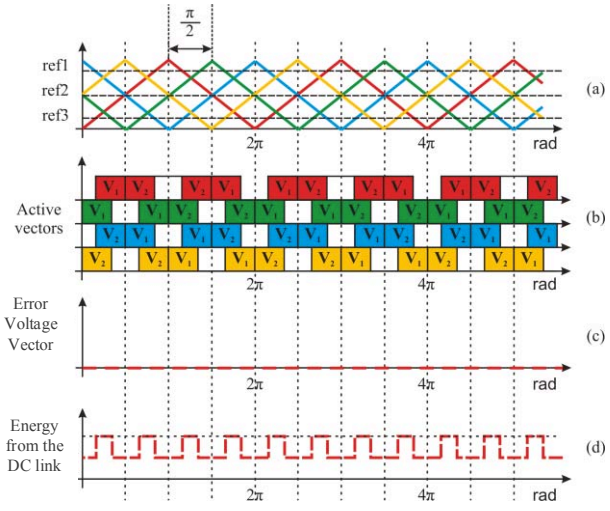

Fig. 8 Voltage vectors and error voltage vector for an interleaving angle of π/2 rad; (a) 4 carrier signals shifted with π/2; (b) the duration of the active voltage vectors; (c) error voltage vector; (d) Energy taken from the DC link .

V. Experimental Validation

In Fig. 9 a picture of the experimental setup, the topology presented in Fig. 1, is shown. The power rating of the system is 10kW, with a DC link voltage of 650V connected to a 3 phase resistive load; each converter had a switching frequency of 2.5 kHz. To control the setup control a Texas Instruments TMS320F28346 processor was used.

Table I

Experimental Parameters

Symbol	Value
V_{DC}	650 [V]
L	20.9 [mH]
f_{sw}	2500 [Hz]
I_{PCC}	10 [A_{RMS}]

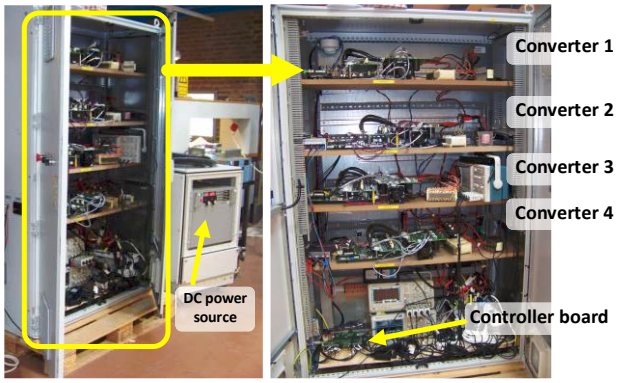

Fig. 9 Picture of the small scale hardware setup

The experimental results from Fig. 11 have been obtained by connecting the PCC to a resistive load. The experiment has been carried out under the same conditions as the simulation. The modulation index was changed between 0.1 and 1.15 with steps of 0.1, and the last measurement with a step of 0.05. The following interleaving angles have been considered: 0º, 15º, 30º, 45º, 60º, 75º and 90º.

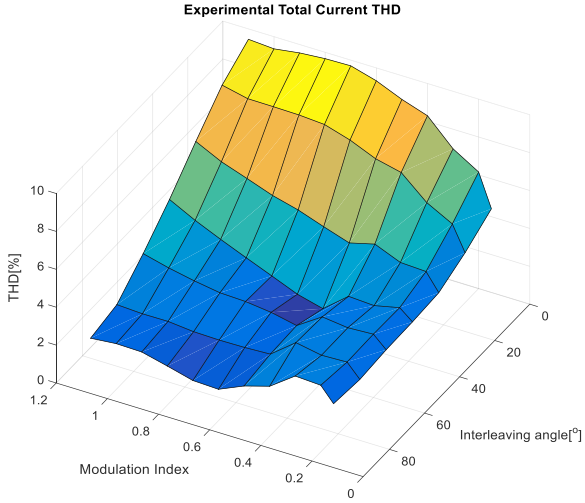

Fig. 10 Experimental results for the variation of the total current THD with the modulation index and interleaving angle for 4 converters in parallel

On Fig. 10 the total current THD is represented in function of the modulation index and the interleaving angle. One can observe that the measurement results are similar to simulation results (Fig. 5).

As for the RMS value of the capacitor current, the measurements could not be carried out, since in the physical system, the DC link capacitor is distributed and it is not a single one. Moreover, due to space constraint current probes cannot be hooked up to the pins of the DC link capacitor to measure the current.

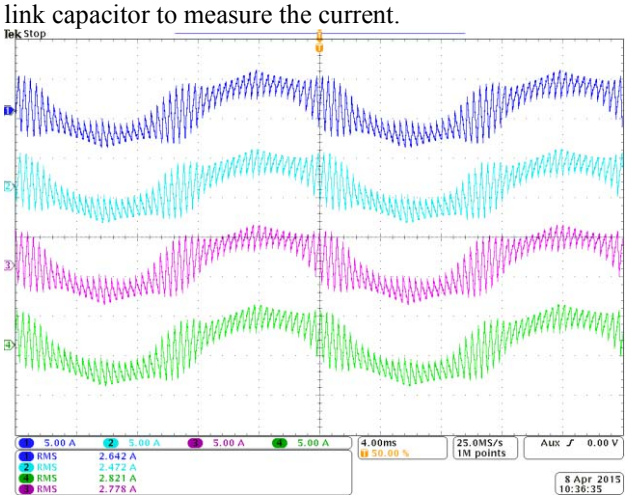

Fig. 11 Measured phase *A* current of four converters in parallel with an interleaving angle of 90º (Blue- Converter 1; Cyan- Converter 2; Magenta- Converter 3; Green- Converter 4)

The individual converter currents for one of the phases with a carrier interleaving of 90º is shown in Fig. 11, while the total current is shown in Fig. 12. As a comparison, the case when no interleaving angle and when 45º presented. Fig. 13 depicts the individual current waveforms for non-interleaving case and Fig. 15 for the interleaving angle of 45º. Total current is shown on Fig. 14 for the non-interleaved case, while Fig. 16 plots for the 45º case. In all of the cases the modulation index was set to be 1. Although, the RMS value of the total current for all of the cases is identical, the ripple content differs. When comparing the THD value the same trend can be observed as in the simulation. The THD of the total current is decreasing when the interleaving angle is closer to 90º. As for the individual currents the amplitude of the switching harmonics is much larger in the case of an interleaving angle of 90º compared to the non-interleaved case. When the interleaving angle of 45º has been used, the magnitude of the ripple in the individual currents and in the total current is between the non-interleaved and the 90º interleaved case. The reason is that in the non-interleaved case there is no circulating current in the system, while in in the 90º case it is maximum. The individual switching harmonics are added in the total current. When no interleaving was applied to the carriers, the ripple in the total current is 4 times the ripple of one converter, while in the 45º case only some of the harmonics are cancelled the rest is visible in the total current.

On the other hand, since due to the carrier interleaving the harmonics in the interleaved case are opposite to each other, and their effect is cancelled in the total current.

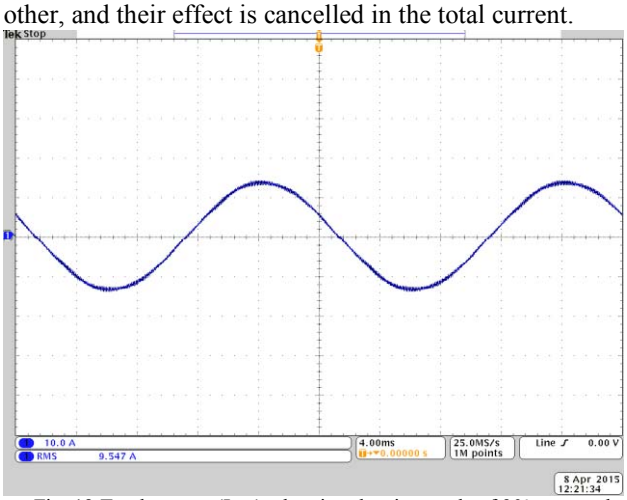

Fig. 12 Total current (I_{PCC}) when interleaving angle of 90º was used.

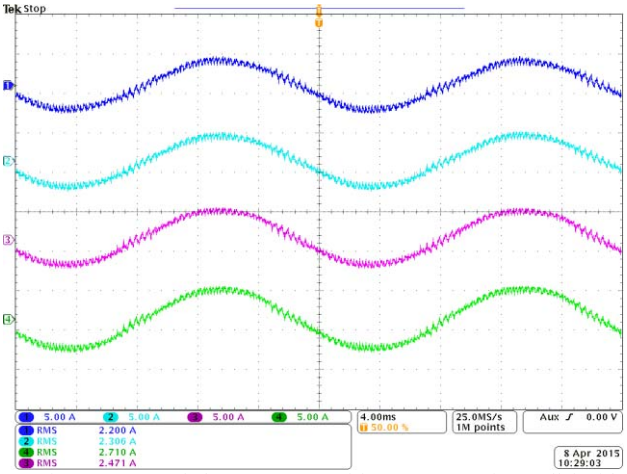

Fig. 13 Measured phase A current of four converters in parallel with no interleaving angle (Blue- Converter 1; Cyan- Converter 2; Magenta- Converter 3; Green- Converter 4)

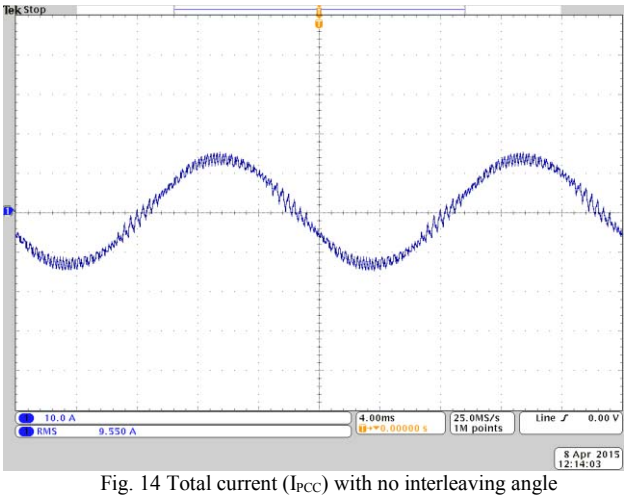

Fig. 14 Total current (I_{PCC}) with no interleaving angle

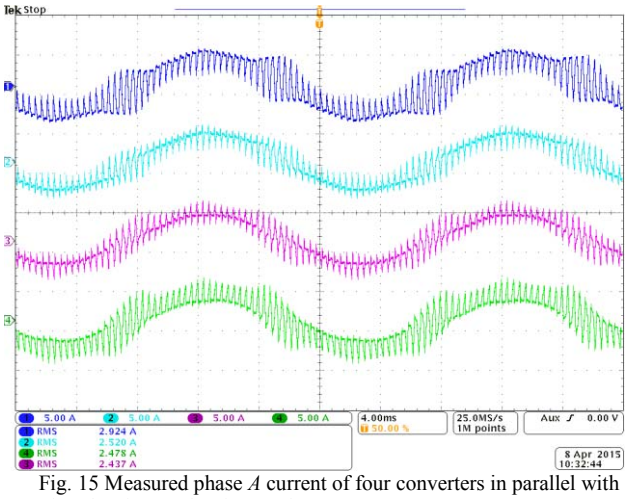

Fig. 15 Measured phase *A* current of four converters in parallel with an interleaving angle of 45º (Blue- Converter 1; Cyan- Converter 2; Magenta- Converter 3; Green- Converter 4)

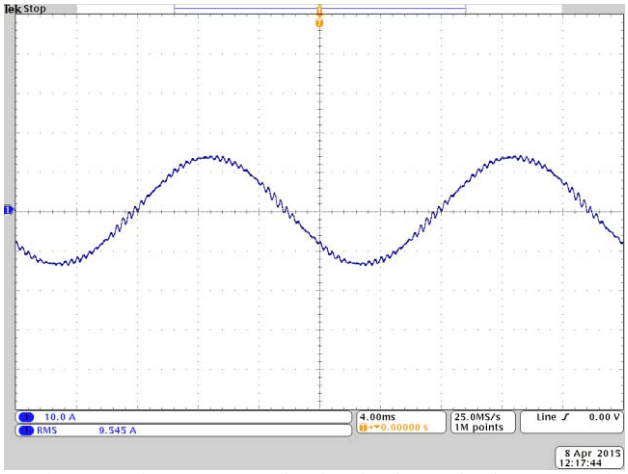

Fig. 16 Total current (I_{PCC}) when interleaving angle of 45º was used.

VI. Conclusion

This article analyzed the effect of the carrier interleaving angle on the total current and the RMS value of the DC link current of 4 parallel converters. In case of parallel converters the amplitude of the current ripple from the DC link and the total current depends on the interleaving angle between the carriers of the PWM signals. Several simulations have been carried out, from where the trend of the current ripple vs. interleaving angle for the DC link and total current was analyzed. It can be concluded that the minimum for the total THD and DC link current ripple can be found at different interleaving angles. Moreover, for different modulation indices the optimal interleaving angle differs. The interleaved modulation schemes were illustrated graphically, thus the cause of the current ripples during a modulation period can be tracked. Depending on the hardware configuration, with an optimal interleaving angle the size of the DC link capacitor can be reduced while the total current can comply with the standards. The concept has been validated for 4 parallel connected converters. Measurement results for multiple interleaving angles from 0º to 90º with a step of 15º for an output current of 10 A, where the modulation index was varied between 0.15 and 1.1 was presented. For the presented cases the total current THD has decreased from 9.45% to 1.65%

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