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Inrush Transient Current Analysis and Suppression of Photovoltaic Grid-Connected Inverters During Voltage Sag

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***Abstract*—The Inrush Transient Current (ITC) in the output of the photovoltaic grid-connected inverters is usually generated when grid voltage sag occurs, which can trigger the protection of the grid-connected inverters, and even destroy the semiconductor switches. Then, the grid-connected inverters will thus fail to ride through the voltage sag and even further cause more serious grid faults. This paper analyzes the generation principle of ITC and explores its influence factors, upon which, the suppression approaches are presented. Simulation and experimental results validate the theoretical analysis and the effectiveness of the proposed method.**

Keywords—the inrush transient current (ITC); photovoltaic grid-connected inverters; voltage sag; influence factors; suppression approaches

I. INTRODUCTION

The recent interest in solar energy is increasing tremendously. And the installation of large photovoltaic (PV) power generation systems, which are interconnected with the utility grid, is accelerating [1], [2]. However, the PV power generation systems may lead to instability when grid disturbances occur. The mainly reason is that the photovoltaic grid-connected inverters (PGI) is sensitive to grid disturbances, especially, the voltage sags [3], [4]. Therefore, to maintain the stability of the power system, one important grid code issued in many countries is that the PGI should success riding through voltage sags [5-8]. In order to meet the requirement of the grid code, firstly, PGI shouldn't disconnect from the grid by the reason of the fault current.

The fault current studies of grid-connected inverters have been widely reported in many literatures [2], [9-13]. In [9], a fault current limiter is used to reduce overcurrent in the converter, but it has the drawback of absorbing active power. Also, in the field of overcurrent reduction, there are other methods relying on the control scheme, which can avoid any increase of devices cost in the system. A study reported in [10] proposes a proportional-resonant (PR) current controller for the current limiter to make sure the output current without overcurrent, this current limiter is acquired indirectly by using an active power limiter. In [11] and [12], a proper reference current is selected to ride through grid faults and achieve requirements of different power quality. Among these methods, although low currents can be acquired, the control scheme does not assure its minimum value, but [13] overcomes this problem. On the other hand, for unbalanced voltage sags, there is also a control algorithm [2] to limit the peak current.

Obviously, the above mentioned technical literatures are all having concerns about the fault current limitation when the digital controller can take control of the output voltage of PGI. However, when a sudden decrease of grid voltage occurs, the output voltage of the PGI cannot change instantaneously. This is because of the time delay in its digital control system. Therefore, a large voltage drop will be generated on the output *L*-filters or *LCL*-filters of the inverter, which will further lead to an inrush transient current (ITC). This ITC may trigger the overcurrent protection of the inverter and in the worst case may even destroy the semiconductor switches, causing the disconnection of the PGI from the grid. The disconnection of too many PGI from the grid system will aggravate the voltage sags and lead to more severe grid faults.

Therefore, it is of great importance to study the ITC suppression solutions for the PGI. Obviously, a good understanding of the ITC influence factors will contribute a lot to this work. Actually, although the generation principle of ITC is not complex, the ITC influence factors have not been fully investigated so far. Therefore, in this paper, a thorough study of the ITC influence factors is carried out. Based on these findings, the appropriate ITC suppression approaches are then discussed. Finally, some experimental results are given to validate the theoretical analysis and the effectiveness of the proposed ITC suppression method.

II. PRINCIPLE AND CAUSE OF INRUSH TRANSIENT CURRENT

Fig.1 shows the basic control structure of the three-phase PGI. To explain the generation principle of ITC, the grid-connected inverter with *L* filter is analyzed for example. *u*, *v*, *i*, *L*, *R* represent the grid phase voltage, inverter output voltage, phase current, grid-connected inductance and its resistance,

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respectively. In this paper, a proportional-integral (PI) current controller is used, which is denoted by $G(z)$ in Fig.1.

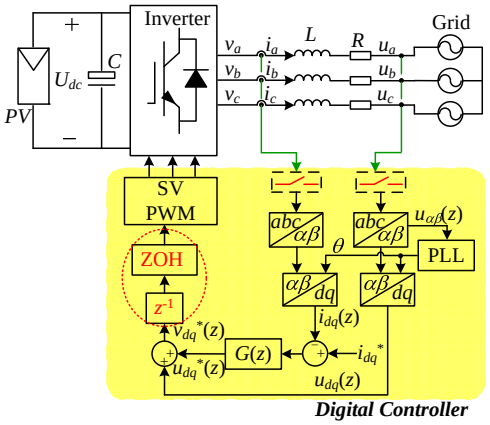

Fig. 1 The basic control structure of the three-phase PGI

As shown in Fig.1, the inverter output voltage reference v^*_{dq} is influenced by two components, which are the output of current controller u^*_{dq} and the direct feed-forward gird voltage u_{dq}. Due to the time inertial of the current PI controller, the direct feed-forward gird voltage is the effective component to control the inductor current during the process of the grid voltage sag.

Traditionally, the single-sampling approach is widely used in PGI digital control system, then the state variables (i.e., inductor currents and grid voltages) needed in the control algorithm are sampled once per switching period [14]. Because of this sampling approach, it is hard to guarantee that the instantaneous voltage can be sampled instantly, and with considering the zero-order hold (ZOH) effect of the PWM [14], [15], the valid output voltage, which can limit the ITC, need at least one and half switching period to be produced by DSP. Due to this delay, the voltage difference on the grid-connected inductor is large and will result in the rapidly rising of the inductor current in this short time. Thus, ITC is generated.

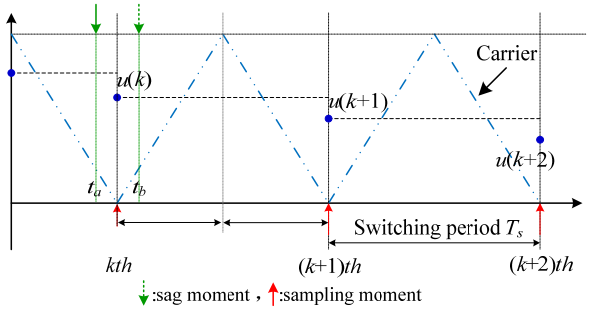

Fig. 2 Generation mechanism of the digital control delay

The generation mechanism of the digital control delay is shown in Fig.2. T_s is the switching period which is equal to the sampling period by using the single-sampling approach. In Fig.2, suppose that the voltage sags at t_a just before the *kth* sampling, the controller could catch the voltage. After one sampling period, the digital regulator could update the command signal to $u(k+1)$ based on the newly sampled state variables of the fault grid voltage, together with the ZOH effect of PWM, the digital control delay is at least $1.5T_s$ when the inverter could control the PGI current. However, as the sag occurs at t_b which lags behind the *kth* sampling, it's impossible to capture the fault voltage at this period. Only during the $(k+1)th$ sampling period, the effective voltage command $u(k+2)$ could be produced by the controller. Therefore, the delay expands to $2.5T_s$. During this $1.5\sim2.5T_s$ time delay, the DSP is not able to trace the variation of voltage, hence the PGI current rapidly increases to form the ITC. In the event the ITC was large enough and beyond the device component limit, a destructive damage of semiconductors could occur. Thus, the analysis the value of ITC is imperative in the next part.

III. Influence Factors Of Inrush Transient Current

According to Fig. 1, the mathematical model of the PGI in the three phase stationary reference frame is shown as following

$$\begin{cases} S_aU_{dc}-u_a-Ri_a-L\dfrac{di_a}{dt} \\ =S_bU_{dc}-u_b-Ri_b-L\dfrac{di_b}{dt} \\ =S_cU_{dc}-u_c-Ri_c-L\dfrac{di_c}{dt} \end{cases} \tag{1}$$

where S_a, S_b, S_c are switch function. In the three-phase three-wire system, the sum of the current is $i_a+i_b+i_c=0$, so (1) becomes

$$\begin{cases} L\dfrac{di_a}{dt}=v_a-u_a-Ri_a+\dfrac{1}{3}u_x \\ L\dfrac{di_b}{dt}=v_b-u_b-Ri_b+\dfrac{1}{3}u_x \\ L\dfrac{di_c}{dt}=v_c-u_c-Ri_c+\dfrac{1}{3}u_x \end{cases} \tag{2}$$

where v_a, v_b, v_c are the inverter output voltage. And their expression can be given by

$$\begin{cases} v_a=\left[S_a-\dfrac{S_a+S_b+S_c}{3}\right]U_{dc} \\ v_b=\left[S_b-\dfrac{S_a+S_b+S_c}{3}\right]U_{dc} \\ v_c=\left[S_c-\dfrac{S_a+S_b+S_c}{3}\right]U_{dc} \end{cases} \tag{3}$$

u_x is the sum of the three phase voltage and is given by

$$u_x=u_a+u_b+u_c \tag{4}$$

According to (2), any single phase equivalent circuit diagram can be seen in Fig. 3 when considering the balance sag.

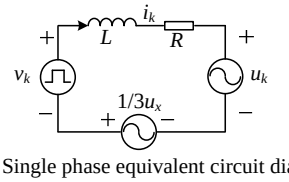

Fig. 3 Single phase equivalent circuit diagram

where k is the symbol of a, b, c phase. Before the voltage sags, according to Fig.3, the single phase voltage expression for this system can be given by

$$L\frac{di_k}{dt} = v_k - u_k - Ri_k + \frac{1}{3}u_x \tag{5}$$

When the voltage sag occurs, (5) changes to

$$L\frac{di_{k\_f}}{dt} = v_{k\_f} - u_{k\_f} - Ri_{k\_f} + \frac{1}{3}u_{x\_f} \tag{6}$$

where v_{k_f} , u_{k_f} and u_{x_f} are the output voltage of PGI, grid phase voltage and the sum of the three phase voltage, respectively.

In (6), the resistance of the grid-connected inductor is so small that its influence to the ITC can be neglected in the following analysis.

When a sudden decreasing of the grid voltage occurs, DSP may not sample the voltage instantly. Hence, the PGI output voltage remains unchanged, with $v_{k\_f}=v_k$. However, the grid voltage could be significantly different and (5) changes to:

$$L\frac{di_{k\_f}}{dt} = v_k + \frac{1}{3}u_{x\_f} - u_{k\_f} \tag{7}$$

In (7), for different sag type, the value of u_x is different. According to [16], the value of u_x under the four typical sag conductions are shown in Table I, where p_u is the sag depth and $p_u \in (0\ ,\ 1]$.

TABLE I u_x VALUE UNDER DIFFERENT SAG TYPE

Sag type	u_x	Sag type	u_x
(A)1Φ*n*	$(p_u\text{-}1)U_m$	(C)2Φ*n*	$(1\text{-}\ p_u)U_m$
(B)2Φ	0	(D)3Φ	0

where U_m is the normal phase voltage. Assuming that the three voltage symmetrical sag occurs in the grid, then $u_{x\_f}=0$ and $u_{k\_f}=p_u u_k$. At the sag moment, the current in the inductor can be given by

$$i_{k\_f} = \frac{1}{L}\int_{t_1}^{t_2}(v_k - p_u u_k)dt + i_0 \tag{8}$$

Thus, the ITC Δi_k is given by

$$\Delta i_k = \frac{1}{L}\int_{t_1}^{t_2}(v_k - p_u u_k)dt = \frac{1}{L}\Delta u \Delta t \tag{9}$$

where $\Delta t=t_2\text{-}t_1$ represents the digital control delay. $\Delta u=v_k\text{-}p_u u_k$ represents the voltage difference of the inductor. It shows obviously that ITC is influenced by the digital control delay Δt, the voltage difference Δu and the inductor L. v_k is the PGI output voltage and kept unchanged during Δt, while the grid voltage is changed to $p_u u_k$.

Under normal grid-connected condition, assuming that the power factor is unit, hence the difference between u_k and v_k is very small compared with the fault condition, approximately, $u_k \approx v_k$. So (9) can be rewritten by

$$\Delta i_k \approx \frac{1}{L}\int_{t_1}^{t_2}(u_k - p_u u_k)dt = \frac{1}{L}(1-p_u)u_k \Delta t \tag{10}$$

According to (10), Figs.4-6 show how the ITC are influenced by these factors.

1) The influence of grid-connected inductor L and the digital control delay Δt to the ITC: The influencing factors were set by following conditions (see Fig. 4):

a) CASE A:

u_k=311V p_u=50% L=2mH $\Delta t=2.5T_s$=75μs

b) CASE B:

u_k=311V p_u=50% L=4mH $\Delta t=2.5T_s$ =125μs

c) CASE C:

u_k=311V p_u=50% L=2mH $\Delta t=1.5T_s$ =125μs

By the comparison between *CASE B* and *CASE C* of Fig. 4, given that the grid-connected inductor is 2mH, the ITC is larger. As shown in *CASE A* and *CASE C*, the only difference is the sampling time which leads to the digital control delay are 75μs and 125μs, respectively. Clearly, the longer the digital control delay is, the larger the ITC is.

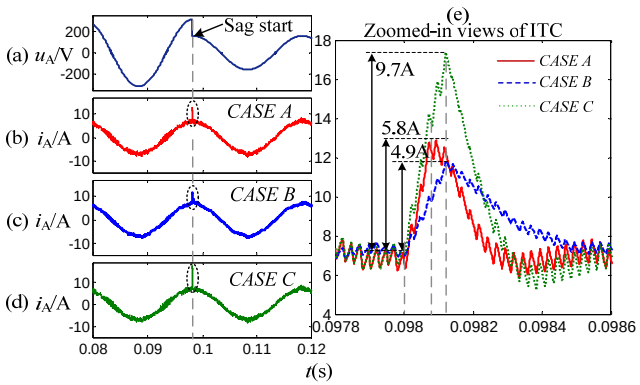

Fig. 4 The influence of L and the digital control delay Δt to the ITC: (a) Phase A grid voltage, (b)-(d) phase A grid-connected current, and (e) zoomed-in views of ITC.

2) The influence of sag depth p_u to the ITC: The influence factors were set by the following conditions (see Fig. 5):

a) CASE A:

u_k=311V p_u=70% L=2mH Δt=125μs

b) CASE B:

u_k=311V p_u=50% L=2mH Δt=125μs

c) CASE C:

u_k=311V p_u=30% L=2mH Δt=125μs

As shown in Fig. 5, it's clearly to see that the ITC is 13.6A when the sag depth is 70%, which is larger than the other two cases (9.7A and 5.8A).

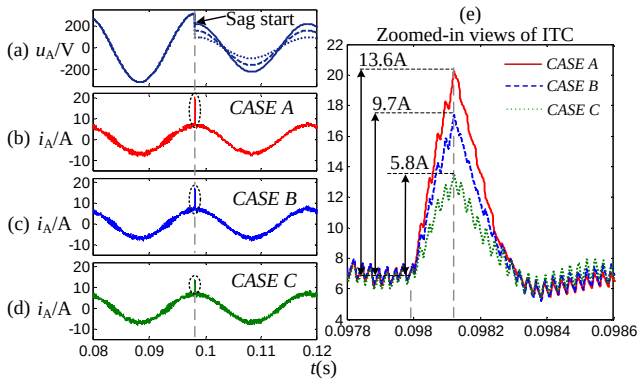

Fig. 5 The influence of sag depth p_u to the ITC: (a) Phase A grid voltage, (b)-(d) phase A grid-connected current, and (e) zoomed-in views of ITC.

3) The influence of sag time to the ITC: The influence factors were set by the following conditions (see Fig. 6):

a) CASE A:

u_k=200V p_u=70% L=2mH Δt=125μs

b) CASE B:

u_k=100V p_u=70% L=2mH Δt=125μs

c) CASE C:

u_k=0V p_u=70% L=2mH Δt=125μs

Fig. 6 shows the ITC at different sag time. The ITC is 8.8A, 4.4A, 0A, respectively. It's easy to find out that the ITC is much larger as the voltage reaches the peak value.

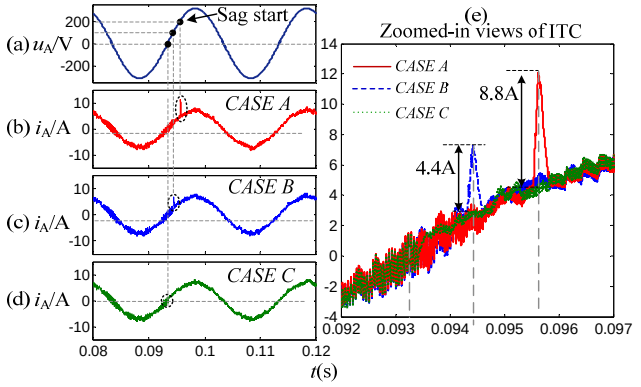

Fig. 6 The influence of sag time to the ITC: (a) Phase A grid voltage, (b)-(d) phase A grid-connected current, and (e) zoomed-in views of ITC.

The validity of the (10) is demonstrated by the simulation results above.

In the high power PGI, the switching frequency can be hundreds hertz per second [17]-[18]. Moreover, considering the worst voltage sag condition, the ITC could reach the destructive value of the semiconductor.

IV. Current Suppression Method

From the above analysis, obviously, the ITC can be suppressed by regulating the influence factors. The ITC can be substantially reduced by using a larger grid-connected inductance, adopting the multi-sampling scheme approach, etc. However, if the system is not able to change these influence factors, the methods mentioned above will be invalid. Due to the time delay of ITC can be dozens of μs, to suppress this inrush current, this paper proposed a hardware suppression method to limit the ITC under the safe range.

As shown in Fig.7, the hardware current limiter in PGI is positioned between the DSP controller and the IGBT driver, when a phase current is sampled with a value exceeding the limiting value, the limiter can thus set a low level of the PWM signals to the IGBT driver. By shutting down the IGBT about dozens of μs, the ITC is suppressed and then the PWM signals resume normal again. Thus, the PGI overcurrent protection will not be triggered and the system will continuously work in the grid-connected condition. This is biggest different between the hardware current limiter and the overcurrent protection circuit. Meanwhile, the limiter does not influence the normal condition. The block diagram of hardware current limiter is shown in Fig.8.

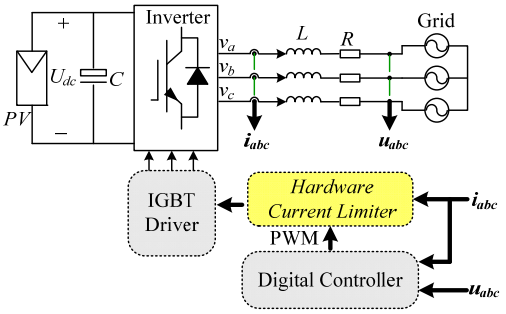

Fig. 7 The location of the hardware current limiter

As shown in Fig. 8, the first part of hardware current limiter is the current sampling circuit whose function is removing the higher harmonics from the sampled current and properly scaling the sampled current. Both the reference current circuit output I_{ref} and the processed current signal i_{sample} are sent to a current comparing circuit. The kernel of the comparing circuit is the hysteresis comparator, which has two thresholds (I_{T1}, I_{T2} and I_{T1}> I_{T2}). This hysteresis comparator is realized by a differential comparator, like LM339. When i_{sample} is larger than I_{T1}, the comparator output Out_C goes low. When i_{sample} is lower than the value of I_{T2}, Out_C will go high. Suppose that Out_C is low, when the PWM signals pass through the PWM blocking circuit which is realized by an *AND* gate, the PWM signals would be set to low level and until Out_C is changed to a high level, the PWM signals then become normal. According to this mechanism, the ITC can be suppressed. This is quite different from the overcurrent protection circuit which will shut down the PGI. Although the above discussion is with one phase case, it also applies to three-phase system.

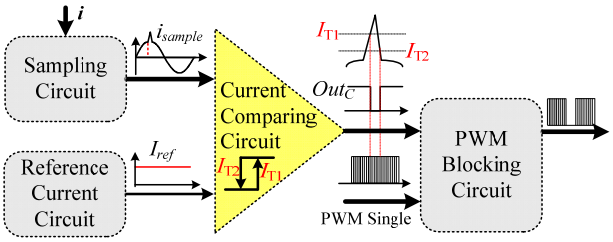

Fig. 8 The block diagram of hardware current limiter

The hardware of the current limiter is shown in Fig. 10. Because the devices used in the hardware limiter is inexpensive, the additional cost of the limiter is quite little.

The simulation results of ITC without and with the hardware current limiter are shown in Fig. 9, where the influence factors were set by the following condition

$$u_k=311\text{V} \quad p_u=70\% \quad L=2\text{mH} \quad \Delta t=125\mu s$$

In Fig. 9, *CASE A* and *B* are the ITC waveform without and with the hardware current limiter. In *CASE B*, the current is suppressed under 11.2A due to the hysteresis of comparator. When the current goes beyond the first threshold (11.2A), the PWM signals are blocked, and this blocking status remains until the current goes down below the second threshold (8.6A). Then the PWM signals resume normal.

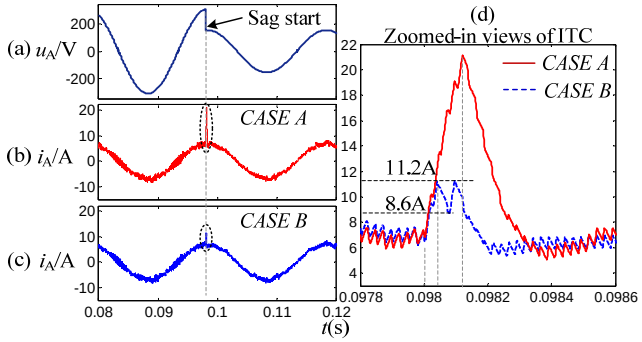

Fig. 9 ITC without and with the hardware current limiter: (a) Phase A grid voltage, (b)-(c) phase A grid-connected current, and (d) zoomed-in views of ITC.

V. Experimental Result

To examine the theoretical analysis and the current limiter proposed in this paper, the experiments with a PGI system are performed shown in Fig.10. In the experimental setup, a voltage sag generator (VSG) is used to simulate the voltage sags. And the inverter is controlled by DSP TMS320F28335. The photovoltaic power source is implemented by a programmed Chroma DC source. The parameters of the actual system are given in Table II.

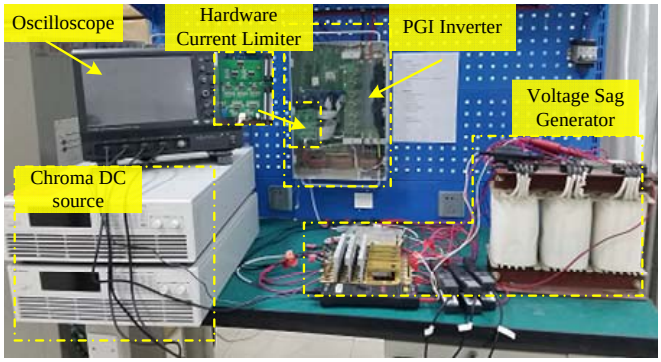

Fig. 10 Experimental system

TABLE II Experimental Parameters

Grid phase voltage amplitude	311 V
Grid frequency	50 Hz
Grid inductance	2.0 mH
DC filter capacitance	1660 μF
Switching frequency	20 kHz
Voltage sag type	Three phase voltage sags
Sag duration time	0.5 s

In the actual system, the grid voltage and current are sampled by the hardware circuit. Due to the existence of the low-pass filter circuit, a hardware delay would be inevitably introduced in digital control. In this PGI system, the hardware delay is $t_d=50\mu s$.

In Fig. 11, the influence factors of ITC were set by the following condition:

$$u_k=311\text{V} \quad p_u=50\% \quad L=2\text{mH} \quad \Delta t=1.5T_s+ t_d=125\mu\text{s}$$

As shown in Fig. 11, under the normal condition, the grid-connected current is 7.0A, yet the ITC is 9.7A as the voltage sags. Substituting the influence factors (L=2.0mH, p_u=50%, u_{ks}=311V, Δt=125μs) into (10), the theoretical result of ITC is 9.69A, which is consistent with the experimental result.

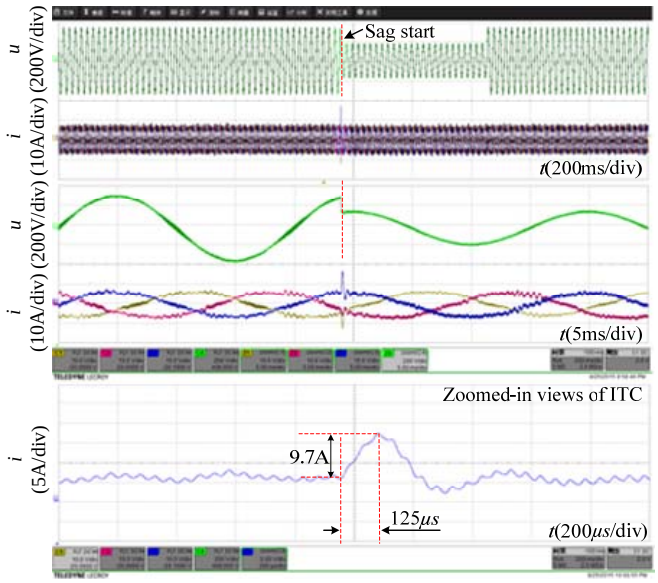

Fig. 11 The experiment waveform when voltage sags at peak value

In Fig. 12, the influence factors of ITC were set as below

$$u_k=190\text{V} \quad p_u=50\% \quad L=2\text{mH} \quad \Delta t=1.5T_s+ t_d=125\mu\text{s}$$

Under this conduction, according to (10), the calculated theoretical result of ITC is 6.0A, which is similar to the experimental result (6.2A). By comparing Fig.11 and Fig.12, the analysis of Fig. 6 is verified.

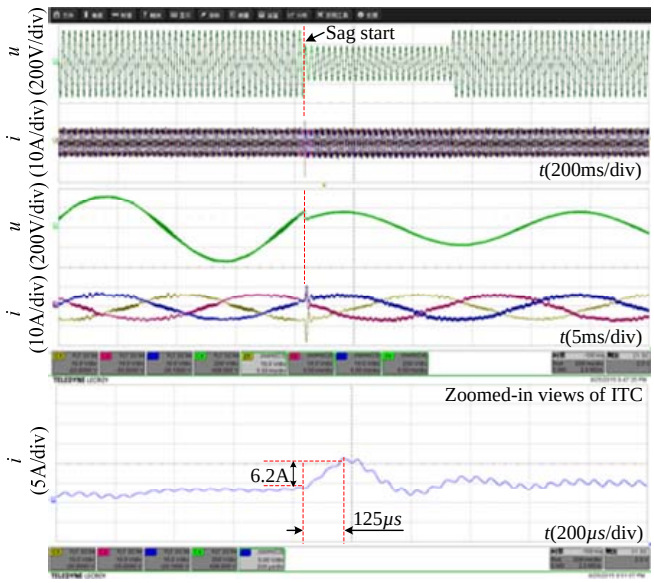

Fig. 12 The experiment waveform when voltage sags at 190V

In Fig.13 and Fig.14, the influence factors of ITC were set by the following conditions:

u_k=311V p_u=70% L=2mH Δt=2.5T_s+ t_d=175μs

u_k=311V p_u=50% L=2mH Δt=2.5T_s+ t_d=175μs

As shown in Fig. 13, when the sag depth is 70%, the ITC is 19.0A which is larger than the ITC in Fig. 14. The only difference between two Figures is that sag depth is changed to 175μs in Fig. 14 from 125μs in Fig. 11, consequently the ITC increases to 13.6A from 9.7A. By substituting the above influence factors into (10), the ITC are 19.05A and 13.56A, respectively. By observing the results given in Fig. 11, Fig. 13 and Fig. 14, obviously, the deeper of the voltage sag and the longer of the digital control delay, the greater destructive of ITC.

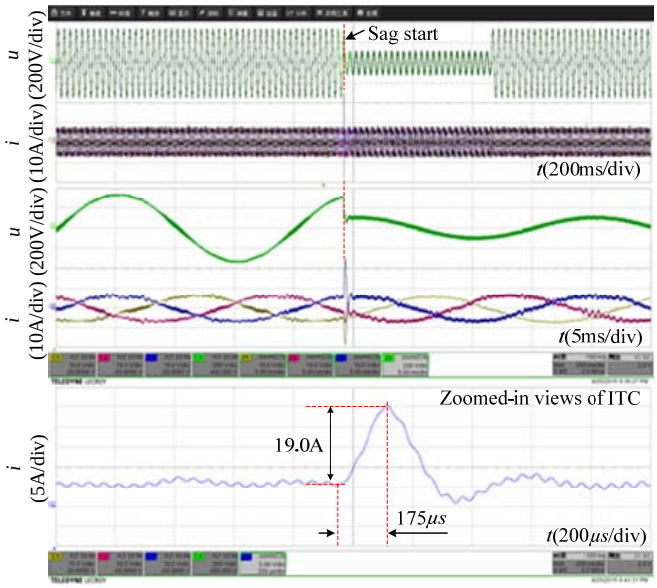

Fig. 13 The experiment waveform when the sag depth is 70%

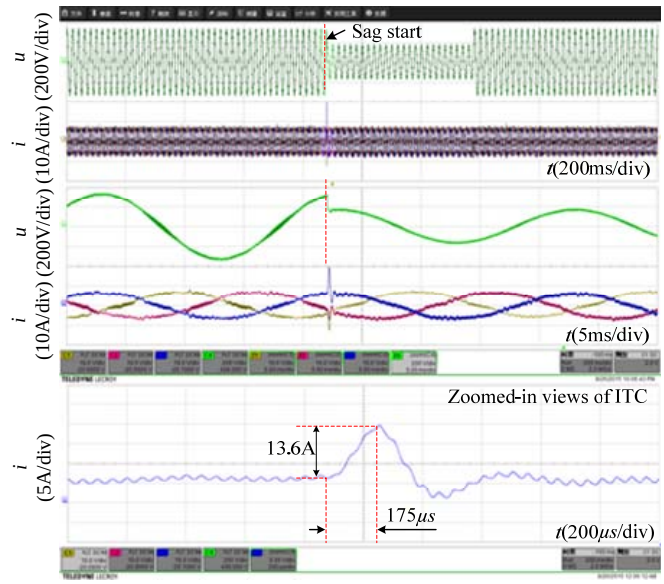

Fig. 14 The experiment waveform when the digital control delay is 175*us*

Fig. 15 shows the effect of the hardware current limiter, the influence factors of ITC were the same as that of Fig. 13. The current limiter suppresses the current under 13.1A, which should be 20.56A in Fig. 13. Meanwhile, because of the hysteresis comparator, as the current is less than 8A, the current limiter releases the PWM signals and the current increases again. In this case, obviously, the PGI does not disconnect from grid. Therefore, Fig. 15 demonstrates the effectiveness of the hardware current limiter.

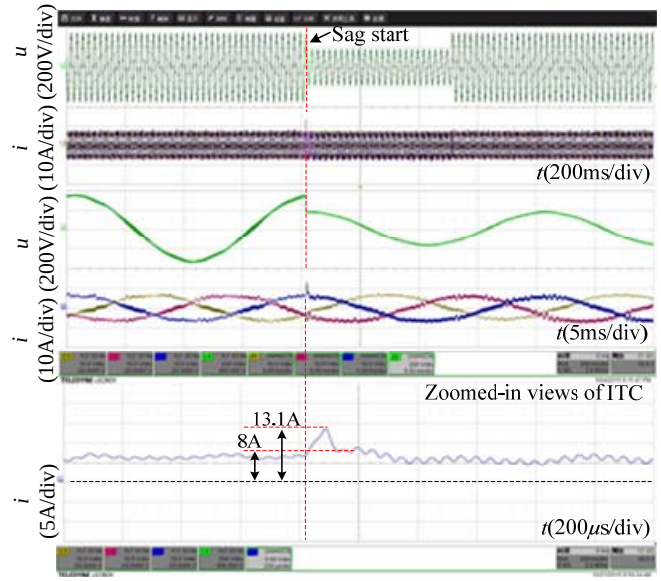

Fig. 15 The experiment waveform with the hardware current limiter

VI. CONCLUSION

In this paper, the influence factors of the Inrush Transient Current (ITC) and its suppression method are presented. By using a hysteresis comparator, the proposed hardware current limiter has fast and excellent suppression ability to suppress the ITC. Thus, the PGI can uninterruptedly work in the grid-

connected condition without the influence of the ITC. Both simulation and experimental results validate the theoretical analysis and the proposed suppression method. Moreover, the proposed methods in this paper can also be used in other applications, where PWM inverters are used.

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