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Adjustable Speed Drives and Power Quality

Challenges and Cost-Effective Opportunities

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Abstract—**This paper provides an overview and proposes cost-effective and efficient opportunities in improving power quality in Adjustable Speed Drive (ASD) systems. In particular, use of Electronic Inductor (EI) technique in single drives to overcome the existing challenges in conventional front-end rectifier systems with focus on partial loading conditions is investigated. Moreover, the effectiveness of EI technique along with a phase-shifted current control in terms of improved grid current quality in multi-drive configurations is addressed. Furthermore, a novel DC-link current modulation scheme for multi-drive systems is proposed. Experimental and simulation results verify the effectiveness of the theoretical analysis.**

Keywords—*adjustable speed drive; electronic inductor; harmonic mitigation; multi-drive; three-phase diode rectifier.*

I. INTRODUCTION

Power quality issues of power electronic systems remain as the main obstacle in developing smarter and clean power grids. The deployment of such technologies can be accelerated by impacting societal perspective through developing more cost-effective power electronic systems with lower complexity. This can be done, by targeting major sources of power quality issues.

Nowadays, Adjustable Speed Drive (ASD) systems are known as one of the major sources of harmonics, which deteriorate the power quality [1]-[6]. Employing adjustable speed technology for motor-drive applications can significantly improve their energy efficiency. However, due to the employment of line-commutated rectifiers (Fig. 1(a)), from power quality point of view the main concern with ASD systems is the generation of current harmonics which may lead to high losses and stability issues in the grid. While improving the input current quality employing Power Factor Correction (PFC) technique is fully accomplished in single-phase systems, it remains as a quite challenging task in three-phase motor drive applications. Although prior art methods [7]-[9] can significantly improve the input current quality, but due to their
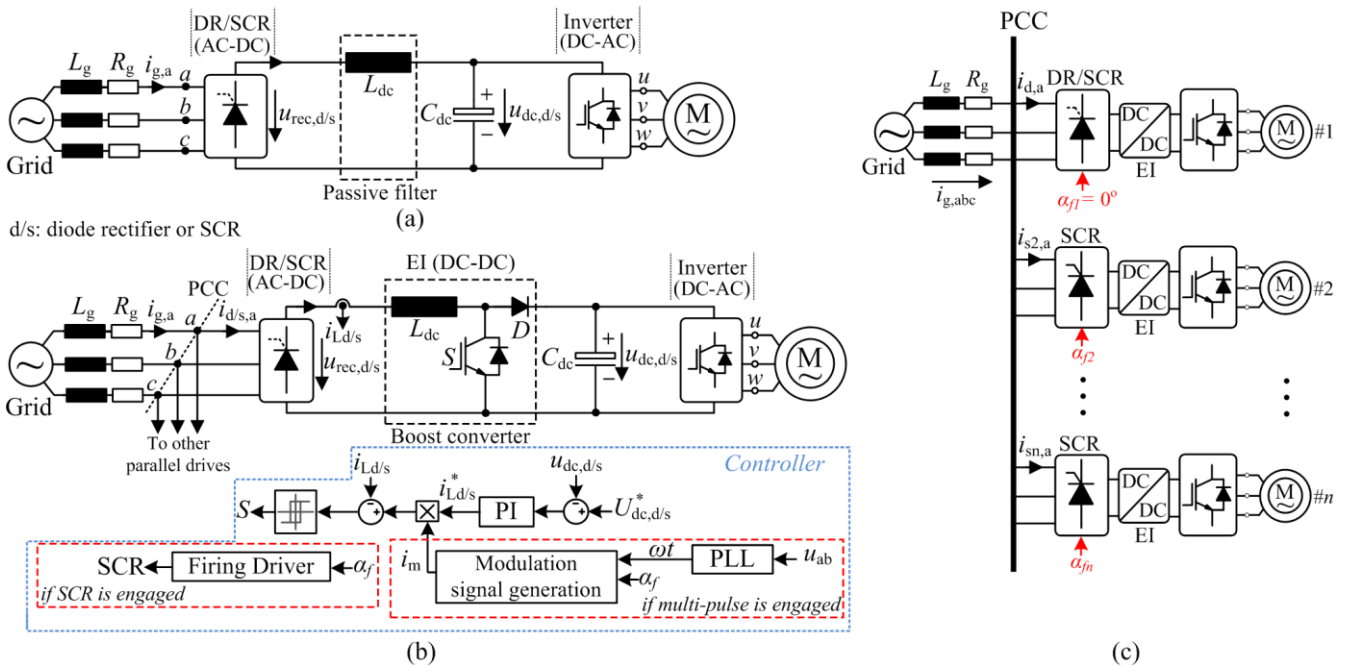

Fig. 1. ASD system architecture with applying: (a) passive filtering at the DC-link, (b) EI technique using boost converter, (c) multi-drive configuration with phase-shifted current control using SCR and current modulation employing the EI technique.

high complexity, cost, and low efficiency they have not gained much attention in ASD applications. Moreover, three-phase power electronics systems with a new specification (according to IEC 61000-3-12 [10], Tables 4 and 5) can even generate more harmonic currents to improve power quality of grids at medium voltage levels. For example, for R_{sce} = 120 and based on Table 4 in IEC61000-3-12, THD_i and the fifth current harmonic should be below 48% and 40%, respectively [10]. Therefore, majority of ASD systems are using Diode Rectifier (DR) or Silicon Controlled Rectifier (SCR) with passive filtering.

This paper provides an overview and proposes possible cost-effective and efficient opportunities in improving power quality in ASD systems. First, the short-comings of common passive filtering approaches such as employing DC-side inductors are addressed (Fig. 1(a)). Secondly, an active filtering scheme based on the Electronic Inductor (EI) concept (Fig. 1(b)) [3]-[6], [11]-[13] is analyzed. Furthermore, considering the wide-spread use of ASD systems, the application of the proposed harmonic mitigation scheme is also investigated on multiple drive configurations (Fig. 1(c)) [3]-[6], [12], [13]. The principle of the proposed scheme lies in modulating the DC-link current and applying phase-shifted current control to the AC-DC rectification stage to shape multilevel grid currents. The effectiveness of the proposed solutions is validated experimentally.

II. CONVENTIONAL THREE-PHASE RECTIFIER WITH PASSIVE FILTER

In this section, the behavior of the three-phase line-commutated rectifiers (i.e., DR or SCR) with conventional passive filtering (Fig. 1(a)) is first analyzed to understand their drawbacks and facing challenges. Generally, the passive filtering solution has two major drawbacks. First, in order to obtain the maximum performance (i.e., THD_i ≈ 30% and Power Factor (λ) ≈ 0.95), it requires a large inductor. Fig. 2 illustrates the input current waveforms with their corresponding harmonic distributions at two different inductor values at the rated power. As it can be seen, only for large inductor values (i.e., L_{dc} = 30 mH), the THD_i and λ can be improved. In practice the inductance value is selected in the range of 3-5% (e.g., L_{dc} = 3 mH), which can be calculated as,

$$Z_L(\%) = \frac{X_L \hat{I}_{(1)}}{\hat{U}_N} \qquad (1)$$

where X_L is the inductor impedance at grid frequency, $\hat{I}_{(1)}$ is the peak amplitude of grid fundamental current and $\hat{U}_N$ is the peak amplitude of the grid phase voltage.

The second shortcoming is that its effective impedance in (1) is dependent on the load current. Fig. 3 illustrates the performance of the passive filtering applying same inductor values in Fig. 2 at a partial loading condition (P_o = 10%). As it can be seen, even with a large inductor value, the performance of the system significantly reduces and cannot effectively reduce the generated harmonics. In fact, this is an important issue as majority of ASD applications operate in partial

Fig. 2. Simulated input current waveforms ($i_{g,a}$) in a three-phase diode rectifier with passive filtering and EI techniques at full power P_o = 100% (i.e., here 7.5 kW): (a) input current waveforms and (b) corresponding harmonic distributions.
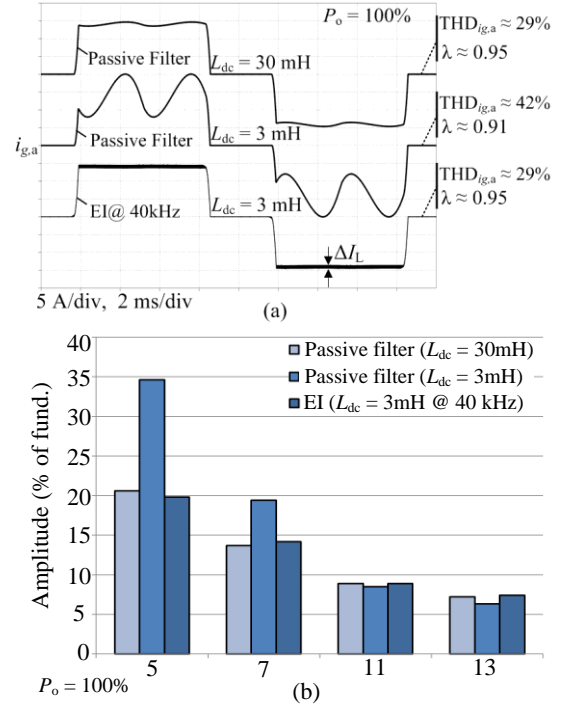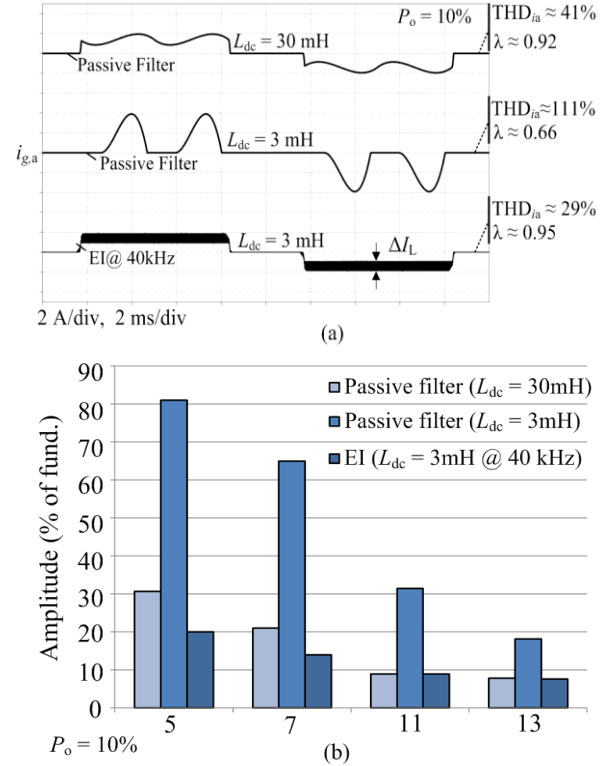

Fig. 3. Simulated input current waveforms ($i_{g,a}$) in a three-phase diode rectifier with passive filtering and EI techniques at full power P_o = 10% (i.e., here 750 W): (a) input current waveforms and (b) corresponding harmonic distributions.

loading conditions. Therefore, in order to cover wide range of output power levels with satisfying THD$_i$ and λ a large inductor is required. However, using a large inductor substantially impairs the power density and dynamic behavior of the system. It should be noted that, in order to meet the required THD$_i$ and λ at partial loading conditions using swinging chokes can be a possible solution. However since the range of load profile is quite wide in ASD applications, employing swinging chokes also results in a large inductor. Another alternative passive solution introduced to improve the input current quality of the line-commutated rectifiers is using slim DC-link capacitor. Using slim DC-link capacitors in addition to reduction of the required hold-up time also as discussed in [2] would result in a more complicated situation as the harmonic performance is highly dependent on the load profile.

III. ELECTRONIC INDUCTOR

The simple and cost-effective solution to maintain the performance of the system in terms of THD$_i$ and λ is to use EI technique (Fig. 1(b)). The basic idea of the EI is to replace the bulky DC-side inductor with a relatively small one by incorporating a DC-DC converter emulating the behavior of an ideal infinite inductor [5]-[6]. In this situation, the input current (i.e., $i_{g,abc}$) will be a square-wave with 120 degrees conduction with THD$_i$ ≈ 30% and λ ≈ 0.95. As Fig. 2 and Fig. 3 clearly show, the main advantage of this technique is its load independence performance (i.e., THD$_i$ ≈ 30% and λ ≈ 0.95 are maintained regardless of the output power level).

Here, the EI technique is implemented using a boost topology. Therefore, same operating principle for a boost converter operating in Continuous Conduction Mode (CCM) applies to EI as well. The only difference is that the switching frequency (f_{sw}) and boost inductor (L_{dc}) should be calculated considering the minimum intended output power, so the converter can maintain its performance over wide range of operating powers which is given as [6],

$$L_{dc} > \frac{D(1-D)^2 U_{dc,d/s}^2}{2P_{o,min} f_{sw}} \qquad (2)$$

For instance, as it is shown in Fig. 3(b), the EI can continue operating in CCM even at 10% of its rated power by suitable selection of the inductor and switching frequency according to (2).

IV. MULTI-DRIVE CONFIGURATION

In many applications it is a common practice to employ parallel connected drive units (e.g., multi-pump arrangement) [14]. In this situation the application demand is met using multiple modestly sized motor units rather than one single large unit. Hence, depending on the applied control strategy such as multi-follower or multi-master the load can be shared across the drive units evenly or unevenly, respectively. This configuration can better satisfy energy efficiency especially under partial load conditions by keeping majority of units in standby mode. More importantly, by implementing a proper interaction among the parallel connected units the input
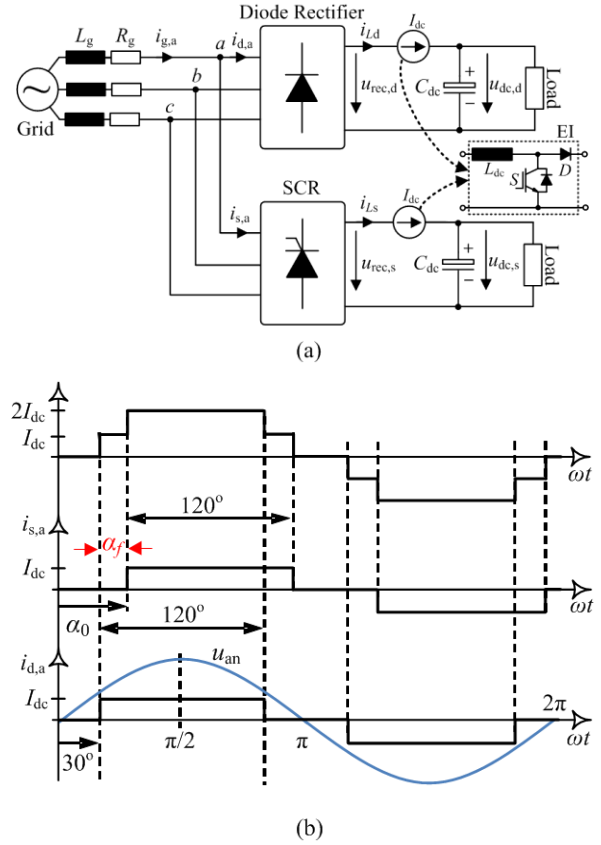

(a)

(b)

Fig. 4. Simplified representation of phase-shifted current control applied to two rectifier system: (a) system schematic with EI units showing as ideal current sources, (b) stair-case waveform of the total input current ($i_{g,a}$) with flat current modulation.

current quality can be significantly improved [3], [5], [12], [13], [15]. Here, the EI technique with a phase-shifted control in a multi-drive configuration is analyzed (Fig. 1(c)).

A. Phase-Shifted Current Control

Fig. 4(a) shows a simplified representation of Fig. 1(c) with two rectifier units using the EI technique. As already mentioned, the EI technique will act as a current source at the dc-link enabling the control of the current at a constant level (i.e., I_{dc}). According to Fig. 4(b), combining the SCR and the diode rectifier offers a possibility to improve the grid current quality by properly phase-shifting ($α_f$) the SCR currents, which in return can cancel out certain harmonics of the total currents drawn by the diode rectifier (i.e., $i_{d,abc}$). Notably, in the case of the first rectifier unit since $α_f = 0$ a three-phase DR can be used instead of SCR (see Fig. 1(c) and Fig. 4(a)).

It can be further explained by Fig. 4(a), which exemplifies that the hth harmonic can completely be eliminated by introducing a phase-shift of 180°/h to the SCR (i.e., $α_f = 180°/h$). In order to further illustrate the influence of the phase-shift of the SCR unit on the grid current quality, the performance of the system has been analyzed by applying a
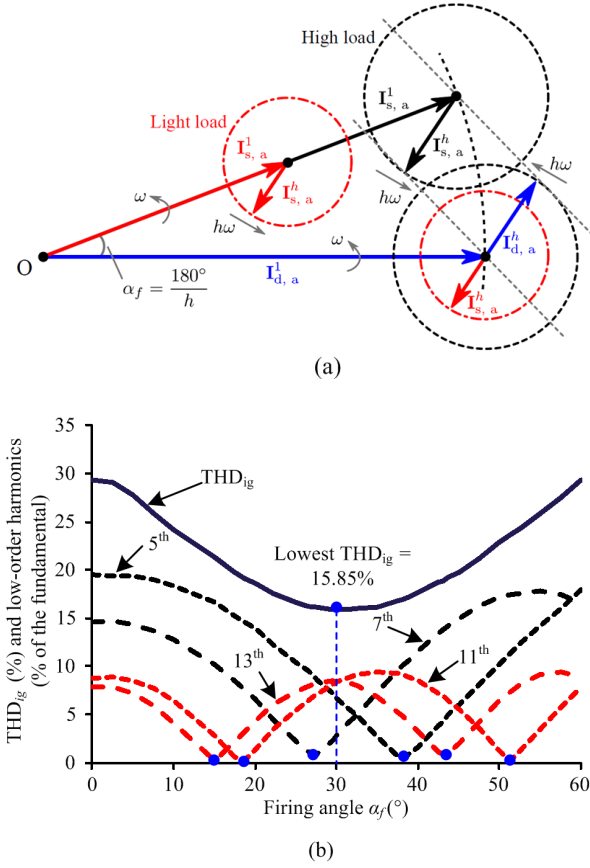
(a)

(b)

Fig. 5. Improving grid current quality based on phase-shifted current control with flat current modulation: (a) basic principle, (b) THD_{ig} as a function of α_f [3], [12].

wide range of the phase-shifts. As it can be seen in Fig. 5(b), an increase of the firing angle can alter the power quality of the grid current by affecting low order harmonics (i.e., 5th, 7th, 11th, and 13th). As it can be seen, the lowest THD_i is observed in the case of $\alpha_f = 30°$.

Notably, the maximum harmonic reduction can be attained when both rectifier units draw equal amount of currents from the grid. This condition cannot easily meet as the ratio of the rectifier's output powers changes as a function of the applied firing angle [2]. This fact happens due to the dependency of the SCR unit rectified voltage on the firing angle. The average rectified voltage of both units can be given as,

$$U_{rec,s} = U_{rec,d} \cos(\alpha_f) = \frac{3}{\pi} U_{LL} \cos(\alpha_f) \qquad (3)$$

where $U_{rec,s}$ and $U_{rec,d}$ are the average rectified voltages of the SCR and diode rectifier, respectively. Therefore, as the firing angle increases the average voltage reduces and in return the boost converter draw more current in order to adjust the output voltage at a constant value. Now ignoring the power losses on the boost converters the following can be obtain:

$$\frac{P_{o,s}}{P_{o,d}} = \frac{U_{dc,s} \times I_{os}}{U_{dc,d} \times I_{od}} \approx \frac{U_{rec,s} \times I_{Ls}}{U_{rec,d} \times I_{Ld}} \qquad (4)$$

with $P_{o,s}$ and $P_{o,d}$ denoting the output power of the SCR and diode rectifier, respectively, and I_{os} and I_{od} being the average output current of each rectifier. Substituting (3) in (4) and the corresponding condition which makes both rectifiers to draw equal amount of current (i.e., $I_{Ls} = I_{Ld}$) is,

$$\frac{P_{o,s}}{P_{o,d}} = \cos(\alpha_f) \qquad (5)$$

Therefore, as long as the above condition holds, the maximum harmonic elimination can be obtained. However, in reality each drive unit may run at different power condition and as it is shown in Fig. 5(a) (i.e., Light load), having different loading conditions at each rectifier units results in unequal input currents and consequently incomplete cancellation of the harmonics of interest [3], [12].

B. DC-Link Modulation Scheme

Although an appropriate adjustment of the phase angle of the SCR unit can contribute to an improvement of the grid current quality, but in order to further improve the current quality and reduce the effect of unequal loading condition on the harmonic reduction performance, a current modulation technique can be applied to the EI technique [3]-[6], [11]-[13]. The current modulation method is based on the calculation of a pre-programmed switching pattern for the dc-link current to achieve elimination of low order harmonics in the grid currents. In this approach, a DC-link current modulation scheme is generated by adding or subtracting the phase-displaced current levels. Fig. 6(a) illustrates the principle of this multi-pulse modulation technique ($i_{s,a} = p_0 + p_1 - p_2$). Notably, in the case of the first rectifier unit $\alpha_f = 0$.

As it is shown in Fig. 6(a), the new modulation signal $i_{s,a}$ consists of flat pulses p_0, p_1, and p_2. Hence, following the Fourier series, the harmonic components of each flat pulse can be expressed as,

$$p_i^h(t) = a_i^h \cos(h\omega t) + b_i^h \sin(h\omega t) \qquad (6)$$

in which, $i = 0, 1, 2$, and $h = 1, 3, 5, 7, \ldots$ is the harmonic order, ω the fundamental grid angular frequency, a_i^h and b_i^h are the Fourier coefficients that are given by,

$$\begin{cases} a_i^h = \frac{2m_i}{h\pi} \left[-\sin(h\alpha_i) + \sin(h\alpha_i + h\beta_i) \right] \\ b_i^h = \frac{2m_i}{h\pi} \left[\cos(h\alpha_i) - \cos(h\alpha_i + h\beta_i) \right] \end{cases} \qquad (7)$$

Notably, in the case of having only flat current modulation (i.e., Fig. 4(b)) $m_1 = m_2 = 0$. Subsequently, according to the superposition principle, the harmonic components of the modulation signal can be obtained as,

$$\begin{aligned} i_{s,ph}^h(t) = &(a_0^h + a_1^h - a_2^h)\cos(h(\omega t - \theta_{ph})) \\ &+ (b_0^h + b_1^h - b_2^h)\sin(h(\omega t - \theta_{ph})) \end{aligned} \qquad (8)$$
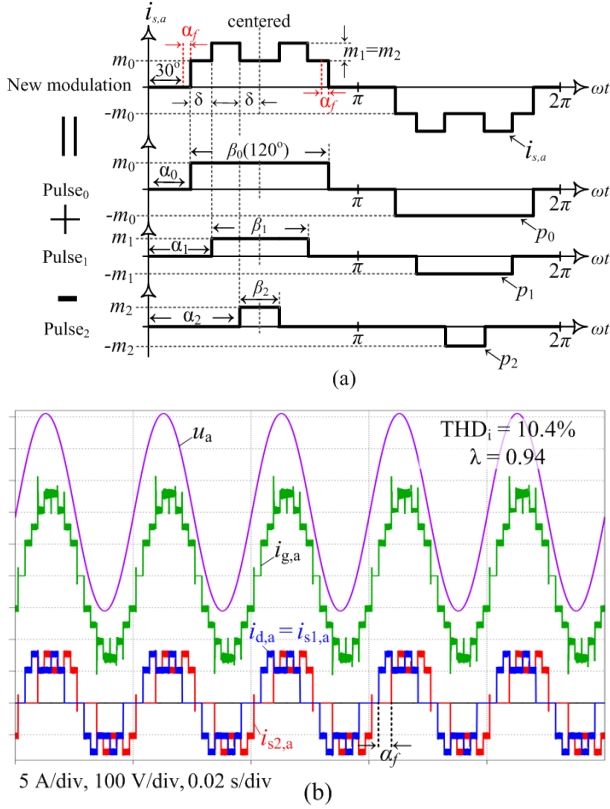
Fig. 6. Illustrations of the multi-pulse modulation scheme for harmonic reduction: (a) detailed analysis, (b) simulated waveforms applying multi-pulse modulation (i.e., adding one new current level) with phase-shifted control for two drive units optimized for minimum THD$_i$ using Table I parameters.

in which $ph = a$, b, and c with $\theta_a = 0$, $\theta_b = -120$, and $\theta_c = 120$. As a result, the h-order harmonic magnitude ($I_{s,ph}^h$) of the resultant DC-link modulation scheme can be expressed as,

$$I_{s,ph}^h = \left[\left(a_0^h + a_1^h - a_2^h \right)^2 + \left(b_0^h + b_1^h - b_2^h \right)^2 \right]^{1/2} \qquad (9)$$

Finally the following condition should hold,

$$\begin{cases} \alpha_1 + \alpha_2 = 2\alpha_0 + 60^o \\ \alpha_0 < \alpha_1 < \alpha_2 < \alpha_0 + 60^o \end{cases} \qquad (10)$$

As Fig. 6(b) exemplifies, applying the above current modulation in conjunction with phase-shifting results in a multi-level current waveform at the grid side. As it can be seen the input current quality is improved by obtaining THD$_i$ = 10.4% and λ = 0.94. In that case, the resultant total harmonics of the grid current ($i_{g,abc}^h(t)$) for parallel connected rectifier systems will become,

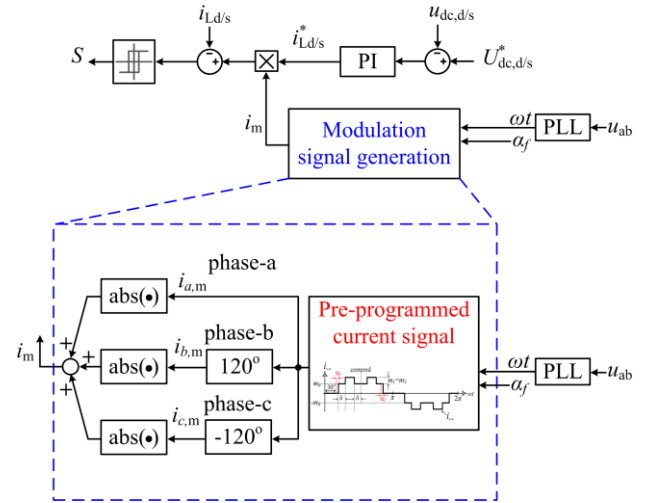$$i_{g,abc}^h(t) = i_{d,abc}^h(t) + i_{s,abc}^h(t) \qquad (11)$$

Fig. 7. Implemented control structure and synthesis process of the proposed DC-link current modulation scheme for the drive systems shown in Fig. 1(b) and (c).

Hereafter, according to (9) and (11) it is possible to achieve harmonic cancellation by calculating harmonic magnitude of the total input current and solving $I_g^h = 0 \, (h \neq 1)$ and $I_g^1 = M$ with M being the desired modulation index. In order to obtain more suitable solution to reduce the harmonics of interest, an optimization can be carried out [2]. Using optimization allows applying the maximum allowable harmonic levels defined by the grid code [10].

As Fig. 7 illustrates, the reference current is formed by multiplying the voltage controller output by a pre-programmed modulation signal. Fig. 7 depicts the basic concept in generating the modulation signal (i.e., i_M) following Fig. 6(a). As it can be seen, i_M can be generated based on the sum of absolute values of three-phase input currents. The illustrated switching parameters (i.e., m_0, m_1 and α_1) at both grid side and DC-link currents helps to better understand this relation. As it can be seen the period of the modulation signal i_M is 1/6 of the input currents i_{abc}. Therefore, the simplest way to generate and synchronize the modulation signal inside the controller is to compare it with a sinusoidal signal (i.e., $|\sin(3\omega_0 t)|$) using the phase locked loop (PLL) estimated angular frequency (ω_0). Comparing the switching angles with the sinusoidal waveform yields the following simple conditions [6]:

$$\alpha_1 < \alpha_2 : \begin{cases} if \left(|\sin(3\omega_0 t)| > \sin(3\beta) \right) \\ i_M = m_0 + m_1 \\ else \\ i_M = m_0 \end{cases}$$
$$\alpha_1 > \alpha_2 : \begin{cases} if \left(|\sin(3\omega_0 t)| > \sin(3\beta) \right) \\ i_M = m_0 - m_1 \\ else \\ i_M = m_0 \end{cases} \qquad (12)$$

To synchronize the current controller with the grid a Second-Order Generalized Integrator (SOGI) based PLL system is adopted [16]. As Fig. 7 depicted, for the simplicity, one line-to-line voltage is fed to the PLL and therefore the result will have 30° phase shift regarding to the phase voltage, which should be corrected within the reference current generator algorithm. In order to obtain a discrete-time integrator for PLL and PI controller, the trapezoidal discretization method is used.

The performance of the proposed harmonic reduction approach can be extended by increasing the number of pulses in the current modulation [6] and increasing the number of the parallel drives. Fig. 8(a) clearly shows that by adding two pulses to the current modulation technique with two drive units the THD$_i$ can be improved to 8.4% comparing with Fig. 6(b). Also the effect of increasing the number of the drives from two to three is shown Fig. 8(b). Here, even with adding only one pulse in the current modulation scheme the THD$_i$ can be reduced to 5.7%. Notably, in all these cases rectifiers draw equal amount of current from the grid according to (3).

Moreover, a suitable solution with high flexibility (i.e., application requirements) can be obtained through an optimization process as discussed in [3], [13], [17]. In other words, instead of fully nullifying the distortions, the harmonics could be reduced to acceptable levels by adding suitable constraints and defining suitable objective functions. It should be noted that, although increasing number of the paralleled-drives reduces the input current distortion but it reduces the power factor (λ). In fact, introducing higher number of drives with phase-shifted currents can adversely affect the displacement factor. Therefore, the power factor should be included in the optimization process in addition to the THD$_i$ when number of the parallel-connected drives increases.

V. EXPERIMENTAL RESULTS

In this section the performance of the multi-drive system is verified based on four different cases. Firstly, performance of the passive filtering technique is investigated. In cases two and three, the phase-shifted current control technique is tested using flat current modulation. In the final case, the performance of the system in terms of obtaining better power quality is examined applying the current modulation technique. Finally, in the last case the total input current
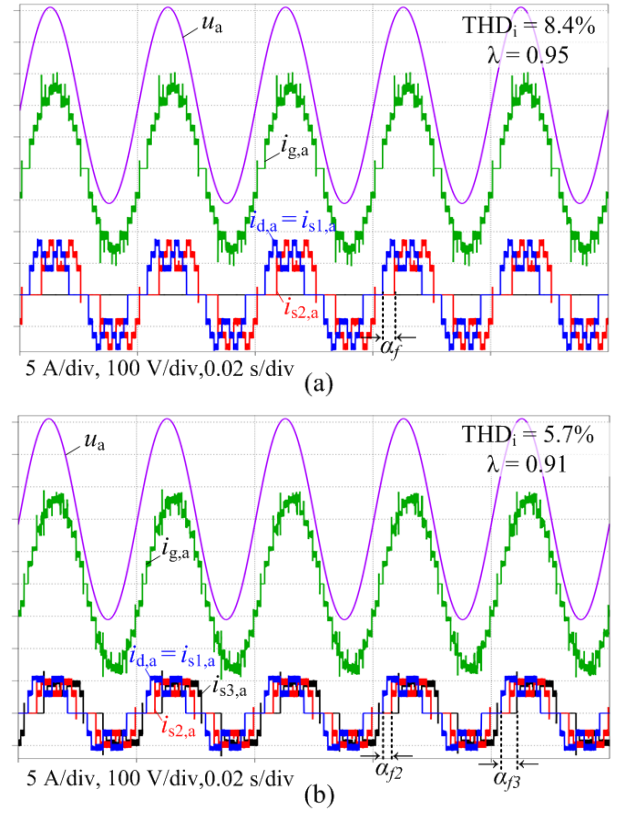
Fig. 8. Simulated waveforms for two different cases showing the flexibility of multi-drive system in harmonic reduction (using Table I parameters): (a) improving the input current quality by increasing number of pulses in current modulation scheme with two drives, (b) performance of the system in harmonic reduction when number of the drives is increased to three.

quality is further improved by increasing number of pulses in the current modulation scheme.

Fig. 9 illustrates the schematic and a photograph of the implemented hardware setup. Experimental results have been carried out on a 6 kW multi-drive system, which consists of two rectifier units (i.e., one DR as the first unit and one SCR as the second unit). As Fig. 9(a) shows, the first rectifier unit (DR) is connected to an Induction Motor (IM) through a 7.5 kW Danfoss Inverter, while the second rectifier (SCR) is connected to a resistive load (R_L). In practice, to avoid SCR
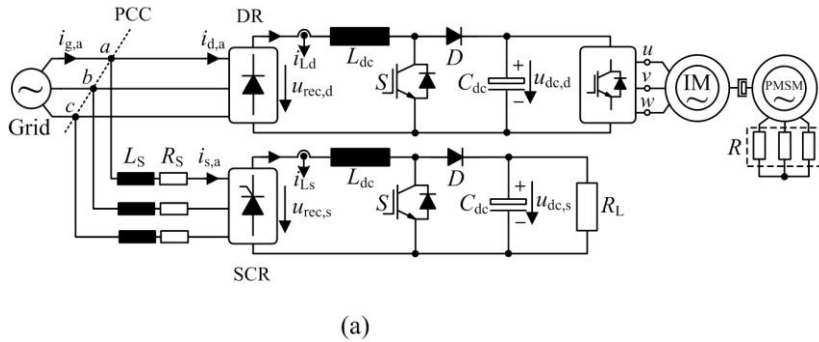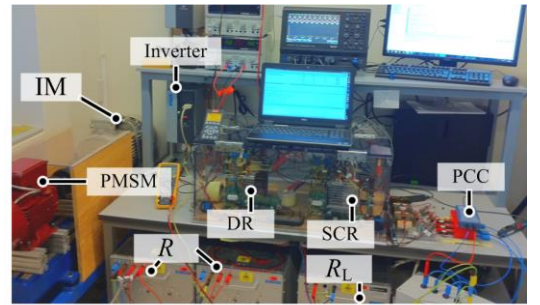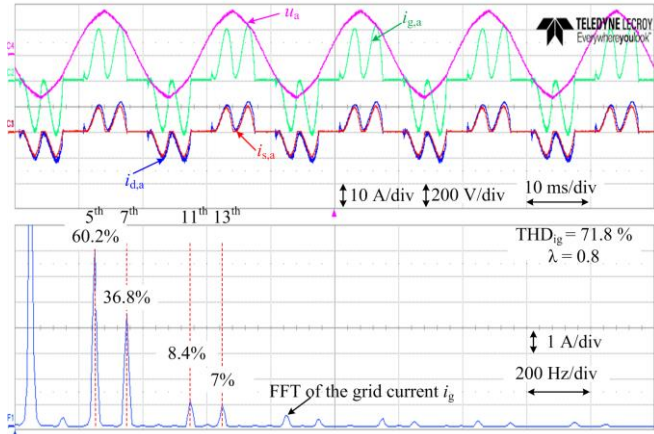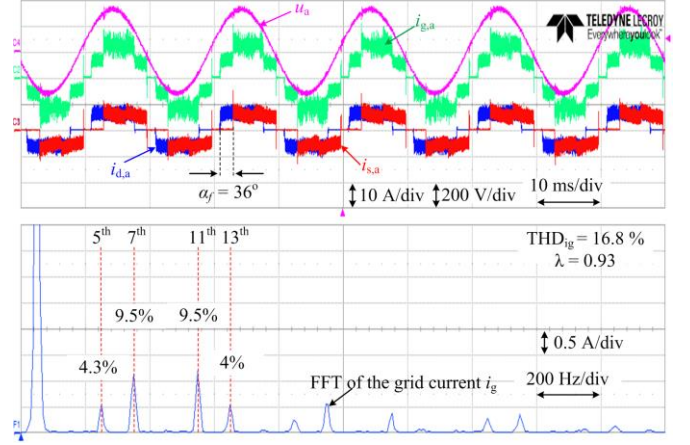
Fig. 9. Implemented multi-drive system with two rectifier units (i.e., one DR as the first unit and one SCR as the second unit): (a) system layout and (b) photograph of the hardware setup.

TABLE I. PARAMETERS OF THE MULTI-RECTIFIER SYSTEM

Parameter	Symbol	Value
Grid phase voltage and frequency	$u_{g,abc}, f_g$	230Vrms, 50Hz
dc-link output voltage	$U_{dc,d}, U_{dc,s}$	700 V dc
Total output power	$P_{o,s} + P_{o,d}$	$\approx$ 6 kW
DC-link inductor	L_{dc}	1.8 mH
DC-link Capacitor	C_{dc}	470 μF
Snubber (RC) across thyristor		100 Ω - 0.1 μF
SCR input filter	L_s, R_s	0.18 mH, 0.1 Ω

TABLE II. EMPLOYED MODULES IN THE PROTOTYPES

Module	Part-Number	Qty
Three-phase diode rectifier	SKD30	1
Three-phase SCR	SKKT 106/16	3
IGBT-diode	SK60GAL125	2
SCR triggering circuit	RT380T	1
Current measurement	HX-15	2
Voltage measurement	LV25-P	4
Controller	TMS320F28335	2

Fig. 11. Experimental results (phase a) of the multi-drive system applying phase-shifted current control with flat current modulation at $\alpha_f = 36^o$, $U_{dc,d/s} = 700$ V, $P_{ototal} \approx 6$kW, Torque = 29 N.m, RPM = 870 with Fast Fourier Transform (FFT) analysis of the grid current.

Fig. 10. Experimental results (phase a) **with passive filtering** for the multi-drive systems at $U_{dc} = 540$ V, $P_{ototal} \approx 6$kW, Torque = 29 N.m, RPM = 870 with Fast Fourier Transform (FFT) analysis of the grid current.
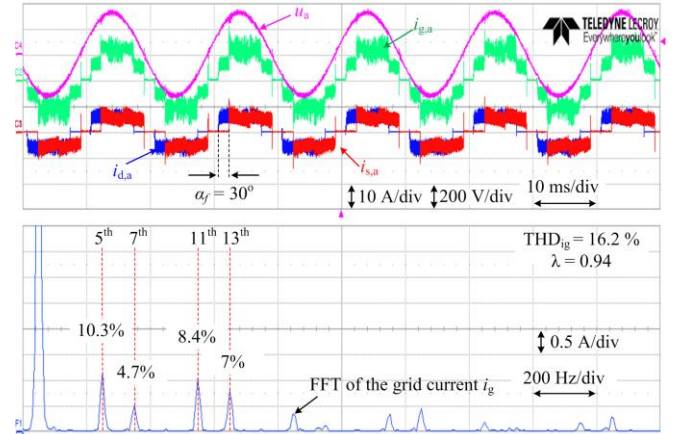
Fig. 12. Experimental results (phase a) of the multi-drive system applying phase-shifted current control with flat current modulation at $\alpha_f = 30^o$, $U_{dc,d/s} = 700$ V, $P_{ototal} \approx 6$kW, Torque = 29 N.m, RPM = 870 with Fast Fourier Transform (FFT) analysis of the grid current.

unit failure and to reduce the overvoltage to a reasonable limit, an RC snubber branch is connected across each thyristor. However, the presence of the snubber branches in the SCR unit causes current spikes in the SCR current (e.g., $i_{s,abc}$) at the point of commutation. In order to damp the current spikes, small inductors (i.e., L_s and R_s) are placed in series at AC-side of the SCR unit. Table I and Table II summarize the employed parameters and modules in the implemented system.

Firstly, the performance of the two-rectifier system when the DC-DC converter is in OFF-state (i.e., L_{dc} performs as a dc-side passive filter) is presented in Fig. 10. As it can be seen, the total input current harmonic distortion (i.e., $THD_{ig,a}$) of 71.8% with $\lambda = 0.8$ have been obtained. As it has been mentioned in Fig. 3, operating at lower power levels further reduces the input current quality.

Fig. 11 shows the effect of applying phase-shifted current control strategy with a flat current modulation where the THD of the grid current is improved to 16.8% with $\lambda = 0.93$. Here,

the firing angle for the SCR unit is set to 36° for 5th harmonic elimination (i.e., $5\times36^o = 180^o$). It can be seen that a relatively low 5th-order (i.e., 4.3% of the fundamental) is achieved. The reason that the 5th harmonic has not fully cancelled out is mainly due to the effect of the grid impedance which slightly changes the applied phase-shift. In order to obtain the lowest THD_{ig}, as it is depicted in Fig. 5(b), the firing angle should be set to 30°. The measured results presented in Fig. 12 verifies the lower distortion of the grid input current (i.e. $THD_{ig,a} = 16.2\%$) with $\lambda = 0.94$. Notably, as a smaller firing angle is applied comparing with the previous case the power factor (λ) is improved to 0.94.

In order to further reduce the THD_i, multi-pulse current modulation scheme is applied. Here, only one additional level is added to DC-link current and the modulation parameters are optimized in order to minimize the THD_i. The obtained results are illustrated in Fig. 13 which the total input current quality has been significantly improved by reducing the THD_i down
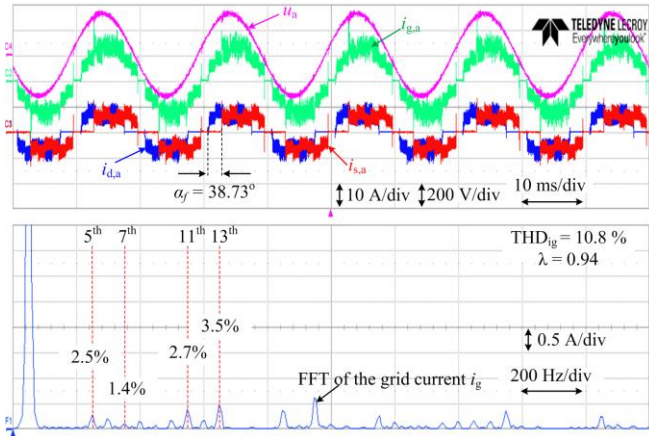
Fig. 13. Experimental results (phase a) of the multi-drive system applying phase-shifted current control with flat current modulation $U_{dc,d/s}$ = 700 V, $P_{ototal} \approx$ 6kW, Torque = 29 N.m, RPM = 870 with Fast Fourier Transform (FFT) analysis of the grid current [with m_0 = 1, $m_1 = m_2$ = 0.4902, α_f = 38.73°].

to 10.8% with λ = 0.94. As it can be seen, comparing with the flat current modulation the first three low harmonics orders of 5th, 7th and 11th haven been reduced below 3% of the fundamental current. This is in a close agreement with the simulation results presented in Fig. 6(b). Notably, even with larger firing angle of 38.73° is applied for the current modulation scheme the power factor is maintained at 0.94. This is due to the significant reduction of the distortion factor.

VI. CONCLUSIONS

In this paper simple and effective solutions in improving the power quality in ASD applications are addressed. The introduced EI solution at single-drive systems can effectively meet the required performance independent of the partial loading conditions. Moreover, improving the input current quality applying the EI technique in multi-drive configuration with phase-shifted current control has been analyzed. Finally, the effect of multi-pulse current modulation in conjunction with phase-shifted current control is addressed which substantially reduces input current harmonics. The experimental results validated the effectiveness of the proposed solutions.

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