Virtual-Impedance-Based Fault Current Limiters for Inverter Dominated AC Microgrids

Lu, Xiaonan; Wang, Jianhui; Guerrero, Josep M.; Zhao, Dongbo

Published in:
IEEE Transactions on Smart Grid

DOI (link to publication from Publisher):
10.1109/TSG.2016.2594811

Publication date:
2018

Document Version
Early version, also known as pre-print

Link to publication from Aalborg University

Citation for published version (APA):
Virtual Impedance Based Fault Current Limiters for Inverter Dominated AC Microgrids

Xiaonan Lu, Member, IEEE, Jianhui Wang, Senior Member, IEEE, Josep M. Guerrero, Fellow, IEEE, and Dongbo Zhao, Senior Member, IEEE

Abstract—In this paper, a virtual impedance based fault current limiter (VI-FCL) is proposed for islanded microgrids comprised of multiple inverter interfaced distributed generators (DGs). Considering the increased fault current capability induced by high penetration of renewable energy sources (RESs), FCLs are employed to suppress the fault current and the subsequent oscillation and even instability in the modern distribution network with microgrids. In this study, rather than involving extra hardware equipment, the functionality of FCL is achieved in the control diagram of DG inverters by employing additional virtual impedance control loops. The proposed VI-FCL features flexible and low-cost implementation and can effectively suppress the fault current and the oscillation in the following fault restoration process in AC microgrids. The systematic model of the inverter dominated AC microgrid is derived, and the stability analysis in consideration of VI-FCLs is thereby studied. MATLAB/Simulink model comprised of three inverter-interfaced DGs is implemented to verify the feasibility of the proposed method.

Index Terms—AC microgrid, distributed generation, fault current limiter, interface inverter, virtual impedance

I. INTRODUCTION

The increasing penetration of renewable energy sources (RESs) has significantly challenged the modern distribution systems in terms of bidirectional power flow in active distribution network [1], stochastic and intermittent power generation [2], different fault current capability [3], etc. In order to effectively control and manage the distributed generators (DGs), the concept of microgrid was proposed years ago to aggregate distributed sources and loads [4]. By employing the proper design and control algorithm, a microgrid can be used to enhance the reliability of distributed generation networks and reduce the operation cost. Meanwhile, by integrating microgrid controller with distribution management system (DMS), the functionality of microgrid can be further extended.

In order to improve the controllability of RESs and ensure the required power quality, power electronic inverters are widely employed as the interfaces [5]. Considering the distributed configuration of DGs, the interface inverters are usually connected in parallel [6]. A general configuration of AC microgrids is depicted in Fig. 1. It should be noted that the proper power sharing among different interface inverters should be achieved to avoid the unnecessary power circulation and the additional power loss. Different control strategies are proposed to realize the proper active and reactive power sharing, e.g. master-slave control [7], circular-chain-control (CC) [8], average current control [9], etc. It should be noticed that the above power sharing methods and their variants are realized based on dedicated high bandwidth communication network, which is less applicable for microgrids considering its distributed nature. Droop control and its modified versions are widely employed in microgrids [10]–[13]. Since it relies on only local information, a decentralized control diagram can be reached. Hence, it is more suitable for power sharing in microgrids compared to the communication-based methods. In order to fulfill the multiple requirements in microgrid operation and implement a systematic control algorithm, a hierarchical control diagram is proposed in [14], including the control objectives of local power sharing, voltage frequency and amplitude restoration, and active and reactive power control when interacting with external utility grid. The lower control layer of the hierarchical control diagram is reached based on decentralized control method, and the higher control layers are implemented based on low bandwidth communication links.

Fault protection schemes should be designed properly to ensure the safe and reliable operation of microgrids. In consideration of DG participation, the protection strategies of microgrids are more complicated than conventional passive distribution systems. The DGs may lead to missing operation or sympathetic tripping of the protective devices (PDs) during fault conditions. Meanwhile, since the fault current inside a microgrid is synthesized by the upstream utility grid and DG branches, the related relay settings for conventional distribution systems should be modified accordingly [3]. Especially for inverter dominated microgrids, the inertia of inverter-interfaced DGs is lower compared to the rotation-based DGs, e.g. small hydro, diesel generator, etc., and the
fault current limits are reduced due to the inverter power rating.

Various strategies are proposed to improve the protection schemes for inverter dominated microgrids. In [15], the amplitude of the inverter output current is calculated to detect the fault, and it is constrained to the maximum value during fault condition. For fault restoration, the post- and pre-fault values of the output current are compared to identify if significant change is entailed in the microgrid. In [16], the voltage magnitude regulation scheme and phase lock loop (PLL) are modified to enhance the performance during faults, and a phase angle restoration loop is employed to improve the fault ride through capability of the inverter interfaces and improve the process of post-fault recovery. In [17], the fault responses of AC microgrids with single inverter and multiple inverters are discussed, and the positive sequence equivalent P&Q model and current source model are derived for analyzing the operation of the interface inverter during faults. In [18], a fault current alleviation method is accomplished by measuring the remote voltage signal of the point of common coupling (PCC). By comparing the local output voltage and PCC voltage, the difference between the amplitudes and the phase angles are minimized to reduce the fault current. In [19], the protection strategy is implemented by using digital relays with communication capability. The failures of hardware devices and communication links are taken into account in the hierarchy of protection scheme. In [3], a multi-layer protection diagram is proposed, including load-way level, loop level, loop-feeder level and microgrid level, which is suitable for different microgrid configurations.

In order to mitigate the influence of fault current in microgrids, fault current limiters (FCLs) are studied and developed. The FCLs behave as rather low impedances in microgrids in the normal operation, while during faults, it becomes a large impedance and limit the amount of fault current. Hence, the uninterrupted operation of electrical systems can be obtained. Two types of technologies for FCLs currently exist, i.e., high temperature superconducting (HTS)-based FCL and solid-state circuit (SSC)-based FCL [20]. For HTS-based FCL, the characteristic of superconductor is utilized to change the impedance. For SSC-based FCL, it is essentially an additional power electronic converter series-connected in the power cable. The discussion of FCLs is found in existing literature. In [21], the functionality of dynamic voltage restorer (DVR) is extended to implement a SSC-based FCL and alleviate the impact of downstream fault current. In [22] and [23], additional inverters are series-connected to the feeder impedance to form a SSC-based FCL and emulate resistive or inductive impedance during faults. In [24], a unidirectional FCL is developed and placed between downstream microgrid and upstream utility grid to cope with the downstream faults. In [25] and [26], the optimal positioning of HTS-based FCLs is discussed. Especially in [26], the location of FCLs in hybrid AC and DC microgrids is studied to ensure the effective suppression of fault current. In [27], HTS-based FCL is employed to protect the key energy storage units in the system. In [28], a constrained nonlinear programming problem is formulated to optimally select the relay settings and size FCLs.

Virtual impedance as a cost-effective and flexible approach has been employed in the control diagram of microgrids in the past years. It can be used to match the output impedance of each interface inverter and decouple the active and reactive power sharing in droop-controlled microgrids [29], [30]. Meanwhile, a virtual impedance can also be used to dampen the resonance peaks in LCL-filtered inverters to increase the stability margin [31], or emulate required damping impedance at different harmonic frequencies so that the certain harmonic components can be eliminated [32].

In this paper, a virtual impedance based FCL (VI-FCL) is proposed to suppress the fault current in islanded AC microgrids. Since three-phase faults have the highest impact on system operation, the proposed method is mainly designed for alleviating the influence of symmetrical three-phase faults. For asymmetrical faults, similar approaches can be developed by implementing VI-FCLs in positive and negative sequences, respectively. Compared to the existing methods of implementing FCLs, the VI-FCL features lower capital and maintenance costs. No extra superconducting devices or inverters are required to work as FCLs. The existing current controller in the primary control level of a DG unit does not work for limiting the fault current considering controller saturation, huge amount of fault current and low voltage at the fault location. By involving additional virtual impedance loops in the DG interface inverters, large output impedances can be implemented during faults to emulate the physical inductance and resistance in the real FCLs. Meanwhile, in normal operation, the VI-FCLs keep zero to avoid unnecessary voltage drops. Furthermore, it should be noted that by using the proposed VI-FCL, the fault ride through capability of DG unit can be enhanced. Hence, they do not need to be cut off although the fault occurs. Compared to the conventional current/voltage based protection schemes, the proposed method does not interrupt the DG operation, so the complicated resynchronization algorithm for DG reconnection can be avoided. The principle and implementation of the proposed VI-FCL is introduced in this study. Meanwhile, a systematic model of inverter dominated AC microgrids during faults is derived, and the stability analysis of the overall system is thereby analyzed. A MATLAB/Simulink model comprised of three interface inverters is implemented to verify the effectiveness of the proposed VI-FCL. Meanwhile, real-time hardware-in-the-loop (HIL) test based on OPAL-RT platform is also conducted to further verify the feasibility of the proposed method.

The following paper is organized as follows. Section II introduces the principle and implementation of VI-FCL. Section III analyzes the model of AC microgrids during faults and conduct the stability analysis of the overall control diagram with VI-FCLs. Section IV shows the simulation results for different cases. Finally, Section V summarizes the paper and draws the conclusion.
II. PRINCIPLE AND IMPLEMENTATION OF VI-FCLS

A. Principle of VI-FCL

The simplified configuration of AC microgrids dominated by multiple interface inverters is shown in Fig. 2. Each inverter interfaced DG unit is modeled by using a voltage source and two virtual impedances. The reference value of the voltage source is calculated by droop control method [14]. In particular, the reference values of the voltage frequency and amplitude are generated as follows:

\[ f_i = f^* - m P_{oi} \]
\[ E_i = E^* - n Q_{oi} \]

where \( f_i \) and \( E_i \) are the voltage frequency and amplitude, \( f^* \) and \( E^* \) are their reference values, \( m \) and \( n \) are the droop coefficients, and \( P_{oi} \) and \( Q_{oi} \) are the output active and reactive power, \( i = 1, 2, \ldots, n \).

Note that the frequency and amplitude deviation of the local output voltage should be limited within the acceptable range, namely

\[ |f^* - f| \leq \Delta f_{\text{max}} \]
\[ |E^* - E_i| \leq \Delta E_{\text{max}} \]

where \( \Delta f_{\text{max}} \) and \( \Delta E_{\text{max}} \) are the maximum acceptable deviation of the frequency and amplitude.

\[ Z_{\text{fcl}1} = \begin{cases} 0 & I < I_{th} \\ |Z_{\text{fcl}1}|_{\text{max}} [1 - e^{-|t-t_{\text{span}}|/\tau}] & I \geq I_{th} \end{cases} \]

Fig. 2. Configuration of AC microgrids dominated by multiple interface inverters.

The two virtual impedances in the equivalent model of the inverter interfaced DG unit are represented by \( Z_{\text{fcl}1} \) and \( Z_{\text{fcl}2} \), respectively. Here, \( Z_{\text{fcl}} \) is used to decouple the active and reactive power sharing and ensure the droop relationship shown in (1) and (2) [29], [30], and \( Z_{\text{fcl}} \) is involved to represent the VI-FCL, which is activated only during faults and keeps zero in normal operation. The amplitude of \( Z_{\text{fcl}} \) is calculated as:

\[ |Z_{\text{fcl}}| = \begin{cases} 0 & I < I_{th} \\ |Z_{\text{fcl}}|_{\text{max}} [1 - e^{-|t-t_{\text{span}}|/\tau}] & I \geq I_{th} \end{cases} \]

where \( |Z_{\text{fcl}}|_{\text{max}} \) is the maximum amplitude of the virtual impedance that is determined by considering the acceptable fault current level, \( t_{th} \) is the time when the measured peak current exceeds the threshold, and \( t_{\text{span}} \) is the transient time for the amplitude of the virtual impedance changing from 0 to the maximum value, \( I \) is the peak value of the current, and \( I_{th} \) is the current threshold of triggering the FCLs.

Based on the above definition, the overall control diagram is shown in Fig. 3, and the flow chart of the working principle of VI-FCL is shown in Fig. 4. In the control diagram in Fig. 3, proportional-resonant (PR) controllers are used in the inner voltage and current control loops [30], which can be shown as:

\[ G_i = k_p + k_r \cdot \frac{s}{s + \omega} \]

\[ G_i = k_p + k_r \cdot \frac{s}{s + \omega} \]

where \( G_v \) and \( G_c \) are the transfer functions of the inner voltage and current controllers, \( k_p \) and \( k_r \) are the coefficients of the proportional and resonant terms in \( G_v \), \( k_p \) and \( k_r \) are the coefficients of the proportional and resonant terms in \( G_c \), \( \omega \) is the angular frequency, \( s \) is the Laplace operator.

Meanwhile, it should be noted that secondary control is employed to eliminate the deviations of frequency and amplitude in normal operation. By using secondary frequency and voltage amplitude control, two compensation terms related to the phase angle \( \Phi \) and voltage amplitude \( E \), i.e., \( \delta \Phi \) and \( \delta E \), are generated and added to the voltage reference. The fault is detected when the peak value of output current reaches its threshold, and the secondary control is deactivated while the VI-FCL is activated. Then, the amplitude of \( Z_{\text{fcl}} \) reaches its maximum value to alleviate the amount of fault current. When the peak value of output current falls below its threshold, the VI-FCL is deactivated to avoid unnecessary voltage drop, and the secondary control is reactivated to restore the voltage frequency and amplitude. Here, deactivating secondary control refers to resetting the proportional-integral (PI) controllers in the secondary control level and stop adding the compensation terms, i.e., \( \delta \Phi \) and \( \delta E \), into the voltage reference.

It can be seen that the VI-FCL, i.e., \( Z_{\text{fcl}1} \), is only activated during fault conditions. However, as aforementioned, when the fault occurs, secondary control should be deactivated. The reason for deactivating secondary control during faults is that the voltage is forced to drop down due to the existence of fault impedance and this voltage drop is inevitable. Since secondary control is used to restore the voltage, it conflicts with voltage drop induced by the faults. Hence, it should be deactivated to avoid the unstable operation of the control diagram.
B. Design and Implementation of VI-FCL

In order to properly design the VI-FCL, as shown in Fig. 5, the representative system is employed, where the $\tilde{Z}_i$, $\tilde{Z}_g$, $\tilde{Z}_{cl}$ and $\tilde{Z}_v$ represent the vectors of line impedance, virtual impedance $Z_v$, VI-FCL $Z_{cl}$ and the ground impedance at the fault location, respectively, and $Z_{cl}$ is only activated during faults. The impedances $\tilde{Z}_i$, $\tilde{Z}_g$ and $\tilde{Z}_{cl}$ can be written as:

$$\begin{align*}
\tilde{Z}_i &= |\tilde{Z}_i| \angle \theta_i \\
\tilde{Z}_g &= |\tilde{Z}_g| \angle \theta_g \\
\tilde{Z}_{cl} &= |\tilde{Z}_{cl}| \angle \theta_{cl}
\end{align*}$$

where $\theta_i$, $\theta_g$ and $\theta_{cl}$ are the phase angles of the corresponding impedances.

In order to simplify the analysis and avoid the potential instability issue, $\tilde{Z}_{cl}$ is selected to be in phase with $\tilde{Z}_v$. Therefore, it is achieved that:

$$\begin{align*}
\theta_{cl} &= \theta_v \\
|\tilde{Z}_{cl}| &= |k| |\tilde{Z}_v|
\end{align*}$$

where $k$ represents the ratio between $|\tilde{Z}_{cl}|$ and $|\tilde{Z}_v|$.

As shown in [29]-[30], the virtual impedance $Z_v$ is used to ensure that the active and reactive power sharing follows the drop control expression shown in (1) and (2) in normal condition. In order to meet this requirement, $Z_v$ should be significantly inductive. To quantitatively identify the required $|\tilde{Z}_v|$ and $\theta_v$, the phasor diagram of the impedances as shown in Fig. 6 are employed. It is defined that:

$$Z_{eq} = Z_l + \tilde{Z_v}$$

Hence, in order to guarantee that the equivalent line impedance $Z_{eq}$ in normal condition is significantly inductive, the phase angle of $Z_{eq}$, i.e., $\theta_{eq}$, should be almost 90°. Namely,

$$90° - \theta_{eq} \leq \theta_{eqm}$$

where $\theta_{eqm}$ is the maximum acceptable phase difference, which is selected as 2° here.

By using the cosine law in the triangle $\Delta OBC$, it is derived that:

$$|\tilde{Z}_{eq}| = \sqrt{|\tilde{Z}_l|^2 + |\tilde{Z}_v|^2 - 2|\tilde{Z}_l||\tilde{Z}_v| \cos(90° - \theta_v + \alpha)}$$

Meanwhile, by using the sine law in the same triangle, it yields that:

$$\alpha = \arcsin \left( \frac{|\tilde{Z}_l|}{|\tilde{Z}_{eq}|} \sin(\theta_v - \theta_l) \right)$$

where $\alpha = \angle COB$.

Hence, it can be derived that:

$$\theta_{eq} = \alpha + \theta_l$$

For a given system, $|\tilde{Z}_l|$ and $\theta_l$ are commonly vary within a certain range that is determined by the practical condition of the DG branch. The selection of $|\tilde{Z}_v|$ and $\theta_v$ should make sure that for arbitrary $|\tilde{Z}_l|$ and $\theta_l$ within their ranges, the equivalent line impedance $Z_{eq}$ should be significantly inductive, i.e., the criteria established by combining (11) – (14) should be satisfied. In the given system, assuming that $|\tilde{Z}_l|$ varies within the range of 0.5 ~ 1 Ω and $\theta_l$ varies within the range of 80° ~ 87.5°, by using MATLAB m-script to search the suitable $|\tilde{Z}_v|$ and $\theta_v$, it can be reached that:

$$|\tilde{Z}_v| = 1.40 \Omega$$

$$\theta_v = 89°$$

Note that some more choices of $|\tilde{Z}_v|$ that is larger than 1.40 Ω can be selected to meet the criteria established by (11) – (14). Since larger $|\tilde{Z}_v|$ reduces the output voltage in normal condition, the smallest $|\tilde{Z}_v|$ that fulfills the criteria is selected.
After designing $|\bar{Z}|$ and $\theta_c$, as mentioned in (9), it is achieved that:

$$\theta_{cl} = \theta_c = 89^\circ$$  \hspace{1cm} (16)

Therefore, the next step for the design procedure is to select the suitable $k$ so that the vector $\bar{Z}_{cl}$ can be determined.

As shown in the representative system in Fig. 5, in case of a fault occurring at the DG branch, a parameter $\lambda$ is employed to indicate the fault location. It is defined as:

$$\lambda = \left| \frac{\bar{Z}_a}{\bar{Z}_a + \bar{Z}_b} \right|$$

where $\bar{Z}_a$ is the part of the line impedance near the DG unit, while $\bar{Z}_b$ is the part of the line impedance near the PCC, and $\bar{Z}_a + \bar{Z}_b = \bar{Z}$. The smaller $\lambda$ indicates that the fault is near the DG terminal, while the larger $\lambda$ indicates the fault is near the PCC.

The variable $k$ should be determined by limiting the maximum $|\dot{I}_o|$ lower than $|\dot{I}_{o\text{max}}|$. As shown in Fig. 5, when the fault occurs, the voltage at the fault location can be regarded as almost zero. Hence, it can be calculated that:

$$|\dot{I}_o| = \left| \dot{V}_{\text{ref}} \right| \leq |\dot{I}_{o\text{max}}|$$

(18)

Assuming that the phase angle of $\dot{V}_{\text{ref}}$ is zero and $|\dot{V}_{\text{ref}}| = 110$ V, (18) should be satisfied with arbitrary line impedances and fault locations. In other words, for the given system, (18) should be fulfilled with arbitrary $|\bar{Z}|$ within the range of $0.5 \sim 1$ Ω, arbitrary $\theta_c$ within the range of $80^\circ \sim 87.5^\circ$, and arbitrary $\lambda$ within the range of 0 ~ 1.

Similar to the design procedure of $|\bar{Z}|$ and $\theta_c$, the suitable value of the variable $k$ can be searched by using MATLAB m-script. Here, it is obtained that $k$ equals 4.

Note that larger $k$ can be also selected to meet the requirement in (18). In order to avoid the unnecessary voltage deviation during faults, the minimum $k$ that satisfies (18) is selected here.

Hence, by summarizing the above results, it yields:

$$\bar{Z}_{cl} = |\bar{Z}_{cl}| \angle \theta_{cl} = k |\bar{Z}| \angle \theta_c = 4 \times 1.4 \angle 89^\circ = 5.6 \angle 89^\circ$$  \hspace{1cm} (19)

It should be noticed that for multiple inverters in an AC microgrid, the VI-FCL for each interface inverter should be designed individually based on the practical line impedance $\bar{Z}_l$ and the virtual impedance $\bar{Z}_v$.

III. MODELING AND ANALYSIS OF AC MICROGRIDS WITH VI-FCLs

A. Modeling of AC Microgrids with VI-FCLs during Faults

In order to analyze the effectiveness of VI-FCLs, the model of AC microgrids during faults is analyzed as follows. Take an AC microgrid with three DGs as an example. The impedance model of AC microgrids during faults is shown in Fig. 7, where $\bar{Z}_{load}$ is the load impedance and $\bar{Z}_g$ is the ground impedance of the fault. It is assumed that the fault occurs at the branch of DG #1.

For each DG interface inverter, the configuration of the main power circuit and the corresponding control diagram are shown in Fig. 8 (a) and (b). It can be derived based on the control diagram in Fig. 8 (b) that:

$$v_{ci} = \frac{G_{ci} G_{d} G_{cap i}}{G_{ci} G_{d} + G_{ind i} + (1 + G_{ci} G_{d} G_{cap i})} v_{rref} - \frac{G_{ci} G_{d} G_{cap i} (\bar{Z}_o + \bar{Z}_{cl}) + (G_{ci} G_{d} + G_{ind i} G_{cap i})}{G_{ci} G_{d} + G_{ind i} + (1 + G_{ci} G_{d} G_{cap i})} i_{ci}$$

(20)

where $G_{ci}$ and $G_{ci}$ are the inner voltage and current controllers, respectively, $G_{d}$ represents the PWM generation unit, $G_{cap i}$ is the transfer function of the inverter filter capacitor, $G_{ind i}$ is the transfer function of the inverter filter inductor, $v_{ci}$ and $i_{ci}$ are the output voltage and current of inverter #i, and $v_{rref}$ is the reference value of $v_{ci}$ (i = 1, 2, 3).

Fig. 5. Representative system for the design of VI-FCL.

Fig. 6. Phasor diagram of the impedances $\bar{Z}_l$ and $\bar{Z}_v$.

Fig. 7. Impedance model of the AC microgrid with VI-FCLs during faults.

Fig. 8. (a) Control diagram in Fig. 8 (b) that:
is the inverter filter capacitance, and respectively. The transfer functions of are the common PR voltage and current controllers, corresponding output voltage of each DG unit. Considering the sum of that variable in each case with single each output current or voltage can be calculated by procedure of PWM generation [33]. Meanwhile, in the transfer function interface inverter.

For simplification, (20) can be rewritten as:

\[
    v_{i} = G_{ref} \cdot v_{ref} - Z_{o} \cdot i_{o} \quad (i=1, 2, 3)
\]

where \( k_{pv} \) and \( k_{rv} \) are the proportional and resonant coefficients of the voltage PR controller, \( k_{pe} \) and \( k_{rci} \) are the proportional and resonant coefficients of the current PR controller, \( T_{o} \) is the delay induced by PWM generation and duty cycle updating, \( C_{i} \) is the inverter filter capacitance, and \( L_{i} \) is the inverter filter inductance.

For the given system in Table I [34], by defining that \( Z_{r} = R_{r} + s \cdot L_{r}, Z_{fc} = R_{fc} + s \cdot L_{fc}, Z_{load} = R_{load} + s \cdot L_{load}, Z_{g} = R_{g} + s \cdot L_{g} \), and using bilinear transformation of (22) \( (i = 1, 2, 3) \) in (28).

By using the same procedure, the output current of each DG branch can be reached, which can be summarized as:

\[
    \begin{bmatrix}
        i_{o1} \\
        i_{o2} \\
        i_{o3}
    \end{bmatrix} = \overline{Y} \cdot \begin{bmatrix}
        v_{o1} \\
        v_{o2} \\
        v_{o3}
    \end{bmatrix}
\]

where \( \overline{Y} \) is the coefficient matrix with elements \( Y_{ij} \) (i, j = 1, 2, 3). Combining (22) \( (i = 1, 2, 3) \) and (27), it is achieved that:

\[
    \begin{bmatrix}
        v_{o1} \\
        v_{o2} \\
        v_{o3}
    \end{bmatrix} = (1 + Z_{o} \overline{Y})^{-1} \overline{G}_{ref} \cdot \begin{bmatrix}
        v_{ref1} \\
        v_{ref2} \\
        v_{ref3}
    \end{bmatrix}
\]

where

\[
    Z_{o} = \begin{bmatrix}
        Z_{o1} & Z_{o2} & Z_{o3}
    \end{bmatrix}, \quad \overline{G}_{ref} = \begin{bmatrix}
        G_{ref1} \\
        G_{ref2} \\
        G_{ref3}
    \end{bmatrix}
\]

Hence, the stability of the system with VI-FCLs can be studied by analyzing the dominant poles of the transfer functions \( v_{oi}/v_{refi} \) \( (i = 1, 2, 3) \) in (28).

B. Stability Analysis of VI-FCLs

For the given system in Table I [34], by defining that \( Z_{r} = R_{r} + s \cdot L_{r}, Z_{fc} = R_{fc} + s \cdot L_{fc}, Z_{load} = R_{load} + s \cdot L_{load}, Z_{g} = R_{g} + s \cdot L_{g} \), and using bilinear transformation of (22) \( (i = 1, 2, 3) \) in (28).

When increasing the virtual inductance \( L_{fdl} \) from 50 mH to 80 mH and having \( R_{fc} = 97.6 \) mΩ, it can be seen in Fig. 9 (a) that the dominant pole of system moves towards the unstable region. When the dominant pole locates near the stability boundary (the unit circles in Fig. 9 (a)), e.g., \( p_{r1} = -0.92 + j 0 \), the system stability is challenged to be at risk. It should be noted that the poles locating on the right side of the figure are not the dominant poles since they are cancelled by the zeros. Similar situations exist for the z domain stability analysis in Fig. 9 (b) and (c). When increasing the virtual resistance \( R_{fdl} \) from 5 mΩ to 1 Ω and keeping \( L_{fdl} = 14.8 \) mH, it can be seen that three dominant poles move towards the stability boundary. As shown in Fig. 9 (b), the dominant poles are finally shown as \( p_{r1} = -0.69 + j 0 \) and \( p_{r2,3} = -0.60 \pm j 10.50 \). It should be noticed that the impact of \( p_{r1} \) and \( p_{r2,3} \) are less significant compared to the case with increasing virtual inductance \( L_{fdl} \) since their magnitudes are smaller than the dominant pole \( p_{r1} \) in Fig. 9 (a). Meanwhile, as aforementioned, a parameter \( \lambda \) is involved to indicate the fault location. When changing \( \lambda \) and keeping \( L_{fdl} = 14.8 \) mH and \( R_{fdl} = 97.6 \) mΩ, all the dominant poles statically locate in the stable region without a trend to orient the unstable boundary. Hence, the proposed VI-FCL method is valid for different fault locations.
### TABLE I

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f$</td>
<td>Rated voltage frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>$E^*$</td>
<td>Rated RMS voltage</td>
<td>110 V</td>
</tr>
<tr>
<td>$L_{11}$</td>
<td>Line inductance #1</td>
<td>2.5 mH</td>
</tr>
<tr>
<td>$R_{11}$</td>
<td>Line resistance #1</td>
<td>0.08 Ω</td>
</tr>
<tr>
<td>$L_{12}$</td>
<td>Line inductance #2</td>
<td>1.8 mH</td>
</tr>
<tr>
<td>$R_{12}$</td>
<td>Line resistance #2</td>
<td>0.03 Ω</td>
</tr>
<tr>
<td>$L_{13}$</td>
<td>Line inductance #3</td>
<td>1.8 mH</td>
</tr>
<tr>
<td>$R_{13}$</td>
<td>Line resistance #3</td>
<td>0.03 Ω</td>
</tr>
<tr>
<td>$L_{\text{load}}$</td>
<td>Load inductor</td>
<td>20 mH</td>
</tr>
<tr>
<td>$R_{\text{load}}$</td>
<td>Load resistor</td>
<td>0.4 Ω</td>
</tr>
<tr>
<td>$L_{g}$</td>
<td>Grounding inductance</td>
<td>0.03 mH</td>
</tr>
<tr>
<td>$R_{g}$</td>
<td>Grounding resistance</td>
<td>0.6 mΩ</td>
</tr>
<tr>
<td>$L_{\text{fcl}}$</td>
<td>Filter inductance of the inverter</td>
<td>1 mH</td>
</tr>
<tr>
<td>$C_{\text{fcl}}$</td>
<td>Filter capacitance of the inverter</td>
<td>47 μF</td>
</tr>
<tr>
<td>$k_{pv}$</td>
<td>Proportional coefficient of the voltage PR controller</td>
<td>0.6</td>
</tr>
<tr>
<td>$k_{rv}$</td>
<td>Resonant coefficient of the voltage PR controller</td>
<td>2</td>
</tr>
<tr>
<td>$k_{pc}$</td>
<td>Proportional coefficient of the current PR controller</td>
<td>1</td>
</tr>
<tr>
<td>$k_{rc}$</td>
<td>Resonant coefficient of the current PR controller</td>
<td>2</td>
</tr>
<tr>
<td>$M$</td>
<td>Droop coefficient for voltage frequency</td>
<td>0.0006 rad/(W·s)</td>
</tr>
<tr>
<td>$n$</td>
<td>Droop coefficient for voltage amplitude</td>
<td>0.02 V/Var</td>
</tr>
<tr>
<td>$k_{pfs}$</td>
<td>Proportional term of secondary frequency control</td>
<td>$3 \times 10^{-4}$</td>
</tr>
<tr>
<td>$k_{ifs}$</td>
<td>Integral term of secondary frequency control</td>
<td>1.4</td>
</tr>
<tr>
<td>$k_{ps}$</td>
<td>Proportional term of secondary voltage amplitude control</td>
<td>$2 \times 10^{-4}$</td>
</tr>
<tr>
<td>$k_{is}$</td>
<td>Integral term of secondary voltage amplitude control</td>
<td>4</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Switching frequency</td>
<td>10 kHz</td>
</tr>
<tr>
<td>$T_d$</td>
<td>PWM delay</td>
<td>100 μs</td>
</tr>
</tbody>
</table>

Fig. 9. Locations of the dominant poles in $z$ domain.
(a) $50 \, \text{nH} \leq L_{\text{fcl}} \leq 80 \, \text{mH}$, $R_{\text{fcl}} = 97.6 \, \text{mΩ}$. (b) $5 \, \text{mΩ} \leq R_{\text{fcl}} \leq 1 \, \Omega$, $L_{\text{fcl}} = 14.8 \, \text{mH}$. (c) $0.05 \leq \lambda \leq 0.95$, $L_{\text{fcl}} = 14.8 \, \text{mH}$ and $R_{\text{fcl}} = 97.6 \, \text{mΩ}$.

### IV. SIMULATION VALIDATIONS

In order to verify the proposed control diagram with VI-FCLs, a MATLAB/Simulink model comprised of three DGs is implemented. The system configuration is shown in Fig. 10 and the fault locations in different test cases are highlighted by using the circled numbers. Meanwhile, real-time HIL test is also conducted based on OPAL-RT platform. The system parameters are the same as those shown in Table I. It should be noted that the proposed method can be also used in practical applications. For practical implementation, the VI-FCL should be designed based on the real condition of power cable, acceptable fault current level, desired transient time for fault clearance, etc. Due to the present hardware limitations, only offline and real-time simulations are shown below for case studies.

**Case I: Different Values of VI-FCLs**

Different values of VI-FCLs are tested to study their impacts on fault current limiting and transient oscillation mitigation. As shown in Fig. 10, taking the fault at the PCC as an example, it occurs at $t = 36 \, \text{s}$ and lasts for $0.2 \, \text{s}$. The comparative study of different VI-FCLs is investigated in this test case. In the illustrative system, as shown in Table I, the length of the power cable for DG #2 and #3 is the same, while the length of the cable for DG #1 is longer. The waveforms of the RMS current for DG #1 and #2 and the system frequency are selected as examples.
shown in Fig. 12 (a) and (b), respectively. It can be seen that the waveforms of the RMS current of DG #1 and #2 are not employed. When activating the VI-FCLs, large oscillations are removed. Meanwhile, Δ_I_m is reduced from 1 Hz to 0.29 Hz and Δ_f_a is reduced from 13.6 s to 0.9 s.

For the case with the fault near the PCC, i.e., λ = 0.85, the waveforms of RMS current of DG #1 and #2 are shown in Fig. 13 (a) and (b), respectively. It can be seen that for the RMS current of DG #1, Δ_I_m is reduced from 7.95 A to 2.96 A and Δ_f_a is reduced from 11.0 s to 3.4 s. For the RMS current of DG #2, Δ_I_m is reduced from 5.82 A to 3.02 A and Δ_f_a is reduced from 5.2 s to 3.6 s. For the frequency waveform, as shown in Fig. 13 (c), Δ_f_m is reduced from 0.38 Hz to 0.22 Hz and Δ_f_a is reduced from 6.4 s to 1.2 s.

Meanwhile, compared to the results of the case with the fault near the DG unit shown in Fig. 12 (a) – (c), it can be found that the proposed VI-FCLs can be used to suppress the fault current and transient oscillations in various cases with different fault locations.

**Case III: Fault Occurs at the PCC**

As shown in Fig. 10, the fault occurs at the PCC is studied. The effectiveness of VI-FCL during fault and in the post-fault procedure is discussed in detail in this test case. As same as Case I and II, the fault occurs at t = 36 s and lasts for 0.2 s. As shown in Fig. 14 (a), for DG branch #1, Δ_I_m changes from 5.36 A to 1.16 A if activating the VI-FCLs, and Δ_f_a is reduced from 10.4 s to 6.1 s. Meanwhile, for DG branch #2, as shown in Fig. 14 (b), Δ_I_m changes from 11.7 A to 4 A, and Δ_f_a reduces from 5.3 s to 4 s with VI-FCLs. It should be noted that the differences in the current and frequency waveforms for DG branch #1 and #2 are caused by different lengths of the power cables. For the frequency waveforms, as shown in Fig. 14 (c), large oscillations can be found without VI-FCLs. If activating the VI-FCLs, Δ_f_m is reduced from 0.33 Hz to 0.21 Hz, and the transient time Δ_f_a is reduced from 6.5 s to 1.4 s.

**Case IV: Multiple Fault Locations**

As shown in Fig. 10, the system responses when multiple faults occur at different locations are shown in this case study. It is set that the faults occur at DG branch #1 and DG branch #2 simultaneously at t = 36 s and lasts for 0.2 s. In order to diversify the fault locations, the fault at DG branch #1 occurs near the DG unit, while the fault at DG branch #2 occurs near the PCC. As shown in Fig. 15 (a), for DG branch #1, Δ_I_m changes from 30.9 A to 9.3 A with VI-FCLs activated, and Δ_f_a is reduced from 15.6 s to 4.7 s. Meanwhile, for DG branch #2, as shown in Fig. 15 (b), Δ_I_m is reduced from 25.3 A to 7.1 A, and Δ_f_a reduces from 10.6 s to 3.8 s with VI-FCLs. For the system frequency, as shown in Fig. 15 (c), when activating the VI-FCLs, Δ_f_m is reduced from 0.94 Hz to 0.53 Hz, and the transient time Δ_f_a is reduced from 13.8 s to 3.6 s.

**Case V: Continuously Variable Load**

The feasibility of the proposed method with continuously variable load is tested in this case study. In particular, the conventional impedance load is replaced by the variable load. The load current continuously changes during the whole simulation procedure, as shown in the current profile of the common load in normal condition in Fig. 16 (a). Meanwhile, as shown in Fig. 10, it is set that the fault at the DG branch #1 occurs at t = 36 s and lasts for 0.2 s. As
shown in Fig. 16 (b) – (d), when the fault occurs, compared to the value in normal condition, the maximum deviation of $I_{\text{rms}1}$ is 52.5 A without VI-FCL, which is reduced to 16.4 A when the VI-FCL is activated. For DG branch #2, also compared to the value in normal condition, the maximum deviation of $I_{\text{rms}2}$ is reduced from 15.6 A to 4.6 A with VI-FCL activated during the fault. At the same time, the maximum deviation of system frequency is reduced from 2.7 Hz to 2.0 Hz. It should be noted that since the load is continuously changed, the transient response time, i.e., $\Delta t_{\text{sf}}$ and $\Delta t_{\text{so}}$, is not calculated. It can be also seen from Fig. 16 (d) that when VI-FCL is employed, the post-fault procedure is significantly improved with much lower oscillations.

**Case VI: Rotating Machine Load**

It should be pointed out that the proposed VI-FCL works with not only impedance load but also the other types of load. In this case study, a rotating machine load is employed as an example to test the feasibility of the proposed method in suppressing the amount of fault current. In particular, a three-phase asynchronous machine is used as the common load. The rated voltage and frequency are 110 V (rms) and 60 Hz, respectively. As shown in Fig. 10, it is set that the fault occurs at DG branch #1 near the DG unit at $t = 36$ s and lasts for 0.2 s.

It can be seen from Fig. 17 (a) that the maximum deviation of the torque $\Delta T_m$ is reduced from 15.6 Nm to 4.6 Nm when activating VI-FCL. Meanwhile, the transient time $\Delta t_{\text{sf}}$ w/o VI-FCL is similar, which is approximately 0.6 s. For the rotor speed, as shown in Fig. 17 (b), its maximum deviation $\Delta \omega_m$ is reduced from 9.6 rad/s to 2.6 rad/s when activating VI-FCL, and the transient time $\Delta t_{\text{so}}$ is reduced from 3.6 s to 1.7 s. Hence, it can be seen that the proposed method works for rotating machine load.

**Case VII: Comparison with Conventional Current/Voltage Based Protection Schemes**

Conventional protection schemes can be generally implemented by detecting the abnormal current or voltage. In order to identify the merits of the proposed VI-FCL based method, traditional current/voltage based protection schemes are implemented in this case study for comparison.

As shown in Fig. 10, it is set that the fault occurs at DG branch #1 near the DG unit at $t = 36$ s and lasts for 0.2 s. The responses with the conventional protection scheme based on current detection is shown in Fig. 18 (a) – (c). It can be seen that when $I_{\text{rms}1}$ reaches its over-current threshold, the protective relay is activated to cut off the fault and the interface inverter for DG #1 stops working. Hence, $V_{\text{rms}1}$ reduces to zero. Meanwhile, since the fault is isolated, the system returns to normal operation. In particular, $V_{\text{rms}2}$ reaches 149.5 V after the transient deviation induced by the fault, and the frequency is gradually returned from 59.84 Hz to the rated value 60 Hz.

It should be noted that although the conventional current/voltage based protection schemes can effectively isolate the fault and make the system return to normal operation. It must be noticed that the DG branch with fault is cut off. Even though it can be reconnected when the fault is cleared, unavoidable resynchronization algorithm should be implemented during reconnection. This resynchronization may involve some additional stability and power quality issues. The proposed VI-FCL based fault ride through method is implemented without interrupting the connectivity of DG units. Hence, no complicated resynchronization is needed.

**Case VIII: Real-Time Hardware-in-the-Loop Simulation Test**

In order to further verify the feasibility of the proposed VI-FCL, real-time HIL test is conducted. In particular, a real-time simulation environment is implemented based on OPAL-RT platform, which can be regarded as a semi-hardware platform where the AC microgrids with DG interface inverters and line impedances are modeled in the real-time environment in OPAL-RT while real hardware controllers are used to test the proposed method. Meanwhile, the whole test procedure is done in real-time. The system configuration of the real-time HIL test platform is shown in Fig. 20.

> Compared to the conventional off-line simulation test based on MATLAB/Simulink, the real-time HIL demonstration based on OPAL-RT features the enhanced test capability. Hence, the longer time test case can be verified. As shown in Fig. 10, during the whole test procedure, at $t = 40$ s, 80 s and 120 s, the fault occurs at different locations, and each fault lasts for 0.2 s. At $t = 40$ s, the fault near PCC occurs at DG branch #1, and at $t = 80$ s, the fault near DG unit occurs at DG branch #2. Finally, at $t = 120$ s, multiple faults occur simultaneously at DG branch #1 near PCC and DG branch #2 near DG unit. It can be seen from Fig. 21 (a) – (c) that with the proposed VI-FCLs, the fault current at different fault locations can be effectively suppressed. Meanwhile, the oscillation in the post-fault procedure can be significantly improved.
Fig. 11. Fault responses with different VI-FCLs.
(a) RMS current waveform with different VI-FCLs. (b) Frequency waveform with different VI-FCLs. (c) Amplitude of virtual impedance.

Fig. 12. Responses with the fault occurring at the DG branch (near DG unit).
(a) RMS current waveform of DG #1. (b) RMS current waveform of DG #2. (c) Frequency waveform.

Fig. 13. Responses with the fault occurring at the DG branch (near PCC).
(a) RMS current waveform of DG branch #1. (b) RMS current waveform of DG branch #2. (c) Frequency waveform.

Fig. 14. Responses with the fault occurring at the PCC.
(a) RMS current waveform of DG branch #1. (b) RMS current waveform of DG branch #2. (c) Frequency waveform.
Fig. 15. Responses with the faults occurring in DG branch #1 and #2 simultaneously.
(a) RMS current waveform of DG branch #1. (b) RMS current waveform of DG branch #2. (c) Frequency waveform.

Fig. 16. Responses with continuously variable load.
(a) Current profile of the common load. (b) RMS current waveform of DG branch #1. (c) RMS current waveform of DG branch #2. (d) Frequency waveform.

Fig. 17. Responses with rotating machine load.
(a) Torque waveform. (b) Rotor speed waveform.

Fig. 18. Responses of conventional current based protection scheme.
(a) RMS current waveform of DG branch #1. (b) RMS current waveform of DG branch #2. (c) Frequency waveform.
**CONCLUSION**

In order to alleviate the impact of the large fault current in inverter dominated AC microgrids, VI-FCLs are proposed to suppress the amount of current flowing through the system and mitigate the oscillation during faults and in the post-fault restoration process. The VI-FCLs are embedded in the control diagram of each DG inverter. Hence, it is a low-cost approach that is implemented without additional hardware devices. Furthermore, the impedance model of AC microgrids during faults is derived with the consideration of VI-FCLs, and the impact of the parameters of VI-FCLs on system stability is analyzed. Meanwhile, it is demonstrated that by using the proposed VI-FCLs, the large fault current can be reduced and the oscillations for different fault locations can be significantly eliminated.

**REFERENCES**


Xiaonan Lu (S’11–M’14) received the B.E. and Ph.D. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2008 and 2013, respectively. From Sep. 2010 to Aug. 2011, he was a guest Ph.D. student at Department of Energy Technology, Aalborg University, Denmark. From Oct. 2013 to Dec. 2014, he was a postdoc researcher in the Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville. In Jan. 2015, he joined the Energy Systems Division, Argonne National Laboratory, where he is currently a postdoc appointee.

His research interests include modeling and control of power electronic converters in renewable energy systems and microgrids, hardware-in-the-loop real-time simulation, distribution automation, etc. Dr. Lu received the Outstanding Reviewer Award for IEEE Transactions on Power Electronics in 2013 and the Outstanding Reviewer Award for IEEE Transactions on Smart Grid in 2015.

Dr. Lu is a member of IEEE PELS, IAS, PES and IES Society.

Jianhui Wang (M’07–SM’12) received the Ph.D. degree in electrical engineering from Illinois Institute of Technology, Chicago, IL, USA, in 2007.

Presently, he is the Section Lead for Advanced Power Grid Modeling at the Energy Systems Division at Argonne National Laboratory, Argonne, IL, USA.

Dr. Wang is the secretary of the IEEE Power & Energy Society (PES) Power System Operations Committee. He is an associate editor of Journal of Energy Engineering and an editorial board member of Applied Energy. He is also an affiliate professor at Auburn University and an adjunct professor at University of Notre Dame. He has held visiting positions in Europe, Australia and Hong Kong including a VELUX Visiting Professorship at the Technical University of Denmark (DTU). Dr. Wang is the Editor-in-Chief of the IEEE Transactions on Smart Grid and an IEEE PES Distinguished Lecturer. He is also the recipient of the IEEE PES Power System Operation Committee Prize Paper Award in 2015.

Josep M. Guerrero (S’01–M’04–SM’08–FM’15) received the B.S. degree in telecommunications engineering, the M.S. degree in electronics engineering, and the Ph.D. degree in power electronics from the Technical University of Catalonia, Barcelona, in 1997, 2000 and 2003, respectively. Since 2011, he has been a Full Professor with the Department of Energy Technology, Aalborg University, Denmark, where he is responsible for the Microgrid Research Program. From 2012 he is a guest Professor at the Chinese Academy of Science and the Nanjing University of Aeronautics and Astronautics; from 2014 he is chair Professor in Shandong University; from 2015 he is a distinguished guest Professor in Hunan University; and from 2016 he is a visiting professor fellow at Aston University, UK, and a guest Professor at the Nanjing University of Posts and Telecommunications.

His research interests is oriented to different microgrid aspects, including power electronics, distributed energy-storage systems, hierarchical and cooperative control, energy management systems, smart metering and the
internet of things for AC/DC microgrid clusters and islanded minigrids; recently specially focused on maritime microgrids for electrical ships, vessels, ferries and seaports. Prof. Guerrero is an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and the IEEE Industrial Electronics Magazine, and an Editor for the IEEE TRANSACTIONS on SMART GRID and IEEE TRANSACTIONS on ENERGY CONVERSION. He has been Guest Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS Special Issues: Power Electronics for Wind Energy Conversion and Power Electronics for Microgrids; the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS Special Sections: Uninterruptible Power Supplies systems, Renewable Energy Systems, Distributed Generation and Microgrids, and Industrial Applications and Implementation Issues of the Kalman Filter; the IEEE TRANSACTIONS on SMART GRID Special Issues: Smart DC Distribution Systems and Power Quality in Smart Grids; the IEEE TRANSACTIONS on ENERGY CONVERSION Special Issue on Energy Conversion in Next-generation Electric Ships. He was the chair of the Renewable Energy Systems Technical Committee of the IEEE Industrial Electronics Society. He received the best paper award of the IEEE Transactions on Energy Conversion for the period 2014-2015, and the best paper award of IEEE-PES in 2015. In 2014 and 2015 he was awarded by Thomson Reuters as Highly Cited Researcher, and in 2015 he was elevated as IEEE Fellow for his contributions on “distributed power systems and microgrids.”

Dongbo Zhao (S’10–M’14–SM’16) received his B.S. degree from Tsinghua University, China in 2008, M.S. degree from Texas A&M University, College Station, Texas in 2010, and Ph.D degree from Georgia Institute of Technology, Atlanta, Georgia in 2015, all in electrical engineering. Since 2014 he is the Lead Engineer at Eaton Corporation in the corporate research and technology department. He has worked with ABB Inc. US Corporate Research Center located in Raleigh, NC from 2010 to 2011. His research interests include power system control, protection, reliability analysis, transmission and distribution automation, and electric market optimization.