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Keywords

«Current regulator», «Voltage Regulator», «Power Quality», «Microgrids».

Abstract

This paper discusses the control design for an islanded microgrid in order to ensure acceptable performance in terms of voltage quality and load sharing by focusing on transient conditions. To this aim, state feedback decoupling approach has been applied. Experimental tests have been performed to demonstrate the effectiveness of the proposed approach.

Introduction

Distributed Generators (DGs) often consist of power sources connected through a power-electronic interface converter (e.g. an inverter in the case of dc-to-ac conversion) to a utility grid or microgrid. Microgrid is a local grid consisting of DGs, energy storage systems and dispersed loads which may operate in grid-connected or islanded mode [1],[2].

The main role of the DG interface converter is to control power injection. Moreover, mitigation of voltage quality problems such as harmonics and unbalance can be achieved through proper control strategies. Another important point in microgrids is the load sharing among DGs especially when the distribution lines are not symmetric [3]-[5]. In order to share fundamental positive sequence load component among inverters, droop control has been extensively applied. In this case, the accuracy of the power control is affected by the output impedance of the DG units as well as the line impedances. By including virtual impedance at fundamental frequency, the effect of the line impedances can be mitigated [6]. Furthermore, the virtual impedance can improve the sharing of nonlinear and unbalanced loads [4],[7],[8]. Recent approaches in control of power converters for stand-alone applications demonstrated the benefits introduced by decoupling the controlled states, i.e. the inductor current and capacitor voltage [9]. Higher damping of the system is achieved improving the response of the regulators during transients.

However, in the present literature, voltage quality and load sharing in transient conditions (e.g. load steps) are not well explored. Based on this, the paper applies a state feedback decoupling approach to ensure minimized voltage distortion and load sharing errors during transient conditions. A general case in which unbalanced nonlinear loads are supplied in the microgrid is considered. The control design is validated through experimental tests.

Control Structure of DGs Interface Converters

Fig. 1 shows the power stage and control system of a three-phase Voltage Source Inverter (VSI) which acts as a DG interface converter in the microgrid. The inverter is terminated by an LC filter and the control structure mainly consists of controllers for fundamental positive sequence powers (droop controllers), virtual impedance block and voltage and current inner control loops.

The details of power calculation and droop control can be found in [10]. The structure of virtual impedance block is depicted in Fig. 2 where the components of the inverter output current are extracted and then fed to a selective structure. In other words, fundamental positive sequence components are fed to an RL impedance block and other components (fundamental negative sequence as well as harmonic components, here 3rd, 5th and 7th) pass through virtual resistances [4].

Voltage controller is Proportional-Resonant (PR) whereas current controller is only formed by a Proportional (P) gain according to the following equations:

$$G_v(s) = k_{pV} + \sum_{h=1,3,5,7} \frac{k_{ih}[scos(\varphi) - h\omega_1 \sin(\varphi)]}{s^2 + (h\omega_1)^2} \tag{1}$$

$$G_i(s) = k_{pI} \tag{2}$$

The inner current and voltage loops are cascaded and designed using serial tuning. The bandwidth of the inner current loop is set to a value that provides fast dynamic performance, and avoids interactions with the voltage loop. In practical applications the maximum allowed bandwidth for the inner current loop is mainly limited by the transport and sampling delays.

In islanded microgrids, the VSI operates in voltage mode where the capacitor voltage and inductor currents are the controlled states [11]. With reference to Fig. 1, the voltage and current are measured and transformed to the stationary reference frame (αβ), being $\boldsymbol{i}_{L\alpha\beta}$ and $\boldsymbol{v}_{o\alpha\beta}$ the inductor current and capacitor voltage vectors, respectively.

The voltage loop, with the limitations imposed by its bandwidth, controls the converter output voltage by fixing the current reference. The inner current loop controls the inverter states in order to follow the current reference.

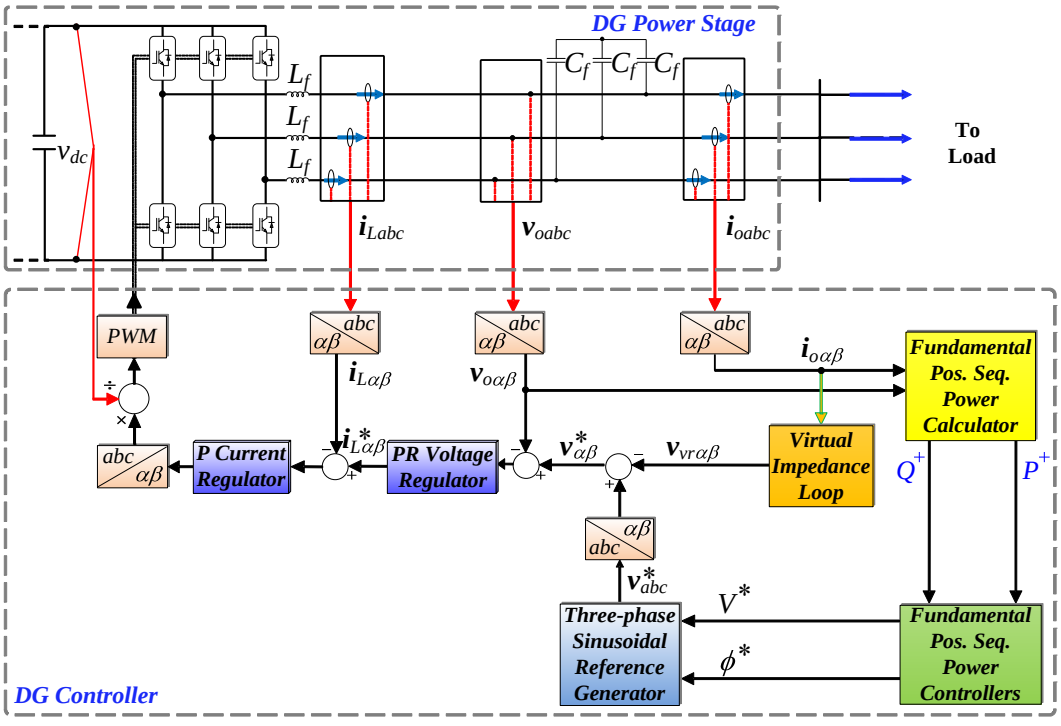


Fig. 1. DG power stage and control system

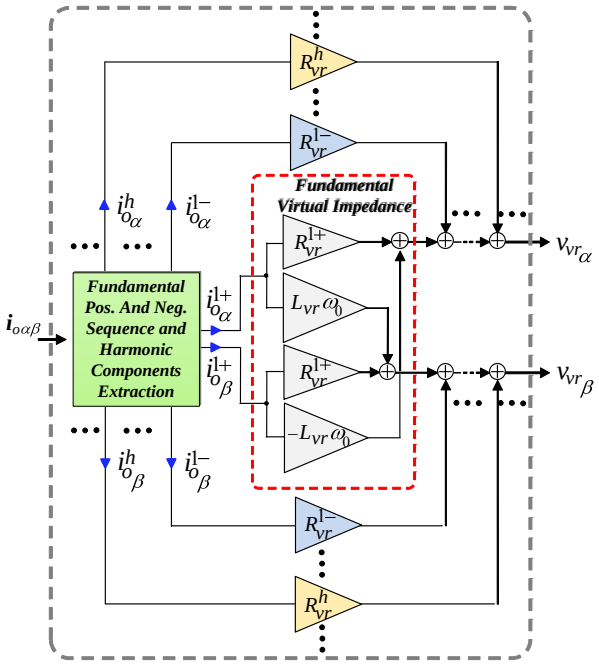


Fig. 2. Virtual impedance scheme [4]

Design of Voltage and Current Regulators

It is expected from any current or voltage regulator: i) to provide zero steady-state error; ii) accurately track the commanded reference during transients; iii) have a bandwidth as higher as possible; and iv) decrease or minimize the total harmonic distortion.

The general approach to design the inner current loop is to neglect the coupling between the inductor current and the capacitor voltage. This is the basic assumption in AC drives and grid connected applications, as the electromotive force is strong, and acts as a disturbance to the current regulator.

The proportional gain of the current regulator is selected to achieve the desired bandwidth of approximately $f_{bw} = 1\,kHz$. For the delay of the system $T_d = 1.5/f_s = 150\,\mu s$, and the system parameters (see Table I), the controller gain is approximately $k_{pI} = 5.61$ (see Table II).

Table I. System parameters

Parameter	Symbol	Value
Switching frequency	f_s	10 kHz
Filter inductance	L_f	1.8 mH
Filter capacitance	C_f	27 µF
Inductor ESR	R_f	0.1 Ω
Rated linear load	R_l	68 Ω
Nonlinear load	C_{NL}	235 µF
	R_{NL}	155 Ω
	L_{NL}	0.084 mH

Table II. Current regulator control parameters

Parameter	Symbol	Value
Proportional gain w/o decoupling	k_{pI}	5.61
Proportional gain with decoupling	k_{pI}	6.42

Table III. Voltage regulator control parameters

Parameter	Symbol	Value
Proportional gain	k_{pV}	0.05
Integral gain	k_{iV}	100
Integral gain 3rd HC	$k_{iV,h3}$	10
Integral gain 5th HC	$k_{iV,h5}$	10
Integral gain 7th HC	$k_{iV,h7}$	10

Table IV. Droop control parameters

Parameter	Symbol	Value
Proportional gain (active power)	k_{pP}	1×10^{-6}
Integral gain (active power)	k_{iP}	1×10^{-4}
Proportional gain (reactive power)	k_{pQ}	5×10^{-4}

Table V. Virtual impedance parameters

Parameter	Symbol	Value
Virtual inductance	L_{vr}	2.5 mH
Fund. pos. sequence	R_{vr}^{1+}	0.3 Ω
Fund. neg. sequence	R_{vr}^{1-}	1.5 Ω
Pos. and neg. sequence 3rd H	R_{vr}^{3}	2 Ω
Pos. and neg. sequence 5th H	R_{vr}^{5}	4 Ω
Pos. and neg. sequence 7th H	R_{vr}^{7}	4 Ω

The effect of decoupling the controlled states is clearly shown by the frequency response analysis of the system with a P controller as current regulator. The frequency response as a function of the load impedance is shown in Fig. 3(a). In this case, the range of variation is from rated to no-load condition, with arrows indicating increase in the load impedance. The system has a strong load dependency with low gain at low frequencies. For this reason, an integral term is needed to achieve zero steady-state error if voltage decoupling is not performed.

On the other hand, if the controlled states are decoupled, the system has much higher damping and less overshoot for the same bandwidth, as shown in the frequency response of Fig. 3(b). Moreover, the inner current loop becomes independent of the load. The magnitude at low frequencies is almost 0 dB, thus allowing the use of a P controller in the current loop when voltage decoupling is performed.

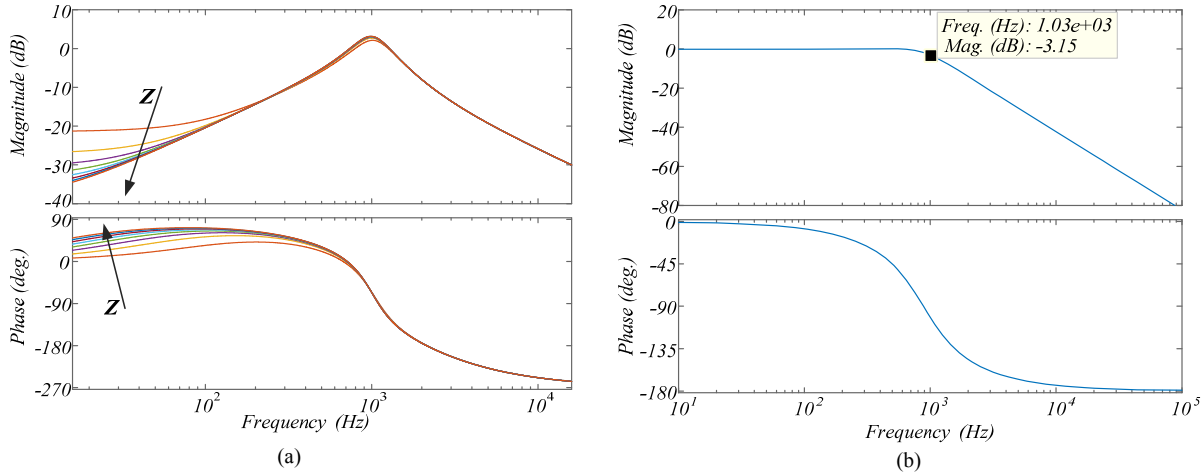


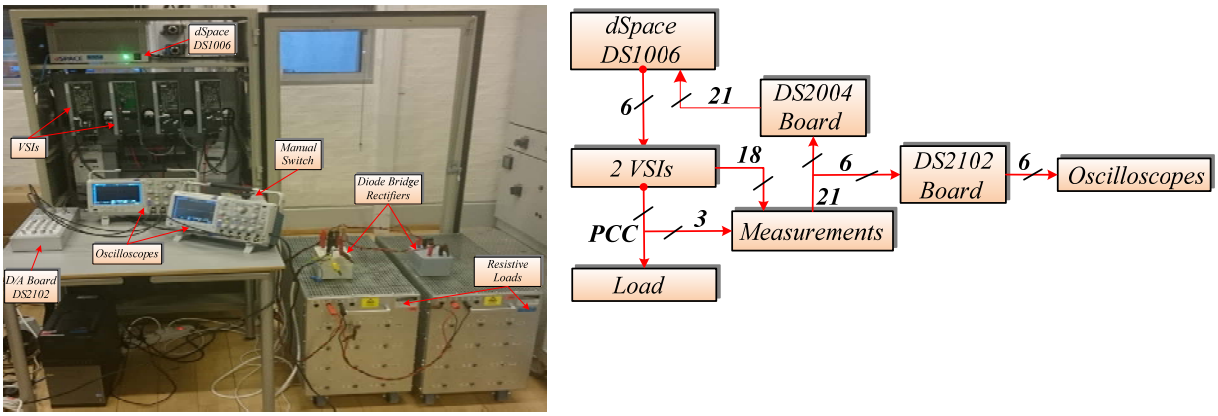
Fig. 3. Frequency response of the current loop only with a P controller as current regulator: (a) without decoupling; (b) with decoupling

The design of the voltage regulator is based on the procedure illustrated in [9]. According to the open loop trajectories on the Nyquist diagram it is possible to determine the leading angles in (1) at each harmonic frequency. The parameters for the voltage loop are shown in Table III.

Experimental Results

The theoretical analysis is validated through experimental results. For this purpose, a low scale test bed made up of two Danfoss power converters of 2.2 kW each has been built. The control platform is based on dSPACE DS1006. An Analog-to-Digital DS2004 board is used to digitalize the analog signals sensed via LEM current and voltage transducers. A Digital-to-Analog conversion 16-bit high resolution board DS2102 has been used to record the data on two oscilloscopes.

The photo and schematic diagram of the experimental setup are shown in Fig. 4(a) and Fig. 4(b), respectively. The PWM signals for each VSI are sent from dSPACE DS1006 platform, based on the implemented control law. Three-phase inductor currents, capacitor voltage and output current are measured for each VSI, as well as the voltage at the Point of Common Coupling (PCC). The measured variables are sent to the A/D board DS2004. Only the reference, measured and error values of capacitor voltage in α-axis from each VSI are sent to the D/A board DS2102 and then to the oscilloscopes.

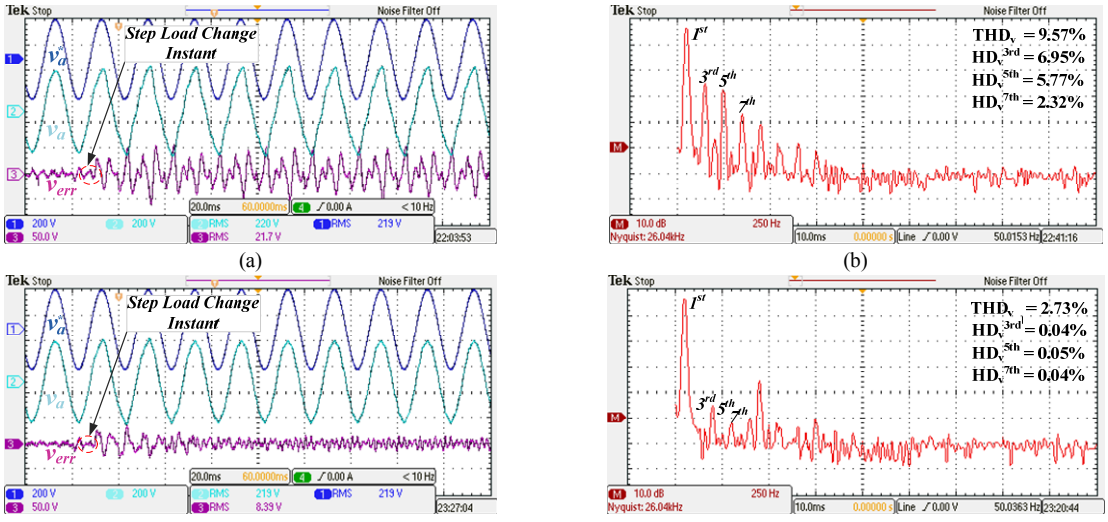


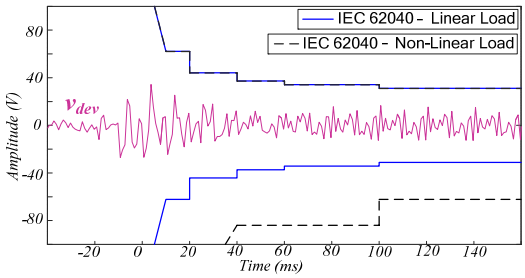
(a) (b)

Fig. 4. (a) Photo and (b) Schematic diagram of the experimental setup

All the following experimental results are performed using a P controller as current regulator and with state feedback cross-coupling decoupling of the capacitor voltage. Resonant regulators tuned at specific harmonic orders are used in the outer voltage loop. The two parallel power converters are droop-controlled and operate in voltage control mode. Two diode bridge rectifiers are used as nonlinear loads, with unbalance created opening one phase on the AC side of the loads. The system and control parameters are shown in Table I-V. In particular, the design of the virtual impedance and droop control parameters is based on [4] and [10].

In Fig. 5(a), a 100% unbalanced nonlinear step load change (from open circuit to full rated load) is performed, without activating the harmonic compensators (HC) in the voltage loop for both power converters. As expected from the FFT analysis [see Fig. 5(b)], harmonics are present in the capacitor voltage, mainly a 3rd harmonic component due to unbalanced nonlinear load. Performing the step load change with HC activated at the 3rd, 5th and 7th harmonic orders [see Fig. 5(c)] reduces significantly the THDv, without interfering with the transient response. Still the system reaches steady-state in less than one cycle and a half after the load step change. Since the bandwidth of the voltage loop has been set to 100 Hz, a 3rd HC is needed. The transient response complies with the standards imposed by IEC 62040 for UPS systems, as shown in Fig. 5(e). Similar results are obtained for the other power converter, referred to as DG_2.





(e)

Fig. 5. Unbalanced nonlinear step load change with DGs in parallel: DG_1 with output impedance of L_1 = 1.8 mH; DG_2 with output impedance of L_2 = 1.8 mH - (a) Transient response without HC, reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis); (b) FFT of the capacitor voltage (250 Hz/div); (c) Transient response with 3rd, 5th, 7th HC, reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis); (d) FFT of the capacitor voltage (250 Hz/div); (e) 100% Step load change, Dynamic characteristics according to IEC 62040 standard for linear and nonlinear loads

Unbalance between the two lines supplying the loads is created doubling the line impedance at the output of DG_1. Again, a 100% unbalanced nonlinear step load change is performed [see Fig. 6(a)]. Both power converters have the HC at 3rd, 5th and 7th harmonic activated. The steady-state voltage at PCC between the two VSIs is shown in Fig. 6(b), which results in an Unbalance Factor (UF) of 0.32%, in compliance with the standards which set the upper limit to 2%. However, the load is not equally shared between the DGs as can be seen comparing Fig. 6(e) and Fig. 6(f). These last data have been plotted in MATLAB after have been recorded in dSPACE ControlDesk scopes.

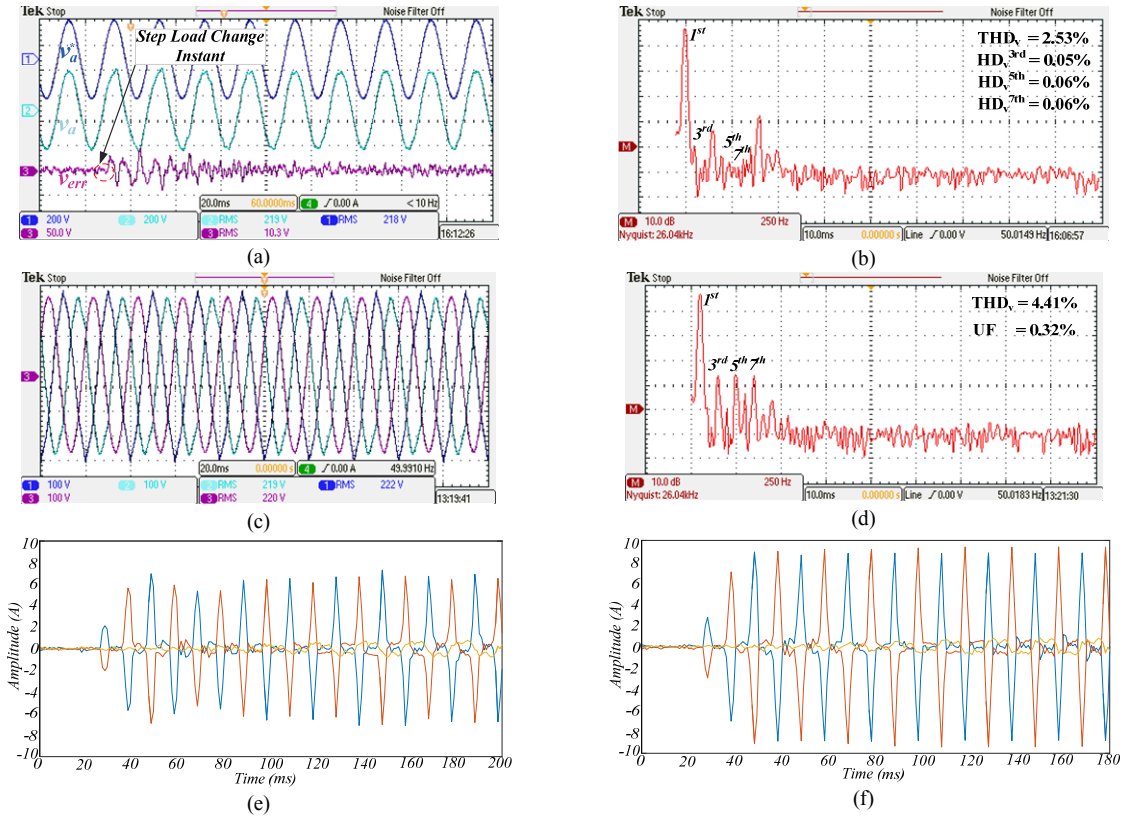


Fig. 6. Unbalanced nonlinear step load change with DGs in parallel: DG_1 with output impedance of L_1 = 3.6 mH; DG_2 with output impedance of L_2 = 1.8 mH; virtual impedance not activated - (a) Transient response, reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis); (b) FFT of the capacitor voltage (250 Hz/div); (c) Voltage at PCC; (d) FFT of voltage at PCC (250 Hz/div); (e) Transient conditions, output current from DG_1; (f) Transient conditions, output current from DG_2

When the Virtual Impedance outer loop is activated, the current sharing improves noticeably [see Fig. 7(e) and Fig. 7(f)]. This improvement is achieved by decrease/increase of DG_2/DG_1 current components. In addition, fundamental positive sequence component of load current is still shared, properly. However, it can be seen that the current sharing improvement is achieved at the expense of increasing all voltage distortions: slight increase in THD and the UF at PCC [see Fig. 7(c) and Fig. 7(d)] as well as DGs terminal [see Fig. 7(a) and Fig. 7(b)].

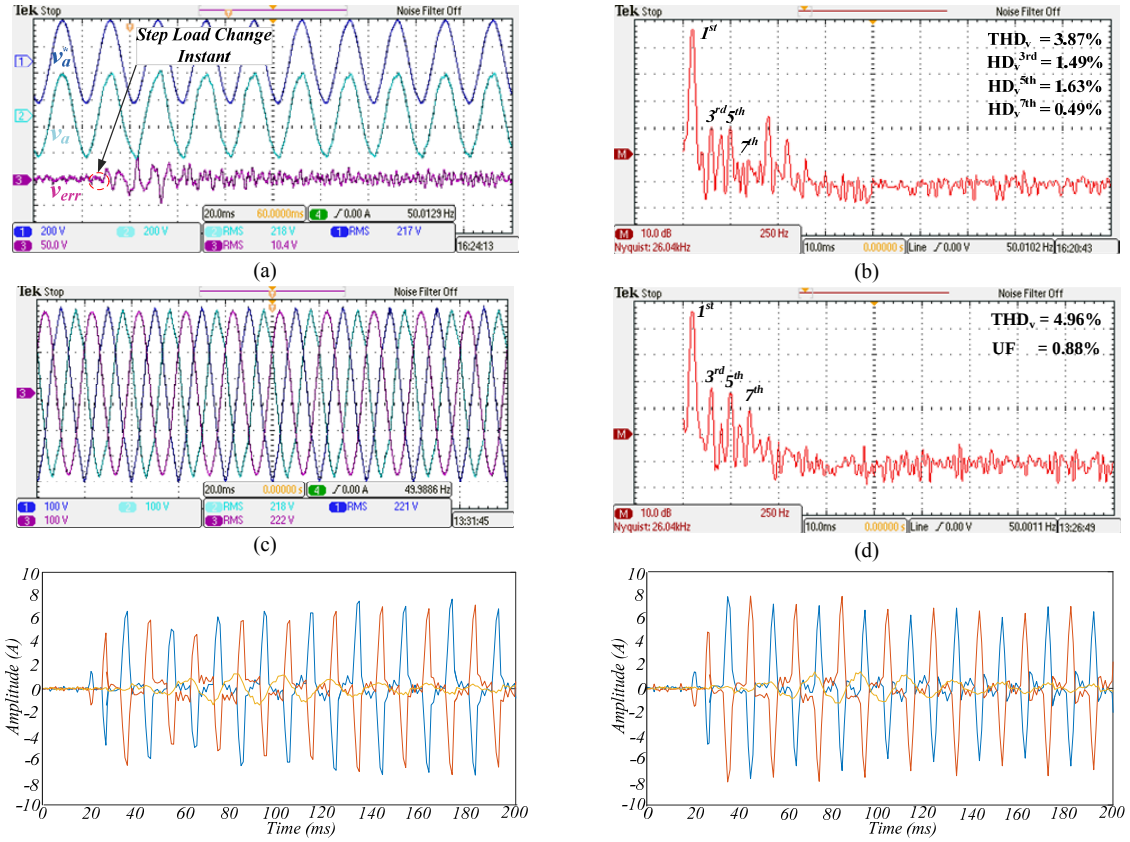


Fig. 7. Unbalanced nonlinear step load change with DGs in parallel: DG_1 with output impedance of L_1 = 3.6 mH; DG_2 with output impedance of L_2 = 1.8 mH; virtual impedance activated - (a) Transient response, reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis); (b) FFT of the capacitor voltage (250 Hz/div); (c) Voltage at PCC; (d) FFT of voltage at PCC (250 Hz/div); (e) Transient conditions, output current from DG_1; (f) Transient conditions, output current from DG_2

Conclusion

Design and experimental validation of control for inverter-based microgrids have been addressed. It is demonstrated that a significant increase in performance for both steady state and transient conditions can be achieved by proper design of inner voltage and current control loops of DGs interface converters. The system is much more damped when the controlled states are decoupled, allowing the use of a proportional controller as current regulator.

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