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Phase-Lock Loop of Grid-Connected Voltage Source Converter under Non-Ideal Grid Condition

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***Abstract*—It is a normal practice that the DC micro-grid is connected to AC main grid through Grid-connected Voltage Source Converter (G-VSC) for voltage support. Accurate control of DC micro-grid voltage is difficult for G-VSC under unbalanced grid condition as the fundamental positive-sequence component phase information cannot be accurately tracked. Based on analysis of the cause of double-frequency ripple when unbalance exists in main grid, a phase-locked loop (PLL) detection technique is proposed. Under the conditions of unsymmetrical system voltage, varying system frequency, single-phase system and distorted system voltage the proposed PLL can accurately detect the fundamental positive-sequence component of grid voltage thus accurate control of DC micro-grid voltage can be realized.**

Keywords—DC micro-grid; grid-connected voltage source converter; PLL; non-ideal grid condition

I. INTRODUCTION

Distributed energy resources which utilize renewable sources of energy has become one of the key elements for modern environmental friendly and sustainable development, and micro-grid systems show great promise for integrating large numbers of distributed energy resource (DER) into future power networks. Micro-grid is a controllable system which consists of multiple distributed power, energy storage devices, as well as local loads. It can be used as an independent entity connected to power grid and can also operate in islanding mode, which is flexible and reliable. Now the prospect of DC micro-grid is expected even if AC micro-grid has been the main type.

Compared with AC micro-grid, DC micro-grid obtains some advantages such as less energy conversion links, higher system efficiency, lower line losses, etc. In addition, tracking the phase and frequency of the voltage is not needed in inner DC micro-gird, which greatly improves the controllability and reliability of system, and thus DC micro-grid is more suitable for the access of the distributed power. However, the DC micro-grid has to be connected to AC main grid through Grid-connected Voltage Source Converter (G-VSC) for voltage support and energy management. The accurate control of DC micro-grid voltage is difficult for G-VSC under unbalanced grid condition as the fundamental positive-sequence component phase information cannot be accurately tracked.

The hardware phase-locked method depends on the detection of zero-cross point of voltage, which is sensitive to harmonic and disturbance. The PLL which is suitable for software implementation can achieve good control results, but it cannot accurately track the phase information of the fundamental positive-sequence voltage for the double-frequency ripple in synchronous rotating coordinates when unbalance exists in power grid. To measure the positive-sequence separately from the negative-sequence, a low-pass filter with a narrow bandwidth is normally used. However, such a filter causes a lot of phase delay, thus the response time of the system tends to be lengthened [4]. To solve this problem, a time shift method is used in [5] to separate the positive-sequence and negative-sequence components, which effectively inhibits the influence of negative-sequence component on phase calculation. In [6], a method of phase-locked loops based on dual-dq synchronous transform is proposed, but the low-pass filter whose interceptive frequency is rather low to obtain the DC component on dq-axis is needed. A PLL detection technique based on sequence-decoupled resonant (SDR) controller which is used to separate positive-sequence component of grid voltage from unsymmetrical voltage to trace the phase of positive-sequence component is proposed in [7] and [8], thus the function of PLL is implemented.

In this work, a PLL detection technique is proposed, in which q-axis signal is added to the d-axis to eliminate the influence of double-frequency ripple after 90° phase shifting through a FIR filter. The proposed PLL is analyzed through the testing of simulation, and the experimental platform was built for experimental verification. Both the results of simulations and experiments show that under the conditions of unsymmetrical system voltage, varying system frequency, single-phase system and distorted system voltage the proposed method can accurately detect the fundamental positive-sequence component of grid voltage.

II. G-VSC PLL

A. Gird-connected converter

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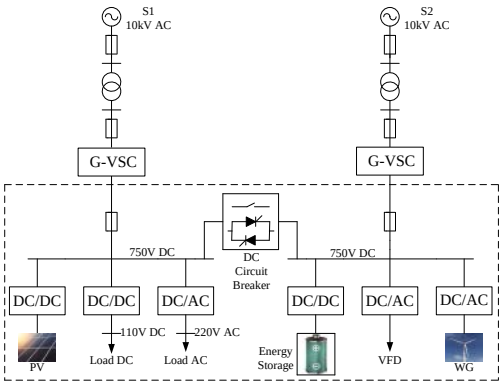

Fig.1. Example of a figure caption

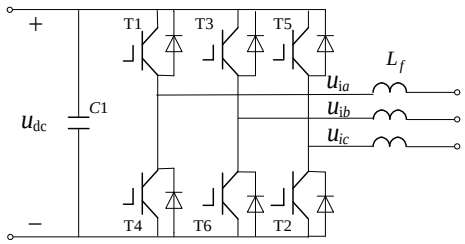

Fig.2. Typical G-VSC topology

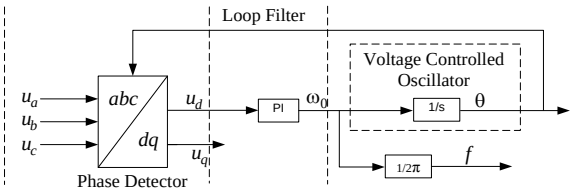

Fig.3. Example of a figure caption

It is a normal practice that the DC micro-grid is connected to AC main grid through bidirectional G-VSC which is employed to support the DC micro-grid voltage during the grid connection operation mode, as shown in Fig.1. Typical G-VSC topology is shown in Fig.2. In order to realize decoupling control of DC bus voltage and reactive power, G-VSC demands transformation between static three-phase coordinate and rotary two-phase coordinate, which is dependent on accurate grid voltage synchronous phase-locked loop.

B. Working Principle of PLL

The structure of software phase-locked loop based on synchronized coordinates is shown in Fig.3 [10], where ω_0 stands for grid angular frequency, f stands for grid frequency, and θ is grid voltage vector rotation angle. The static three-phase coordinate is transformed to rotary two-phase coordinate by phase detector.

III. PHASE-LOCKED UNDER THREE-PHASE UNBALANCE CONDITION

A. Unbalanced power grid

The AC grid voltage could exist three-phase unbalance for short-circuit fault or unbalanced load, which proposes higher demand on PLL. Without considering harmonic component, the grid three-phase voltage can be formulated as

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} E^+ sin(\omega_0 t + \theta_p) + \\ E^+ sin\left(\omega_0 t - \frac{2\pi}{3} + \theta_p\right) + \\ E^+ sin\left(\omega_0 t + \frac{2\pi}{3} + \theta_p\right) + \end{bmatrix} \begin{bmatrix} E^- sin(-\omega_0 t + \theta_n) \\ E^- sin\left(-\omega_0 t - \frac{2\pi}{3} + \theta_n\right) \\ E^- sin\left(-\omega_0 t + \frac{2\pi}{3} + \theta_n\right) \end{bmatrix} \quad (1)$$

where E^+ and E^- stand for the positive-sequence and negative-sequence voltage respectively, θ_p and θ_n stand for positive-sequence and negative-sequence initiative voltage phase respectively, and ω_0 is grid angle frequency.

The coordinate transforms of static three-phase coordinate (a, b, c) to rotary two-phase coordinate (d, q) for three-phase voltage can be presented as

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} E^+ sin(\omega_0 t + \theta_p - \theta) + \\ -E^+ \cos\left(\theta - \left(\omega_0 t + \theta_p\right)\right) - \end{bmatrix} \begin{bmatrix} E^- sin(-\omega_0 t + \theta_n - \theta) \\ E^- \cos\left(\theta - (-\omega_0 t + \theta_n)\right) \end{bmatrix} \quad (2)$$

where θ stands for the output phase information of PLL. When the error of output phase information is smaller, it can be considered that

$$\theta = \omega_0 t + \theta_p \quad (3)$$

Using equation (3), equation (2) can be rewritten as

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} -E^- sin\left(2\omega_0 t - \theta_n + \theta_p\right) \\ -E^+ - E^- \cos\left(2\omega_0 t - \theta_n + \theta_p\right) \end{bmatrix} = \begin{bmatrix} u_d^+ + u_d^- \\ u_q^+ + u_q^- \end{bmatrix} \quad (4)$$

where

$$\begin{bmatrix} u_d^+ \\ u_q^+ \end{bmatrix} = \begin{bmatrix} 0 \\ -E^+ \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} u_d^- \\ u_q^- \end{bmatrix} = \begin{bmatrix} -E^- sin\left(2\omega_0 t - \theta_n + \theta_p\right) \\ -E^- \cos\left(2\omega_0 t - \theta_n + \theta_p\right) \end{bmatrix} \quad (6)$$

Analyzing equation (4)-(6), it can be found that positive-sequence and negative-sequence voltage produce DC component and double frequency component respectively. To measure the positive-sequence voltage separately from the negative-sequence, a low-pass filter with a narrow bandwidth is normally used in traditional PLL. However, such a filter causes a lot of phase delay, thus the response time of the system tends to be lengthened.

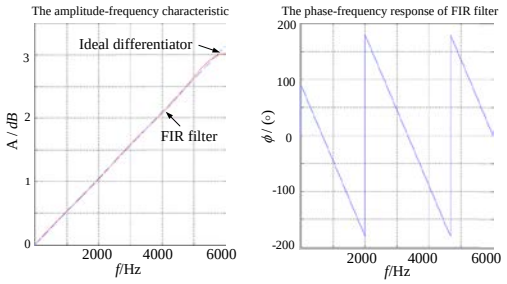

Fig.4. The amplitude frequency characteristics and phase-frequency characteristics of FIR filter (*N*=9)

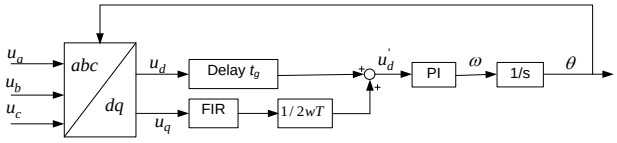

Fig.5. Proposed PLL

B. Proposed PLL

In this paper, a PLL detection technique is proposed, in which a signal that has 180 degree shift to u_d^- is added to u_d to eliminate the influence of double-frequency ripple. Equation (6) shows that u_d^- and u_q^- must be equal of amplitude and the phase-shift between each other should be 90 degree, thus the 90^0 phase difference of u_q^- can be shifted to obtain the signal that has 180 degree shift to u_d^- by all-pass filter. However, the phase shift angle must be changed as the frequency has a change. To solve this problem, the differentiator can be used to realize 90^0 phase shift of u_d^-, as shown in equation (7).

$$u_d^- + \frac{1}{2\omega_o}\frac{d(u_q^-)}{dt} = 0 \tag{7}$$

Nevertheless, the differentiator is very sensitive to noise, by which the PLL instability is induced [10]. Therefore the FIR filter is used in approximating differentiator.

The frequency response of ideal differentiator can be written as

$$H_0(f) = j2\pi f = 2\pi f e^{j\pi/2} \tag{8}$$

Generally the differentiator can be approximated by IV-type linear phase FIR filter, as show in equation (9).

$$H_1(f) = 2\pi f T e^{j\pi/2 - j\pi N f T} \tag{9}$$

where *N* should be odd. In this paper, *N*=9 and sampling period *T*=1/12000s. Its amplitude frequency characteristic and phase frequency characteristic is shown in Fig.4, which shows that FIR filter can commendably approximate differentiator. Its frequency amplitude response and phase frequency response can be written respectively as

$$\begin{cases} A(f) = 2\pi f T \\ \varphi(f) = \dfrac{\pi}{2} - \pi N T f \end{cases} \tag{10}$$

It is noted in (10) that the output signal amplitude is $2\pi fT$ times than input signal amplitude, so the output signal amplitude must divided by $2\pi fT$. f is two times larger than fundamental frequency f_0 as u_q^- is double frequency component. In addition, the delay time of FIR filter is πNTf, namely the group delay $t_g = NT/2$, so u_d must delay $NT/2$ before injecting FIR filter output signal. After eliminating the double-frequency ripple, we can get

$$u_d' = u_d \cdot (t - t_g) + \frac{FIR(u_q)}{2\omega T} \tag{11}$$

As N should be odd, group delay $t_g = NT/2$ cannot be the integral multiple of sampling period. Considering linear processing between two sampling points, the following is obtained

$$\begin{aligned} u_d(t - t_g) &= u_d(t - NT/2) \\ &= \frac{\left[u_d\left(t - \frac{(N-1)T}{2}\right) + u_d\left(t - \frac{(N+1)T}{2}\right)\right]}{2} \end{aligned} \tag{12}$$

So equation (11) can be rewritten as

$$\begin{aligned} u_d' &= FIR(u_q)/2\omega T + \\ &\frac{\left[u_d\left(t - \frac{(N-1)T}{2}\right) + u_d\left(t - \frac{(N+1)T}{2}\right)\right]}{2} \end{aligned} \tag{13}$$

The control block diagram of proposed PLL is shown in Fig.5. This PLL is not affected by grid frequency and when the grid frequency varies, the response rate depends on the FIR filter parameters design.

C. *Application of the PLL to single-phase power system*

The proposed PLL is also applicable to single-phase power system. In three-phase system, when loss of power accident occurs in two phases, the three-phase voltage is obtained

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} E\sin(\omega_0 t + \theta_p) \\ 0 \\ 0 \end{bmatrix} \tag{14}$$

where E is voltage amplitude, ω_0 is system angle frequency, θ_p is initiative voltage phase. Thus equation (2) can be rewritten as

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} E[\sin(\omega_0 t + \theta_p + \theta) + \\ E[\cos(\omega_0 t + \theta_p + \theta) - \end{bmatrix} \begin{matrix} \sin(\omega_0 t + \theta_p - \theta)]/3 \\ \cos(\omega_0 t + \theta_p - \theta)]/3 \end{matrix} \tag{15}$$

It can be considered that $\theta = \omega_0 t + \theta_p$ while the locked phase errors is small, then equation (15) can be rewritten as

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} \frac{E}{3}\sin(2\omega_0 t + 2\theta_p) \\ \frac{E}{3}\cos(2\omega_0 t + 2\theta_p) - \frac{E}{3} \end{bmatrix} \tag{16}$$

It can be found that u_d and u_q has equal amplitude and 90 degree phase difference, and same result was also obtained by analyzing three-phase unbalanced power grid in previous paper. Therefore the formula represented by expression (6) is shown to be available for single-phase system.

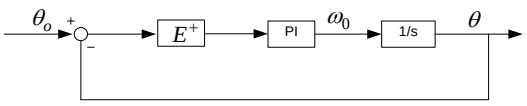

Fig.6. Small signal linear model of PLL

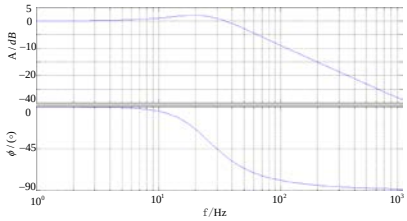

Fig.7. The bode diagram of closed-loop transfer function of PLL

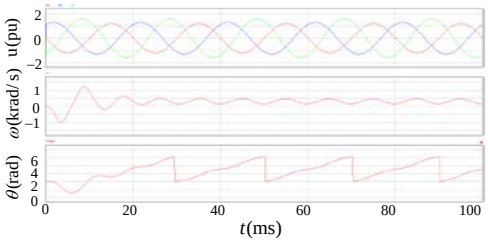

Fig.8. The simulation results of conventional PLL

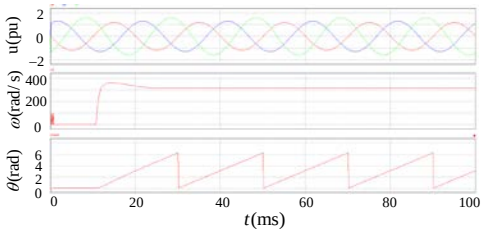

Fig.9. The simulation results of proposed PLL

Fig.10. Experimental platform

IV. PLL PARAMETER DESIGN

Neglecting sample delay, the small-signal linear model is shown in Fig.6. From Fig.6 it can be seen that the PLL open-loop transfer function is

$$H_0(s) = \frac{E^+(k_p s + k_i)}{s^2} \tag{17}$$

Thus the closed-loop transfer function is given

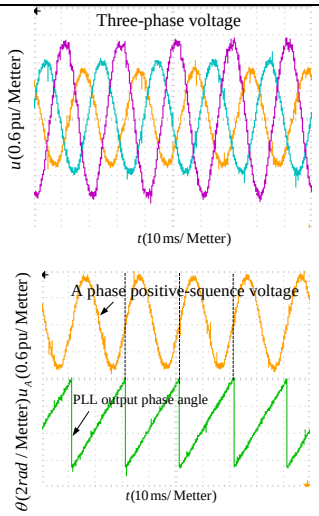

Fig.11. Experimental waveforms of PLL under unsymmetrical voltage

$$H(s) = \frac{\theta(s)}{\theta_o(s)} = \frac{2\varepsilon\omega_n s + \omega_n^2}{s^2 + 2\varepsilon\omega_n s + \omega_n^2} \tag{18}$$

where $\omega_n = \sqrt{k_i E^+}$, $\varepsilon = k_p\omega_n/2k_i$. It is noted in (18) that the closed-loop transfer function is a typical second-order system transfer function, and the natural angle frequency has great influence on PLL performance. Increasing the natural angle frequency can improve response speed, but the noise inhibiting ability will be decreased. Through PARK transformation, the voltage frequency wave of N times in power system will generate $N-1$ times frequency and $N+1$ times frequency component, so the PI parameters should be designed to inhibit harmonic components produced by odd harmonics of power system. As the proposed PLL can eliminate double frequency component, inhibiting four and above times frequency component should be considered in the design of PI parameters. In this paper, $\omega_n = 2\pi \times 25$, $\varepsilon = 0.707$, let positive-sequence voltage amplitude sampled by DSP $E^+ = 1$V, thus the PI parameters can be obtained

$$k_i = 24649, \qquad k_p = 222 \tag{19}$$

The bode diagram of $H(s)$ is shown in Fig.7. It can be seen that the amplitude response of four times frequency component is -15dB, and the more the times of harmonics, the better effect of the inhibition.

V. DIGITAL SIMULATION AND PHYSICAL EXPERIMENT VERIFICATION

In order to study on the performance of proposed PLL under three-phase unbalance, computer simulations were carried out by using PSIM, and Fig.8 and Fig.9 are the simulation result. Fig.8 shows that the output angle phase of traditional PLL contains second harmonic component and the grid voltage phase information cannot be accurately tracked by traditional PLL, while the proposed PLL can accurately track the grid voltage phase information and the angle phase does not contain second harmonic component as shown in Fig.9.

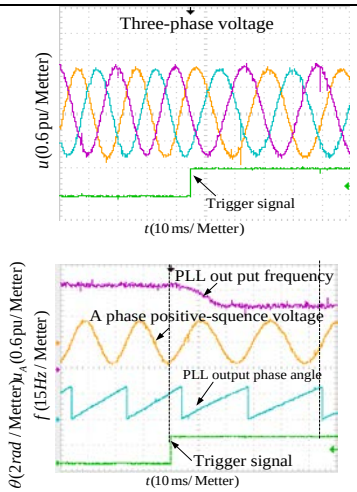

Fig.12. Experimental waveforms of PLL under varying system voltage(50Hz—37.5Hz)

The experiment platform based on TMS32OF28335 DSP which is designed by TI company was build for further verification, as shown in Fig.10. Fig.11 is the phase-locked result under unsymmetrical voltage, which shows that the proposed method can accurately detect the fundamental positive-sequence component of grid voltage even though the three-phase unbalance exists. Fig.12 shows the phase-locked result when the grid voltage frequency is changed from 50Hz into 37.5Hz. The proposed PLL can detect grid phase and frequency information within two periods.

The experimental waveforms of proposed PLL under single-phase system are shown in Fig.13, which prove that the fundamental positive-sequence component phase information can be accurately tracked while the grid system is in single-phase.

When there are harmonics on the power system, the experimental waveform is shown in Fig.14. Third harmonic, fifth harmonic and seventh harmonic are injected into three-phase grid voltage. It is seen that the proposed PLL still exhibit high performances in spite of harmonics within the grid system.

VI. CONCLUSIONS

Based on the analysis of the cause of double-frequency ripple when unbalance exists in main grid, a new PLL detection technique is proposed, in which q-axis signal is added to the d-axis to eliminate the influence of double-frequency ripple after 90° phase shifting through a FIR filter. Both the results of simulation and experiments show that under the conditions of unsymmetrical system voltage, varying system frequency, single-phase system and distorted system voltage the proposed method can accurately detect the fundamental positive-sequence component of grid voltage.

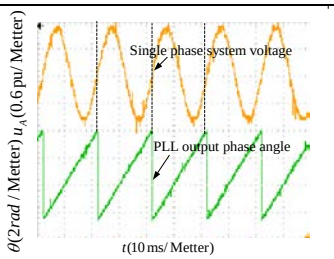

Fig.13. Experimental waveforms of PLL under single-phase system voltage

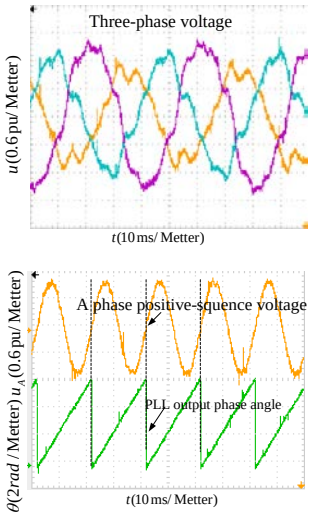

Fig.14. Experimental waveforms of PLL under distorted system voltage

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