A Circulating Current Suppression Method for Parallel Connected Voltage-Source-Inverters (VSI) with Common DC and AC Buses

Wei, Baoze; Guerrero, Josep M.; Quintero, Juan Carlos Vasquez; Guo, Xiaoqiang

Published in:
Proceedings of 8th IEEE Energy Conversion Congress and Exposition (ECCE), 2016

DOI (link to publication from Publisher):
10.1109/ECCE.2016.7854655

Publication date:
2016

Document Version
Early version, also known as pre-print

A Circulating Current Suppression Method for Parallel Connected Voltage-Source-Inverters (VSI) with Common DC and AC Buses

Baoze Wei, Josep M. Guerrero, Juan C. Vásquez
Department of Energy Technology
Aalborg University
Aalborg, Denmark
bao@et.aau.dk, joz@et.aau.dk, juq@et.aau.dk

Xiaoqiang Guo
Department of Electrical Engineering
Yanshan University
Qinhuangdao, China
gxq@ysu.edu.cn

***Abstract*—This paper describes a theoretical with experiment study on a control strategy for the parallel operation of three-phase voltage source inverters (VSI), to be applied to uninterruptible power systems (UPS). A circulating current suppression strategy for parallel VSIs is proposed in this paper based on circulating current control loops used to modify the reference currents by compensating the error currents among parallel inverters. Both of the cross and zero-sequence circulating currents are considered. The proposed method is coordinated together with droop and virtual impedance control. In this paper, droop control is used to generate the reference voltage of each inverter, and the virtual impedance is used to fix the output impedance of the inverters. In addition, a secondary control is used in order to recover the voltage deviation caused by the virtual impedance. And the auxiliary current control loop is added to acquire a better average current sharing performance among parallel VSIs, which can effectively suppress both of the cross and zero-sequence circulating currents. Experimental results are presented in order to verify the effectiveness of the proposed control strategy.**

Keywords—voltage source inverter; parallel connected; cross circulating current; zero-sequence; common DC and AC buses; uninterruptible power system

I. INTRODUCTION

As the rating of switching devices is often limited or constrained by technical or economic considerations, parallel architecture is often adopted to increase the power rating [1], [2]. The features of high reliability and redundancy make it attractive in many UPS applications [3], such as high speed elevators, high-power electric drives and distributed generation systems as an interface between the utility grid and distributed power sources [4]. The topology of two paralleled inverters is shown in Fig.1.

In a parallel system, one of the main problems is the circulating current. Furthermore, when inverters are connected in parallel with common dc and ac buses, the zero-sequence circulating current problem will occur besides the cross circulating current [2], [5]. One simple method of dealing with such a problem is to add isolation transformers to the ac sides of inverters, thus changing the circulating current circuit into an open circuit. The main disadvantage of this solution is that the isolation transformers are bulky and expensive, and they incur both core and copper losses [5].

A traditional current-sharing solution is the frequency and voltage droop method with the feature of wireless control among UPS units [6]. But the droop-method performance is particularly sensitive to the output impedance of the parallel inverters [7]. Virtual impedance is proposed in [8] to modify the output impedance, contributing to good power-sharing accuracy. However, in a practical paralleled inverters system, it is difficult to design proper virtual impedance. And if poorly designed or implemented, the virtual impedance may introduce current distortions and adversely affect the system stability and dynamics [9].

In order to solve the problems of above mentioned control strategies, this paper proposed a control strategy based on circulating current control loops with droop and virtual impedance control. In the control strategy, the droop control is used to generate the reference voltages of each inverter, and the virtual impedance is used to regulate the output impedance of the inverters, and the proposed circulating current control loops are added to analysis the current difference between parallel inverters, including the d-axis, q-axis and zero-axis currents, then the error currents are used to compensate the reference currents, and with proper controller design, both of the cross circulating current and zero-sequence circulating current can be effectively suppressed, finally to reach the purpose of average current-sharing between parallel inverters. The concept of the proposed control strategy is based on the distributed control strategy. In the distributed control strategy, the average unit current can be determined by measuring the total load current and then divide this current by the number of units in the system [10]. More details will be introduced in section II.

This paper is organized as follows: In Section II, the circulating current analysis for paralleled VSIs is discussed. And the proposed control strategy based on circulating current control loops with droop and virtual impedance control is presented. In Section III, experimental results are implemented which verify the effectiveness of the proposed method. The conclusion is given in Section IV.

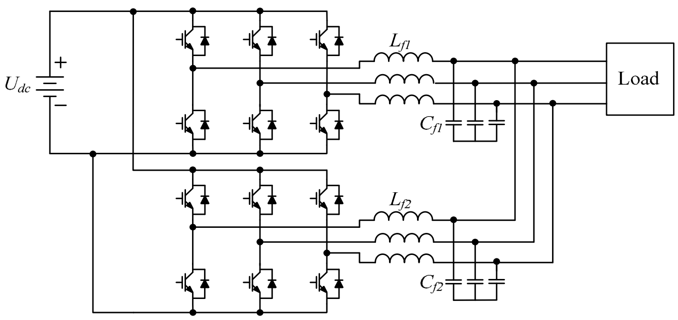


Fig. 1. Two inverters work in parallel.

II. The Proposed Control Strategy

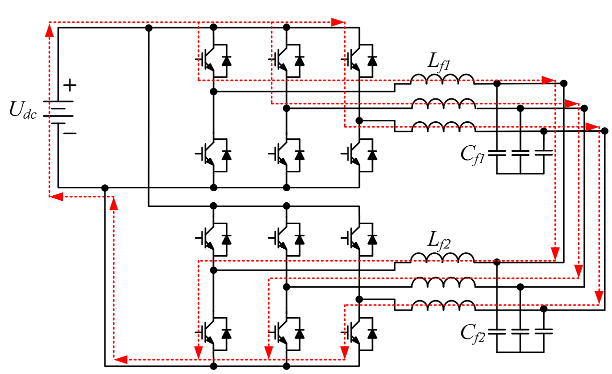
A. The Analysis of the Circulating Current

This paper takes a system of two parallel-connected VSIs for an example to analyze the circulating currents. The circulating currents can be classified into cross circulating current and zero-sequence circulating current, which will flow from one inverter to another through the common AC and DC buses [2]. Figure 2(a) shows the probably zero-sequence circulating current paths. Figure 2(b) shows the probably cross circulating current paths because of different switching states. According to literature [11], the cross circulating current I_{cir} can be defined as (1), in which I_1 and I_2 are the output currents of the parallel inverters. Considering the output impedances and assuming that the output impedances of the parallel inverters are equal to each other, then the cross circulating current can be calculated as (2). E_1 and E_2 are the output voltages of the two inverters, Z is the output impedance of the inverters. But in a practical system, the output impedances of each inverter will be different because of the different parameters of filters and line impedances or stray parameters. So virtual impedance can be used to modify the output impedance of the parallel inverters. The zero-sequence circulating current I_{zcir} can be calculated as (3), in which I_a, I_b and I_c are the three phase currents of the inverter [2], [5].

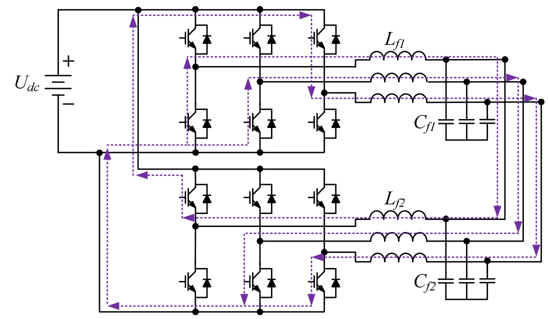
$$I_{cir} = (I_1 - I_2)/2 \tag{1}$$

$$I_{cir} = (E_1 - E_2)2Z \tag{2}$$

$$I_{zcir} = (I_a + I_b + I_c)/3 \tag{3}$$



(a)



(b)

Fig. 2. Circulating current paths. (a) Zero-sequence circulating current path. (b) Cross circulating current path.

B. The Proposed Control Strategy

Figure 3 shows the block diagram of the control architecture for one of the parallel three-phase VSIs, the other one VSI will use the same control principle. In the control architecture, droop control is used to generate the reference voltages, the virtual impedance is used to modify the output impedance of the inverters, and in order to increase the stability of the droop control, a secondary control is added to recover the output voltage. R_{v1} and L_{v1} are the virtual resistor and virtual inductor respectively. The proposed circulating current control loops are marked with purple line. The basic concept is to appropriately revise the reference currents from voltage control loop by sum of the error currents of d-axis, q-axis and zero-axis currents among the two parallel inverters which are named I_{dex}, I_{qex} and I_{zex}, x=1,2. With this compensation, new reference currents will be generated.

Take the generation of I_{dex} and I_{qex} for example, I_{zex} will use the same principle. I_{d1}, I_{q1}, I_{d2} and I_{q2} are the d-axis and q-axis currents from the Clark and Park transformation of the output currents I_{abc1}, I_{abc2} of VSI_1 and VSI_2 respectively. I_{dr1}, I_{qr1}, I_{dr2} and I_{qr2} are the reference currents from the outer voltage control loop. I_{dr1}*, I_{qr1}*, I_{dr2}* and I_{qr2}* are the new reference currents after compensation with the error current between the real output currents of VSI_1 and VSI_2. With formulas (4) and (5), the d-axis error current I_{de1} and q-axis error current I_{qe1} between VSI_1 and VSI_2 are obtained. Note that this calculation is in the controller of VSI_1, so I_{d1} and I_{q1} are in the position of dividend in (4) and (5). Then the error currents between I_{d1}, I_{d2}, I_{q1} and I_{q2} will be compared with 0 because if there is no cross circulating current among parallel inverters, the error currents I_{dex} and I_{qex} (x=1,2) will be 0, and the other one important purpose is to define the direction of the compensation. The gain "1/2" is from the cross circulating current calculation formula (1). And G_{oexs} (x=1,2) is the controller in the auxiliary current control loop.

For example, if currents $I_{d1}>I_{d2}$, the direction of compensation in the control loop should be decreasing reference I_{dr1} for VSI_1 and increasing I_{dr2} for VSI_2. Based on (4) and (6), the calculation results will be $I_{de1}<0$, $I_{de2}>0$. Institute (4) to (8), (6) to (10), compared with I_{dr1}, I_{dr2}, the new d-axis reference current I_{dr1}* will be decreased, and I_{dr2}* will be increased which indicates the right compensation direction. With proper controller design in the circulating current control

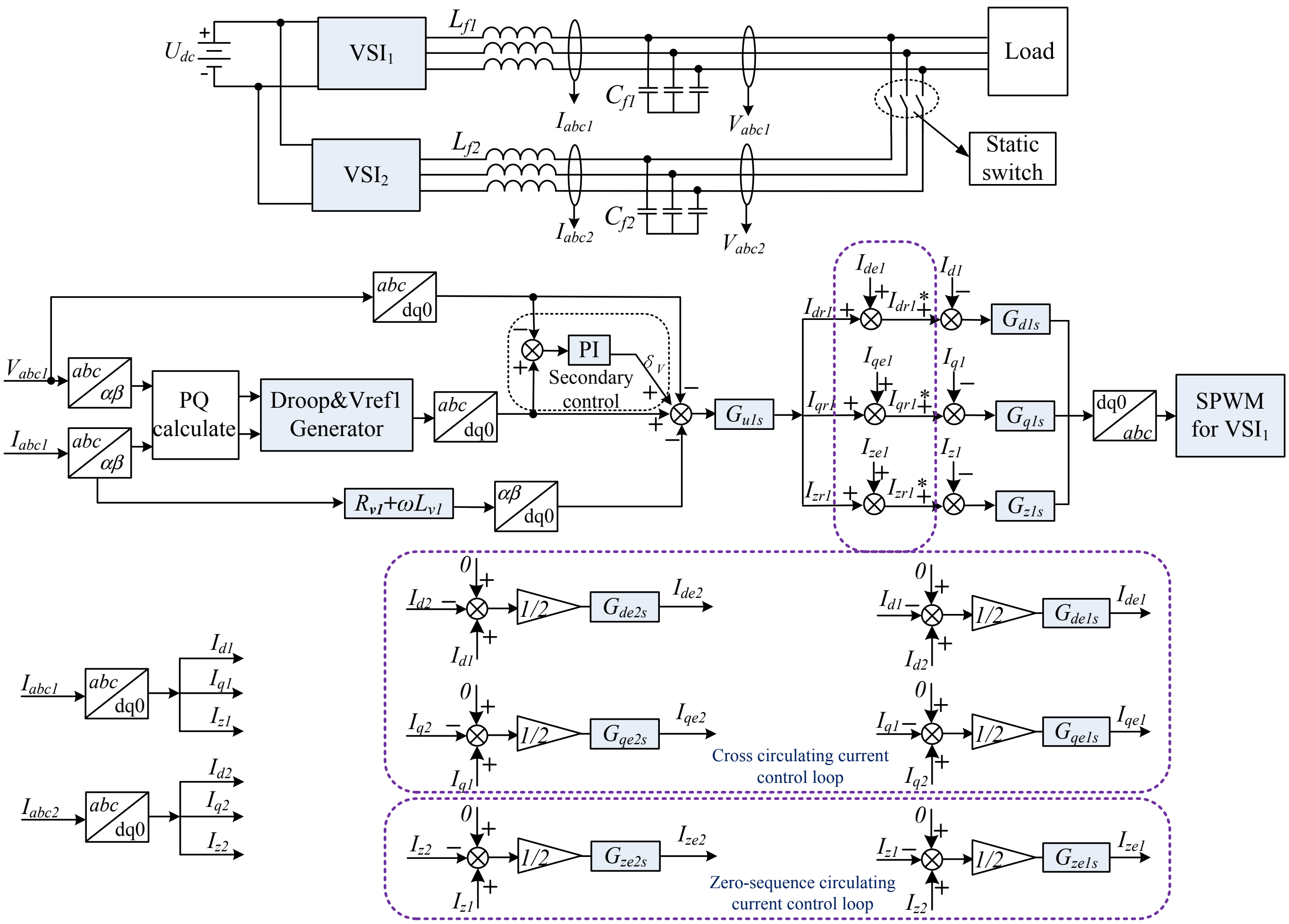


Fig. 3. The control architecture of parallel VSIs.

loops, both of the cross circulating current and the zero-sequence circulating current can be effectively suppressed.

$$[0-(I_{d1}-I_{d2})]/2=I_{de1} \tag{4}$$

$$[0-(I_{q1}-I_{q2})]/2=I_{qe1} \tag{5}$$

$$[0-(I_{d2}-I_{d1})]/2=I_{de2} \tag{6}$$

$$[0-(I_{q2}-I_{q1})]/2=I_{qe2} \tag{7}$$

$$I_{dr1}+I_{doff1}=I_{dr1}^{*} \tag{8}$$

$$I_{qr1}+I_{qoff1}=I_{qr1}^{*} \tag{9}$$

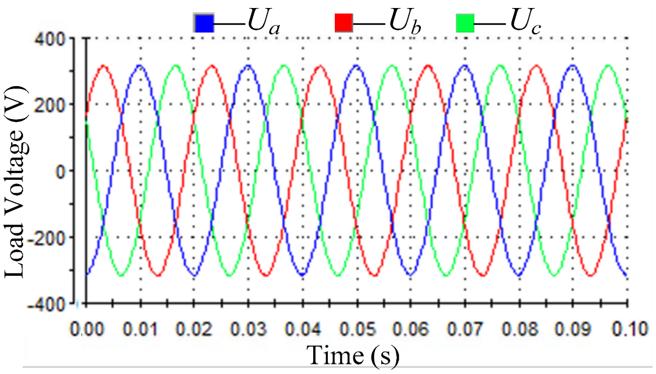
$$I_{dr2}+I_{doff2}=I_{dr2}^{*} \tag{10}$$

$$I_{qr2}+I_{qoff2}=I_{qr2}^{*} \tag{11}$$

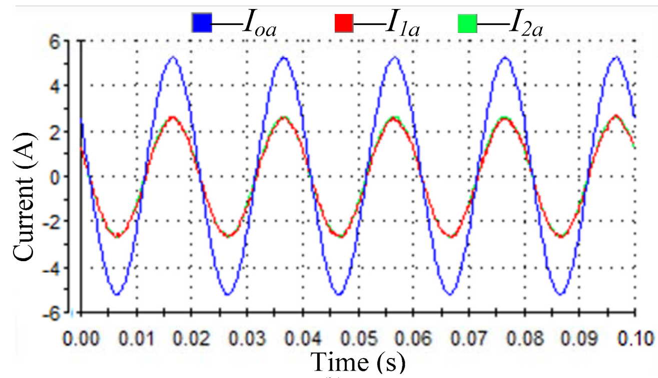
III. EXPERIMENTAL RESULTS

In order to verify the effectiveness of the proposed control strategy, experiments had been done with dSPACE 1006, using the proposed control strategy. Both of the linear and nonlinear loads were considered in the experiments. The nonlinear load was a rectifier connected with a resistor and a capacitor. The maximum phase voltage of the load is 325V. The experimental results with linear load are shown in Fig.4~Fig.6, and Fig.7~Fig.8 are the experimental results when nonlinear load is connected.

With the proposed control strategy, when the parallel VSIs supplied a linear load, the maximum value of the cross circulating current is about 50 mA, the number will be about 75mA for the zero-sequence circulating current. But without the proposed strategy, the maximum value will be more than 200 mA and 300mA for the cross and zero-sequence circulating currents respectively. If the parallel inverters were sharing a nonlinear load, the maximum value of the cross and zero-sequence circulating currents is about 75 mA and 100 mA respectively. But with the conventional droop and virtual impedance control, the maximum value of the cross circulating current is more than 200 mA, the number will be about 400mA for the zero-sequence circulating current. So compared with the conventional droop and virtual impedance control method, both of the cross circulating current and the zero-sequence circulating current can be effectively suppressed using the proposed control strategy with both linear and nonlinear loads. Therefore, a better average current-sharing performance is obtained.

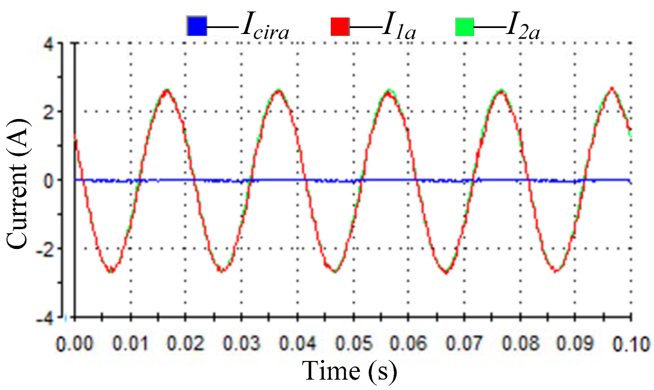


(a)

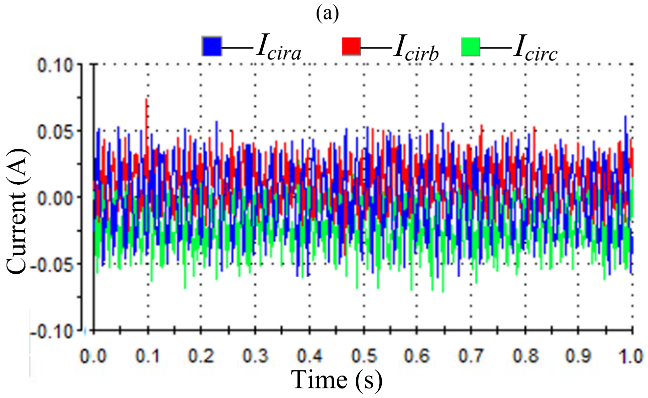


(b)

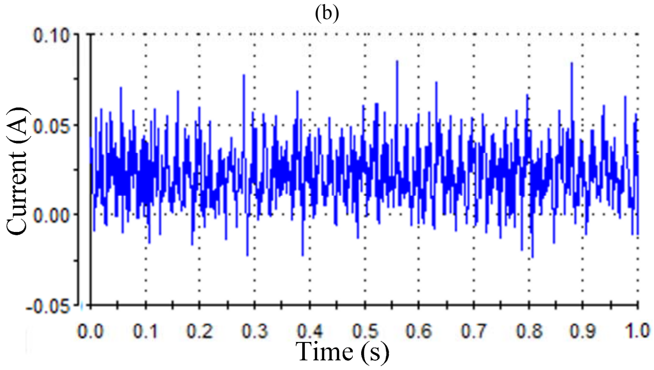
Fig.4. Experimental results with the proposed control strategy when linear load is connected. (a) Load voltage. (b) A phase currents of two inverters and the load.



(a)

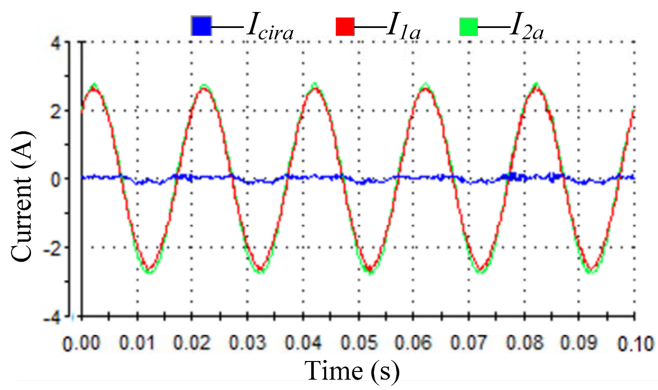


(b)

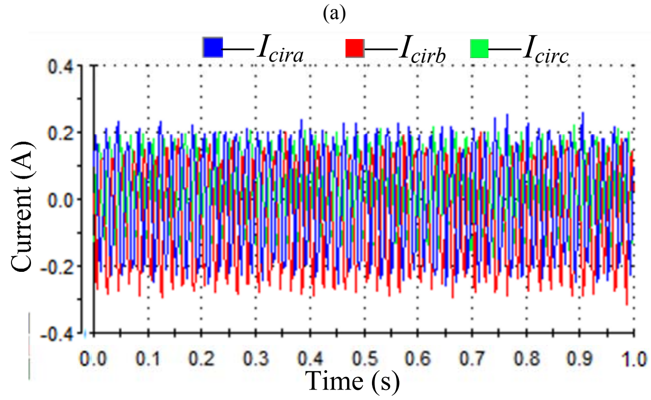


(c)

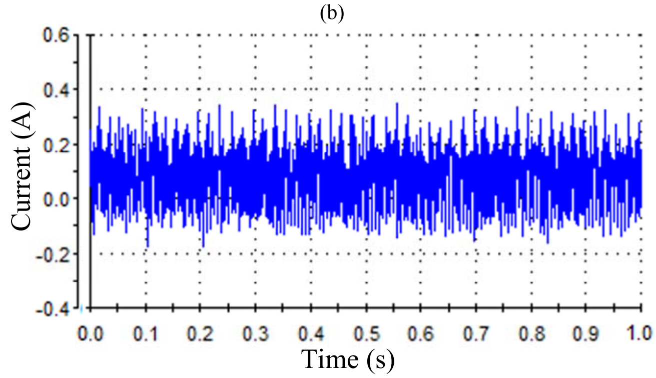
Fig.5. Experimental results with the proposed control strategy when linear load is connected.



(a)



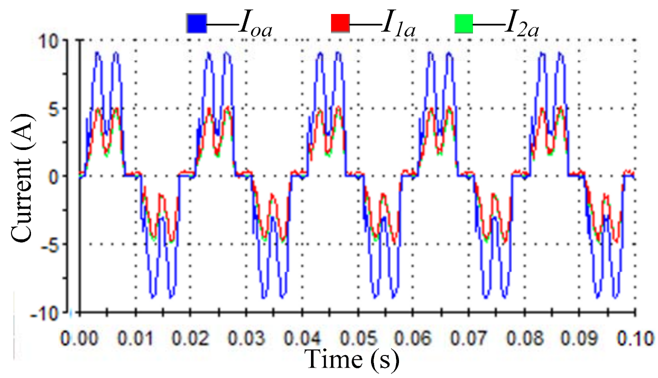
(b)



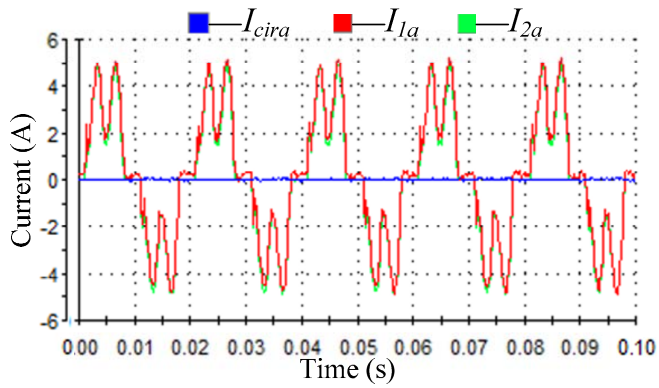
(c)

Fig.6. Experimental results without the proposed control strategy when linear load is connected.

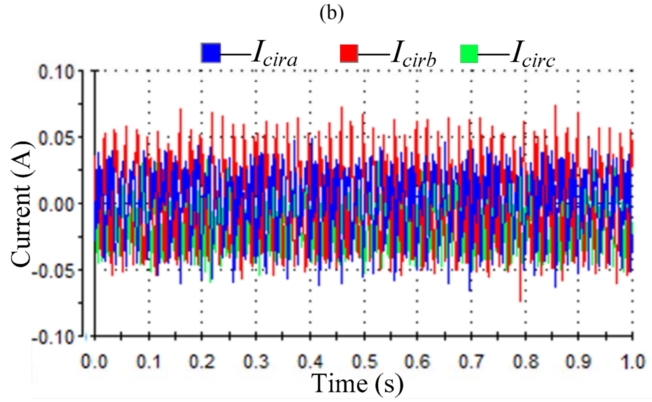
(a) The A phase currents and cross circulating currents among parallel VSIs. (b) The zoomed-in cross circulating current.
(c) The zero-sequence circulating current of VSI_1.



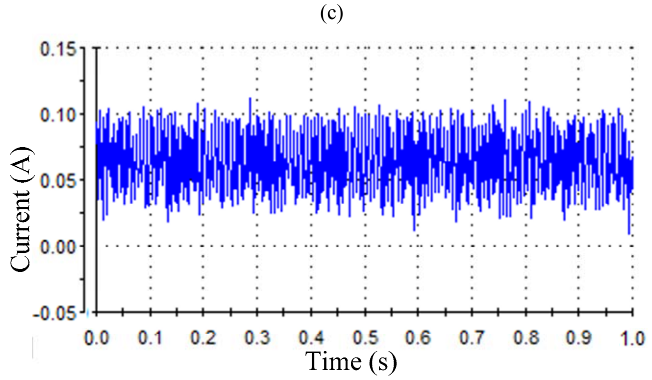
(a)



(b)

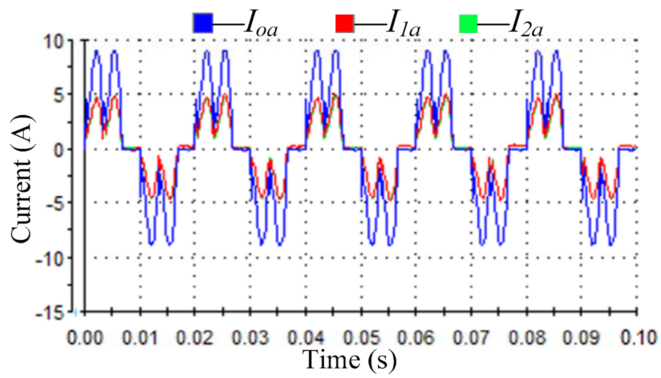


(c)

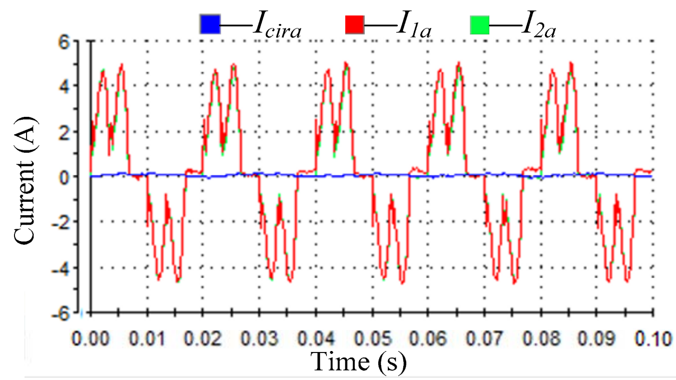


(d)

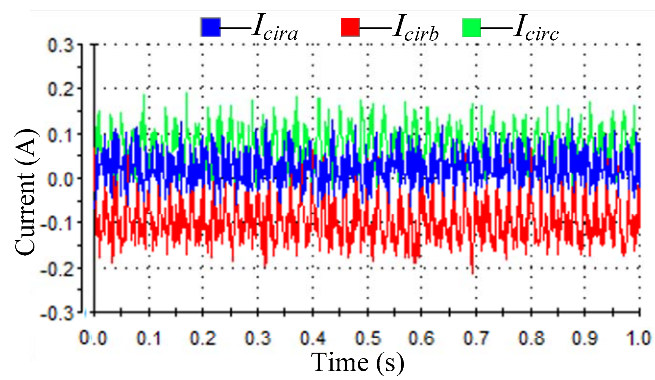
Fig.7. Experimental results with the proposed control strategy when nonlinear load is connected.



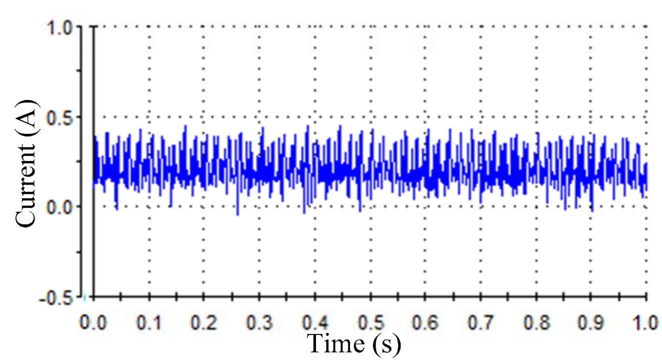
(a)



(b)



(c)



(d)

Fig.8. Experimental results without the proposed control strategy when nonlinear load is connected.

(a) The A phase currents of the load and the parallel VSIs. (b) The A phase currents and cross circulating currents among parallel VSIs. (c) The zoomed-in cross circulating current. (d) The zero-sequence circulating current of VSI_1.

IV. CONCLUSION

Parallel inverters are widely used for high power demand, and the average current-sharing scheme is necessary. A control strategy considering both of the cross circulating current and zero-sequence circulating current with droop and virtual impedance control is proposed in this paper. It combined the concept of droop control and the distributed control strategies. Experiments had been done when parallel-connected inverters were sharing linear or nonlinear loads. The results demonstrate that, both of the cross and zero-sequence circulating currents among the parallel VSIs can be effectively suppressed, then the average current-sharing is realized.

REFERENCES

[1] T. B. Lazzarin, G. A. T. Bauer, and I. Barbi, "A control strategy for parallel operation of single-phase voltage source inverters: Analysis, design and experimental result," IEEE Trans. Ind. Electron., vol. 60, no. 6, pp. 2194–2204, Jun. 2013.

[2] F. Wang, Y. Wang, Q. Gao, C. wang, and Y. liu, "A Control Strategy for Suppressing Circulating Currents in Parallel-Connected PMSM Drives With Individual DC Links," IEEE Trans. Power Electron., vol. 31, no. 2, pp. 1680-1691, Feb. 2016.

[3] D. C. Pham, S. Huang, and K. Huang, "Modeling and Simulation of Current Source Inverters with Space Vector Modulation," in Proc. IEEE ICEMS 2010, Oct. 10–13, pp. 320 - 325.

[4] Z. Bai, Z. Zhang, and X. Ruan, "A Natural Soft-Commutation PWM Scheme for Current Source Converter and Its Logic Implementation," IEEE Trans. Ind. Electron., vol. 58, no. 7, pp. 2772 - 2779, Jul. 2011.

[5] T. -P. Chen, "Zero-Sequence Circulating Current Reduction Method for Parallel HEPWM Inverters Between AC Bus and DC Bus," IEEE Trans. Ind. Electron., vol. 59, no. 1, pp. 290–300, Jan. 2012.

[6] J. M. Guerrero, J. Matas, L. G. Vicuna, M. Castilla, and J. Miret, "Wireless-control strategy for parallel operation of distributed-generation inverters," IEEE Trans. Ind. Electron., vol. 53, no. 5, pp. 1461–1470, Oct. 2006.

[7] Y. Zhang, M. Yu, F. Liu, and Y. Kang, "Instantaneous Current-Sharing Control Strategy for Parallel Operation of UPS Modules Using Virtual Impedance," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 432-440, Jan. 2013.

[8] J. M. Guerrero, L. G. Vicuna, J. Matas, M. Castilla, and J. Miret, "Output impedance design of parallel-connected UPS inverters with wireless load-sharing control," IEEE Trans. Ind. Electron., vol. 52, no. 4, pp. 1126–1135, Aug. 2005.

[9] J. He, and Y. Li, "Analysis, Design, and Implementation of Virtual Impedance for Power Electronics Interfaced Distributed Generation," IEEE Trans. Ind. Applica., vol. 47, no. 6, pp. 2525–2538, Nov. 2011.

[10] M. Prodanovic, T.C. Green, and H. Mansir, "Survey of control methods for three-phase inverters in parallel connection," IEEE Conference Publication (475) 472-477.

[11] H. Cai, R. Zhao, and H. Yang, "Study on Ideal Operation Status of Parallel Inverters," IEEE Trans. Power Electron., vol. 23, no. 6, pp. 2964–2969, Nov. 2008.