Effect of state feedback coupling on the transient performance of voltage source inverters with LC filter

Federico, de Bosio; Pastorelli, Michele; Antonio DeSouza Ribeiro, Luiz ; Freijedo Fernandez, Francisco Daniel; Guerrero, Josep M.

Published in:
Proceedings of 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), 2016

DOI (link to publication from Publisher):
10.1109/EPE.2016.7695497

Publication date:
2016

Document Version
Early version, also known as pre-print

Effect of state feedback coupling on the transient performance of voltage source inverters with LC filter

Federico de Bosio, Michele Pastorelli
Energy Department
Politecnico di Torino
Corso Duca degli Abruzzi, 24
10129 Torino, Italy
federico.debosio@polito.it
michele.pastorelli@polito.it

Luiz Antonio de Souza Ribeiro
Institute of Electrical Energy
Federal University of Maranhao
Av. Dos Portugueses, 1966
65072010 Sao Luis MA, Brazil
l.a.desouzaribeiro@ieee.org

Francisco Daniel Freijedo
Power Electronics Lab
École Polytechnique Fédérale de Lausanne
ELD 137, Station 11
1015 Lausanne, Vaud, Switzerland
francisco.freijedo@epfl.ch

Josep M. Guerrero
Institute of Energy Technology
Aalborg University
Pontoppidanstraede, 101/45
9200 Aalborg, Denmark
joz@et.aau.dk
www.microgrids.et.aau.dk

Acknowledgements

This work was supported in part by the CNPq/Brazil, CEMAR, and Schneider Electric.

Keywords

«Control system analysis», «Voltage control», «Current Control», «Power Quality».

Abstract

State feedback coupling between the capacitor voltage and inductor current deteriorates notably the performance during transients of voltage and current regulators in stand-alone systems based on voltage source inverters. A decoupling technique is proposed, considering the limitations introduced by system delays. Laboratory experiments were executed in compliance with the normative for Uninterruptible Power Supply systems to prove the developed analysis.

Introduction

A correct design of voltage and current loops allows to achieve acceptable performance of power converters. The design should achieve the best attainable performance during steady-state and transient conditions, without affecting the system stability. Poor dynamics of the inner loops is responsible for worse performance of the overall control system, independently of outer loops with reduced bandwidth. This problem can occur in microgrids with droop control and eventually secondary and tertiary control loops [1], and variable speed drives [2]. Thus, efficient voltage and current control is needed to positively implement the desired feature of each application. Based on [3], any current or voltage regulator should accomplish the following tasks: i) to achieve zero steady-state error; ii) accurately track the commanded reference during transients rejecting any disturbance; iii) have bandwidth as high as possible; iv) compensate for low order harmonics.

A possible design of regulators is based on a Proportional Resonant (PR) controller in the stationary reference frame. This structure corresponds to two Proportional Integral (PI) controllers, designed for the positive and negative sequence in the synchronous reference frame but implemented in stationary reference [4]. Since less transformations are required to reach the α- and β-axis reference frame, PR controller represents an interesting alternative for implementation in DSP units because of

its lower computational burden. Apart from the PR controller structure the effect of delays and coupling between the controlled states should be seriously addressed in the design stage.

Although valuable research has been developed for systems with a strong electromotive force, e.g. grid connected converters and drives applications, the isolated microgrid structure has not been analyzed in depth yet. Accordingly, as recently proved in [5], the coupling between the capacitor voltage and inductor current in VSI with LC output filter affects the performance of the inner regulators.

The following literature review is considered, but adapting those backgrounds to the scenario addressed (stand-alone application). In [6] the maximum allowed gains of PI and PR current regulators in the synchronous and stationary reference frames are derived analytically, considering the limitations introduced by computation and PWM delays, DC bus voltage and plant series inductance. In [7] several cascaded control structures using different feedback controlled states are compared. In [8] the authors perform a frequency-domain analysis of different PR controllers for current regulators intended for active power filters (APF), taking into account computation and PWM delays. In [9] a methodology based on the error signal transfer function roots is proposed to achieve fast and non-oscillating transient responses in grid-connected applications of PR current regulators. In [10], a current control scheme aimed to eliminate the inrush current occurring during the energizing phases of several load transformers has been proposed. Nevertheless, in the papers addressed, the effect and modelling of the delays for stand-alone applications have not been considered or partially analyzed.

The aim of this paper is to investigate the performance during transient conditions of voltage and current regulators for stand-alone applications taking into account the effect of voltage coupling and system delays in their design.

Physical System Modelling

In stand-alone applications the Voltage Source Inverter (VSI) is implemented with an LC filter at its output. In general, it works in voltage control mode with the capacitor voltage and inductor currents as controlled states. Fig. 1 shows the block diagram including a three-phase three-legs power converter with its inner loops. The inner current loop has to track the commands provided by the outer voltage loop while guaranteeing disturbance rejection within its bandwidth. Every time the current regulator is not able to perform properly these tasks the system performance deteriorates.

The block diagram representation of the physical system is shown in Fig. 2, where $\boldsymbol{V}^*_{c\alpha\beta} = V^*_{c\alpha} + jV^*_{c\beta}$ and $\boldsymbol{I}^*_{L\alpha\beta} = I^*_{L\alpha} + jI^*_{L\beta}$ are the reference phase voltage and current vectors and $\boldsymbol{I}_{o\alpha\beta} = I_{o\alpha} + jI_{o\beta}$ is the load current vector, which acts as a disturbance to the system. $G_i(s)$ and $G_v(s)$ represent the current and voltage regulators transfer functions (TF), $G_{pwm}(s)$ is the TF used to represent computation and PWM delays, while $G_{dec}(s)$ is the TF related to the decoupling of the controlled states. The capacitor $C_f = 3C$ is the equivalent capacitance in a Y connection configuration.

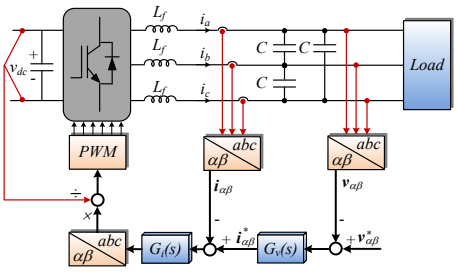


Fig. 1. Block diagram of a three phase VSI with voltage and current loops

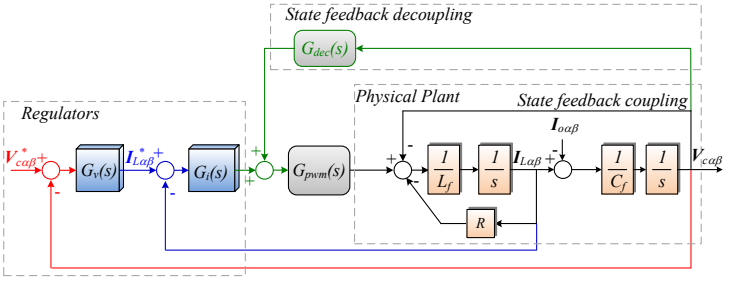


Fig. 2. Simplified block diagram of the closed loop system

Design of Voltage and Current Regulators

Since voltage and current regulators are built in a cascade control configuration, serial tuning can be used for design purposes. For this reason, the loop characterized by the fastest dynamics is the first to be designed according to the system requirements [11].

Current regulator design

The proportional gain of the current regulator was selected to achieve the desired bandwidth (f_{bw}), which has to be much faster than the outer loops [12]. For the design of the regulator bandwidth, a common assumption is to neglect the computation and PWM delays. However, the error introduced by this assumption could be very large depending on the delay ($e^{-T_d s}$) and its approximation, and on the chosen bandwidth as well. A first order Padé approximation is the common choice. There are at least two different ways to approximate it: 1) $e^{-T_d s} \cong 1/(1+T_d s)$; 2) $e^{-T_d s} \cong [1-(T_d/2)s]/[1+(T_d/2)s]$. As shown in Fig. 3, the second expression preserves the magnitude, and for frequencies up to $0.1 f_s$, being f_s the switching frequency, the phase difference becomes negligible. Therefore, the second approach is more appropriated to design the regulator. Furthermore, the non-minimum phase zero presented is useful to understand how the system can become unstable when the regulator bandwidth increases [13]. Considering the value of the delay used in this application ($T_d = 1.5/f_s$), and the bandwidth chosen for the inner loop ($f_{bw} \cong 1\ kHz$), the gain difference, including or neglecting the delay model, is more than 25%, which proves its importance in the tuning.

The system and control parameters used both in the simulation and in laboratory tests are presented in Table I, Table II and Table III.

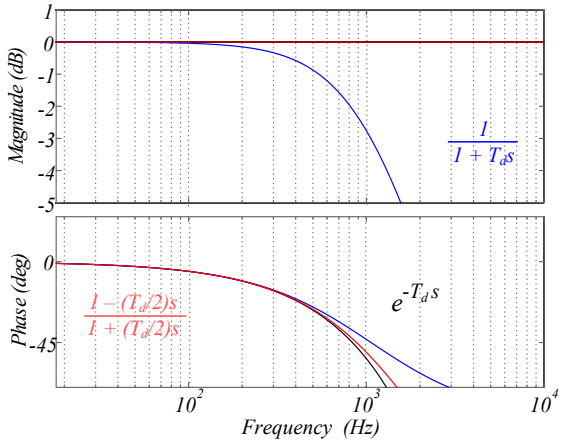


Fig. 3. Frequency response of the delay and its Padè approximations : $T_d = 1.5/f_s$

Table I. System parameters

Parameter	Value
Switching frequency	$f_s = 10\ kHz$
Filter inductance	$L_f = 1.8\ mH$
Filter capacitor	$C_f = 27\ \mu F$
Inductor ESR	$R = 0.1\ \Omega$
Linear load	$R_l = 68\ \Omega$
Nonlinear load	$C_{NL} = 235\ \mu F$ $R_{NL} = 155\ \Omega$ $L_{NL} = 0.084\ mH$

Table II. Current Regulator Control Parameters

Parameter	Value
Proportional gain w/o voltage decoupling	$k_{pI} = 5.61$
Proportional gain with voltage decoupling	$k_{pI} = 6.42$

Table III. Voltage Regulator Control Parameters

Parameter	Value
Proportional gain	$k_{pV} = 0.05$
Integral gain @50Hz	$k_{iV} = 31.47$
Integral gain @250Hz	$k_{iVh5} = 15$
Integral gain @350Hz	$k_{iVh7} = 15$

By neglecting the computation and PWM delays, it can be noticed from the root locus in Fig. 4(a) that as the gain is increased, higher damping is achieved. This is in contradiction with the results where

system delays are included for analysis. According to Fig. 4(b), it can be observed that if the inductor current and capacitor voltage are not decoupled ($G_{dec}(s)$ in Fig. 2 neglected) and computation and PWM delays are taken into account, the system is always lightly damped with a high overshoot independently of the gain. In detail are the closed loop poles for the desired bandwidth of 1 kHz. If ideal voltage decoupling is performed [see Fig. 4(c)], the open loop poles are real and higher damping is achieved for the same bandwidth (1 kHz).

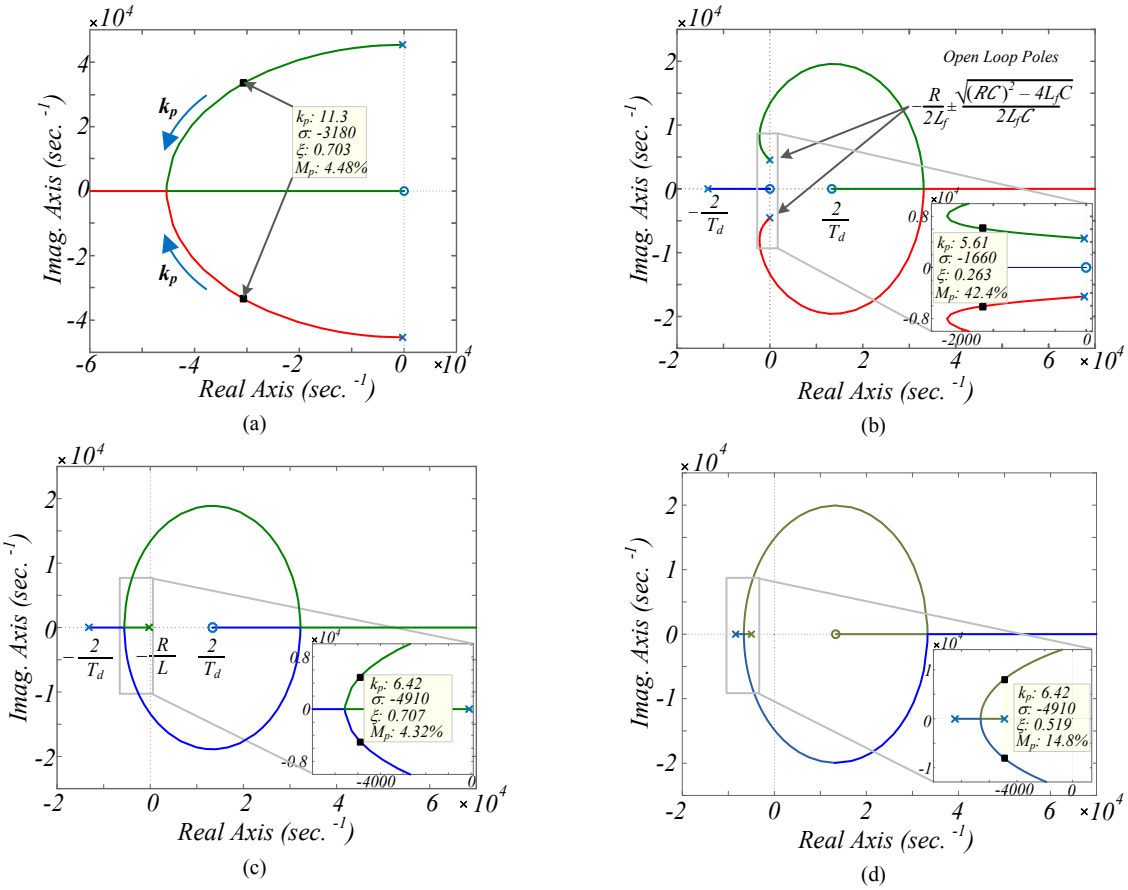


Fig. 4. Root locus of a P controller for the current loop: (a) without decoupling and neglecting system delays; (a) without decoupling; (b) with ideal decoupling [$G_{dec}(s) = G_{PWM}(s)^{-1}$]; (c) with non-ideal decoupling [$G_{dec}(s) = 1$]

However, ideal voltage decoupling implies to design $G_{dec}(s) = G_{PWM}(s)^{-1}$. This implementation is not feasible whatever approximation for $G_{PWM}(s)$ is used. In fact, if the approximation with a zero on the right half plane is selected, $G_{PWM}(s)^{-1}$ is an unstable TF. Similarly, the inverse of the approximation based on the low-pass filter results in a derivative term.

By choosing $G_{dec}(s) = 1$, the system delays on the state feedback decoupling path are not compensated for. This approach is referred to in this paper as non-ideal decoupling. Compared to ideal voltage decoupling [see Fig. 4(c)] the damping of the system degrades [see Fig. 4(d)] for the same proportional gain. However, the damping is still much higher than without voltage decoupling [see Fig. 4(b)].

Fig. 5(a) and Fig. 5(b) show the frequency response (FR) analysis of the current loop only. The system depends on the load impedance if the controlled states are coupled or not ideally decoupled. The arrow refers to increase in the load impedance, until open-circuit conditions (no load). As the states are coupled [see Fig. 5(a)], a low gain for a broad frequency range including rated frequency (50 Hz) is observed, which means the reference is not accurately tracked. On the contrary, if the states are ideally decoupled, the system is not dependent on the load and approximately zero steady-state error is produced. This low steady-state error is determined by the inductor ESR value. In Fig. 5(b) the FR with non-ideal voltage decoupling is reported. The system is still load dependent, but to a much lesser degree

than without decoupling. Consequently, due to these interesting characteristics, voltage decoupling is implemented for the inner current loop.

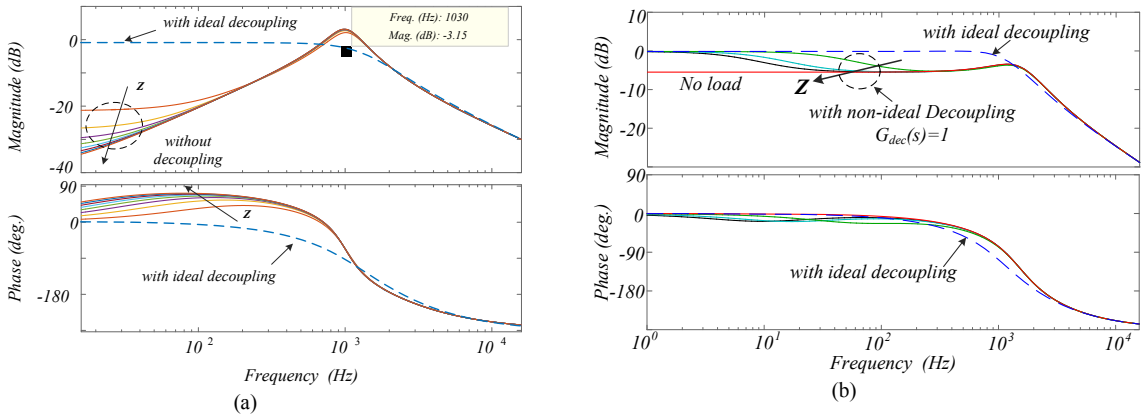


Fig. 5. Frequency response of the current loop only with a P controller as current regulator: (a) with ideal decoupling and w/o decoupling; (b) with ideal and non-ideal decoupling

Voltage regulator design

The voltage loop is designed for a bandwidth roughly one tenth of the one selected for the current loop. A PR regulator with a lead compensator structure is employed as

$$G_v(s) = k_{pV} + \sum_{h=1,5,7} k_{iV,h} \frac{s\cos(\varphi_h) - h\omega_1 \sin(\varphi_h)}{s^2 + (h\omega_1)^2}, \tag{1}$$

where h is the harmonic order, φ_h the leading angle at each harmonic frequency and k_{pV} the proportional gain of the voltage loop. This latter settles the bandwidth of the voltage regulator, designed for about 150 Hz.

The procedure proposed in [14] is applied to determine the voltage regulators gains. The leading angles are selected such that the trajectories of the open loop system on the Nyquist diagram, with the PR regulators at fundamental, 5th and 7th harmonic frequency, ensure a sensitivity peak η higher than a threshold value. In this analysis the threshold has been set to $\eta = 0.5$ at no-load condition. This constraint is verified, as shown in Fig. 6.

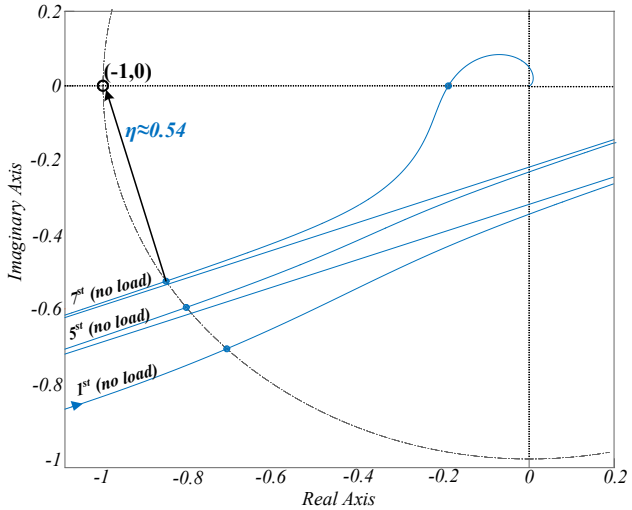


Fig. 6. Nyquist diagram of the system at no-load conditions

After calculating the leading angles, the fundamental resonant gain is chosen to promptly react to changes in the fundamental component, without affecting system stability. To this extent, (1) is rearranged for the resonant controller at fundamental, leading to

$$G_v(s) = k_{pV}\frac{s^2 + \frac{k_{iV,1}}{k_{pV}}\cos(\varphi_1)s + \left[\omega_1^2 - \frac{k_{iV,1}}{k_{pV}}\omega_1\sin(\varphi_1)\right]}{s^2 + \omega_1^2}. \quad (2)$$

The zeros of the PR controller in (2) are moved as furthest as possible from the right half plane to be coincident on the real axis. This implies to select $k_{iV,1}$ according to

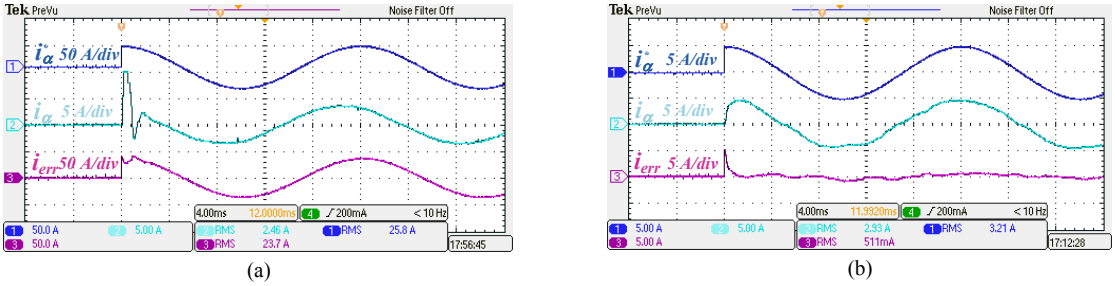
$$k_{iV,1} \geq K\frac{2k_{pV}\omega_1}{\cos(\varphi_1)}, \quad (3)$$

where the lower bound of the inequality corresponds to $K = 1$. For the leading angle at fundamental frequency $\varphi_1 = 3.3°$, the minimum gain is $k_{iV,1} = 31.47$. This value is set as integral gain. The harmonic resonant gains are chosen to reduce the post-fault oscillations [9] while complying with the standards imposed by the standards for UPS systems as well.

Experimental Results

The theoretical analysis developed is verified with reference to the power system shown in Fig. 1. To this extent, a laboratory prototype has been built using a 2.2 kW power converter, controlled by a dSpace platform. A 16-bits resolution Digital-to-Analog conversion board has been used to record data on an oscilloscope. The main system parameters are summarized in Table I. The regulators are implemented via Impulse Invariant as discretization method for the resonant terms.

For what concerns the current loop only, a step in the reference inductor current is performed. Without decoupling the controlled states, because of the low gain for a broad frequency range [see Fig. 5(a)] a high reference current must be provided to achieve the rated inductor current. However, the initial current during transient is too high and the inverter current protections activate. In order to record step response captures without voltage decoupling, a lower reference current is imposed. In Fig. 7(a) it can be seen the higher initial current respect to steady-state value because of low damping achieved without voltage decoupling. With reference to the decoupling of the controlled states the step response is much more damped and the reference current is in the order of magnitude of the rated inductor current [see Fig. 7(b)]. From this analysis, it can be concluded that just a P controller can be implemented in the inner current loop, but only if voltage decoupling is performed. It must be noted that the use of a P controller is possible only if an outer voltage loop with an integration action (PI or PR) is used to correct steady state errors in the outer loop.

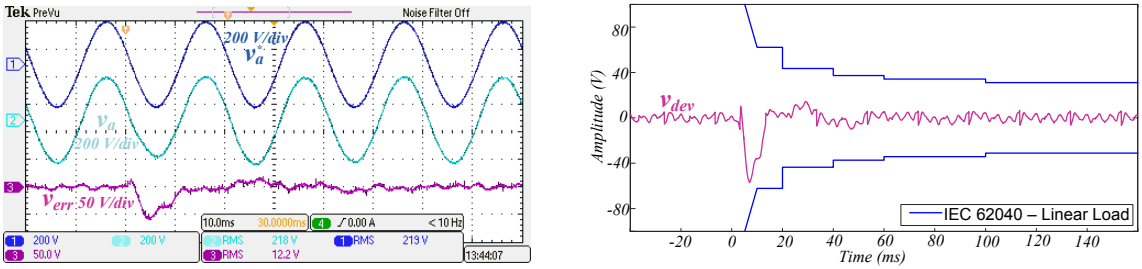


(a) (b)

Fig. 7. Step response of the reference inductor current, time scale (4 ms/div): (a) without voltage decoupling, reference (50 A/div), real (5 A/div) and inductor current error (50 A/div) (α-axis); (b) with voltage decoupling, reference (5 A/div), real (5 A/div) and inductor current error (5 A/div) (α-axis)

The results from Fig. 8 to Fig. 10 relative to the voltage loop are performed with voltage decoupling and a P controller as current regulator. In Fig. 8(a) the results of a linear step load changing from 0% to 100% are reported. In Fig. 8(b) the deviations of the real capacitor voltage from the reference are compared to the envelope of the voltage deviation according to the IEC 62040 standard for UPS

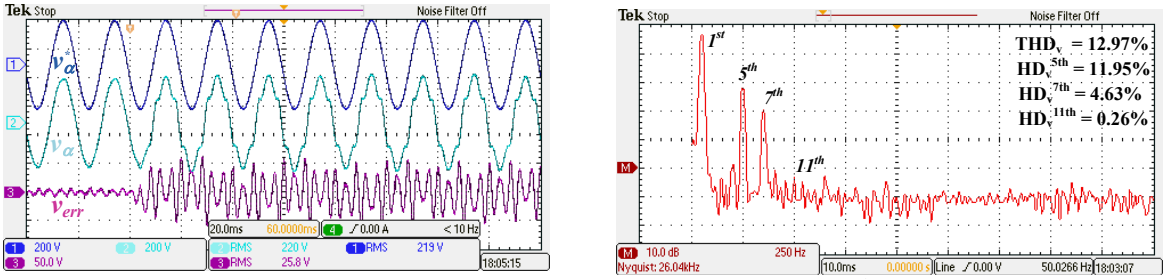
systems. It can be observed that the capacitor voltage reaches steady-state in less than half a cycle after the step load changing. The dynamics response is within the limits required by the standard.



(a) (b)

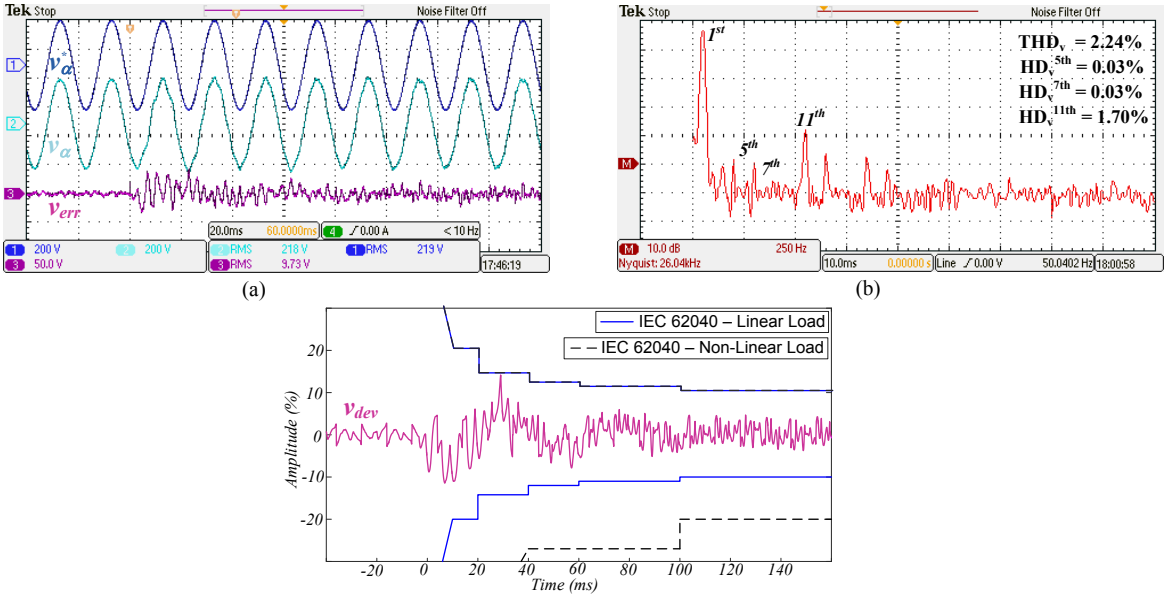
Fig. 8. Linear step load changing (0 – 100%): (a) reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis), time scale (10 ms/div); (b) Dynamic characteristics according to IEC 62040 standard for linear loads, capacitor voltage deviation

A diode bridge rectifier with an LC output filter supplying a resistive load is selected as nonlinear load. Its parameters are summarized in Table I. A nonlinear step load change from 0% to 100% is performed without (Fig. 9) and with harmonic compensators (HC) tuned at 5th and 7th harmonics (Fig. 10).



(a) (b)

Fig. 9. Voltage loop without HC and nonlinear load: (a) Step load changing (0 - 100%), reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis), time scale (20 ms/div); (b) FFT of the capacitor voltage (250 Hz/div)



(a) (b)

(c)

Fig. 10. Voltage loop with 5th, 7th HC and nonlinear load: (a) Step load changing (0 - 100%), reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis), time scale (20 ms/div); (b) FFT of the capacitor voltage (250 Hz/div); (c) Dynamic characteristics according to IEC 62040 standard for linear loads, capacitor voltage deviation

The results with the HC activated comply with the IEC 62040 standard, as shown in Fig. 10(c). From the FFT analysis it can be observed the compensation of the harmonics to which the resonant controllers have been tuned. Nevertheless, some small augmentation of higher order harmonics can be seen in the frequency spectrum, specifically the 11^{th} harmonic. This can be understood as the resonant peaks can marginally influence close harmonic orders.

Conclusion

In this paper the effect of state feedback decoupling on the performance of current and voltage regulators for stand-alone applications has been analyzed. As the controlled states are decoupled, higher damping of the system with less overshoot is achieved. System delays are the main factors which limit the bandwidth that can be achieved by the current regulator and consequently by the voltage loop. The system dynamics is independent of the load impedance when the capacitor voltage is decoupled ideally, allowing a proportional controller to be used as current regulator.

References

[1] J. C. Vasquez, J. M. Guerrero, M. Savaghebi, J. Eloy-Garcia, and R. Teodorescu, "Modeling, Analysis, and Design of Stationary-Reference-Frame Droop-Controlled Parallel Three-Phase Voltage Source Inverters," *IEEE Trans. Ind. Electron.,* vol. 60, no. 4, pp. 1271-1280, 2013.

[2] K. Hongrae, M. W. Degner, J. M. Guerrero, F. Briz, and R. D. Lorenz, "Discrete-Time Current Regulator Design for AC Machine Drives," *IEEE Trans. Ind. Appl.,* vol. 46, no. 4, pp. 1425-1435, 2010.

[3] T. M. Rowan and R. J. Kerkman, "A New Synchronous Current Regulator and an Analysis of Current-Regulated PWM Inverters," *IEEE Trans. Ind. Appl.,* vol. IA-22, no. 4, pp. 678-690, 1986.

[4] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid Converters for Photovoltaic and Wind Power Systems*: Wiley-IEEE Press, 2011.

[5] F. de Bosio, L. A. de S. Ribeiro, M. S. Lima, F. Freijedo, J. M. Guerrero, and M. Pastorelli, "Current control loop design and analysis based on resonant regulators for microgrid applications," in *IEEE Conf. Rec. IECON*, Yokohama, Japan, 2015, pp. 5322 - 5327.

[6] D. G. Holmes, T. A. Lipo, B. P. McGrath, and W. Y. Kong, "Optimized Design of Stationary Frame Three Phase AC Current Regulators," *IEEE Trans. Power Electron.,* vol. 24, no. 11, pp. 2417-2426, 2009.

[7] L. Poh Chiang and D. G. Holmes, "Analysis of multiloop control strategies for LC/CL/LCL-filtered voltage-source and current-source inverters," *IEEE Trans. Ind. Appl.,* vol. 41, no. 2, pp. 644-654, 2005.

[8] R. Bojoi, L. R. Limongi, D. Roiu, and A. Tenconi, "Frequency-domain analysis of resonant current controllers for active power conditioners," in *IEEE Conf. Rec. IECON*, Orlando, FL, USA, 2008, pp. 3141-3148.

[9] A. Vidal, F. D. Freijedo, A. G. Yepes, P. Fernandez-Comesana, J. Malvar, O. Lopez*, et al.*, "Assessment and Optimization of the Transient Response of Proportional-Resonant Current Controllers for Distributed Power Generation Systems," *IEEE Trans. Ind. Electron.,* vol. 60, no. 4, pp. 1367-1383, 2013.

[10] S. S. H. Bukhari, T. A. Lipo, and K. Byung-Il, "An on-line UPS system that eliminates the inrush current phenomenon while feeding multiple load transformers," in *IEEE Conf. Rec. ICPE-ECCE Asia*, Seoul, Korea, 2015, pp. 385-390.

[11] K. J. Aström and T. Hägglung, PID Controllers: Theory, Designing, and Tuning, 2nd ed., Research Triangle Park, NC, USA: Instrument Society of America, 1995. 2006.

[12] F. Briz, M. W. Degner, and R. D. Lorenz, "Analysis and design of current regulators using complex vectors," *IEEE Trans. Ind. Appl.,* vol. 36, no. 3, pp. 817-825, 2000.

[13] A. G. Yepes, F. D. Freijedo, O. Lopez, and J. Doval-Gandoy, "Analysis and Design of Resonant Current Controllers for Voltage-Source Converters by Means of Nyquist Diagrams and Sensitivity Function," *IEEE Trans. Ind. Electron.,* vol. 58, no. 11,pp. 5231-5250, 2011.

[14] F. de Bosio, L. A. de S. Ribeiro, F. D. Freijedo, M. Pastorelli, and J. M. Guerrero, " Effect of state feedback coupling and system delays on the transient performance of stand-alone VSI with LC output filter," *IEEE Trans. Ind. Electron.,* Early Access, 2016.