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Enhancement of Current and Voltage Controllers Performance by Means of Lead Compensation and Anti-Windup for Islanded Microgrids

Federico de Bosio[1], Luiz A. de S. Ribeiro[2], Francisco D. Freijedo[3], Josep M. Guerrero[4], Michele Pastorelli[1]
[1]Energy Department, Politecnico di Torino, 10129 Torino, Italy
[2]Institute of Electrical Energy, Federal University of Maranhao, 65072010 Sao Luis MA, Brazil
[3]Power Electronics Lab, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Vaud, Switzerland
[4]Department of Energy Technology, Aalborg University, 9200 Aalborg, Denmark www.microgrids.et.aau.dk

***Abstract*— The decoupling of the capacitor voltage and inductor current has been shown to improve significantly the dynamics performance of voltage source inverters in isolated microgrids. However, still the computation and PWM delays limit the achievable bandwidth. A technique based on a lead compensator structure is proposed to overcome this limitation. It is shown how a widen bandwidth for the current loop with still well damped characteristics allows to enlarge the outer voltage loop bandwidth. These features are demanding requirements in high performance islanded applications. Discrete-time domain implementation issues of an anti-wind up scheme are discussed as well. In fact, algebraic loops can arise if the wrong discretization method is used making unfeasible the real-time implementation of digital controllers. Experimental tests in accordance with the standards for UPS systems verify the theoretical analysis.**

***Index Terms*— Control system analysis, current control, microgrids, power quality, voltage control**

I. INTRODUCTION

THE design of voltage and current regulators for Voltage Source Inverters (VSI) should aim to achieve good performance during steady-state and transient conditions, which means allow the system to work with wide stability margins. Poor dynamics of these regulators is responsible for degraded performance of the overall control system, independently of outer loops with slower dynamics. Thus, effective control of voltage and current is mandatory to succeed in implementing the desired feature of each application. According to [1], it is desirable from any current or voltage regulator the following: i) to achieve zero steady-state error; ii) accurately track the commanded reference during transients rejecting any disturbance; iii) have bandwidth as wider as possible; iv) compensate for low order harmonics.

A possible design of voltage or current regulators employs a Proportional Resonant (PR) controller in the $\alpha\beta$ stationary reference frame. This structure is equivalent to two Proportional Integral (PI) controllers, one for the positive and the other for the negative sequence in the synchronous reference frame [2]. Independently of the controller structure the effect of delays and voltage coupling should be carefully considered in the design stage [3].

Even though substantial research has been done in systems with a strong electromotive force (e.g. grid connected and drives applications), the isolated microgrid structure has not been so far discussed in depth. In this context, as proved in a recent publication [4], the coupling between the capacitor voltage and inductor current in VSI with LC output filter degrades the dynamics of the inner regulators.

The aim of this paper is to analyze the performance of voltage and current regulators for isolated microgrids during transient, with respect to the effect of voltage coupling between the inductor current and capacitor voltage as well as computation and PWM delays in their design. A control method based on a lead compensator structure is proposed in order to improve the dynamics performance of the current regulator. As a consequence, the bandwidth of the voltage regulator can be widen allowing to achieve a better system dynamics. Its design is based on the Nyquist criterion taking into account the previous design of the current loop. Moreover, discretization issues of an anti-wind up scheme for the voltage regulator based on the inverse of its control structure on a feedback path are analyzed. This technique allows to drive the states with bounded signals in any condition, i.e. also during demanding transients. This represents a major advantage compared to usual anti-wind up implementations, e.g. the frozen scheme [5]. Finally, the solutions proposed are verified experimentally according to the requirements imposed by IEC 62040 standard to Uninterruptible Power Supply (UPS) systems.

II. SYSTEM DESCRIPTION

In isolated microgrids the VSI is implemented with an LC filter at its output. In general, it operates in voltage control mode with the capacitor voltage and inductor currents being the controlled states.

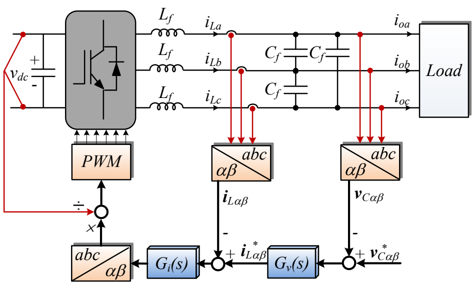

Fig. 1. Block diagram of a three phase VSI with voltage and current loops

In Fig. 1 the block diagram including a three-phase inverter with its regulators is presented. The aim of the inner current loop is to track the commands from the outer voltage loop and to ensure fast dynamic disturbance rejection within its bandwidth [4]-[7].

The simplified block diagram of the closed-loop system is shown in Fig. 2, where $\boldsymbol{V}_{c\alpha\beta}^{*}$ and $\boldsymbol{I}_{L\alpha\beta}^{*}$ are the reference voltage and current vectors and $\boldsymbol{I}_{o\alpha\beta}$ is the output current vector, which acts as a disturbance to the system. $G_i(z)$ and $G_v(z)$ represent the current and voltage regulators transfer functions (TF) in the discrete-time domain. There is one sample computational delay due to the implemented regular sample symmetrical PWM strategy [8]. $G_{dec}(z)$ is the TF related to the decoupling of the cross-coupling states, designed to compensate for the system delay within the current controller bandwidth.

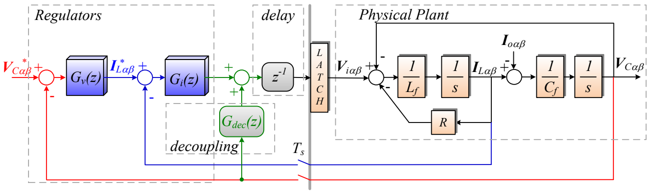

Fig. 2. Simplified block diagram of the closed-loop system

III. CURRENT REGULATOR DESIGN

The proportional gain k_{pI} of the current regulator is selected to achieve the desired bandwidth (f_{bw}), which has to be much wider than the outer loops [9]. No resonant filters are needed. In fact, using just simple proportional based structures allows to enlarge the bandwidth with practical small bad effects on the average error. However, as k_{pI} is increased the steady-state error reduces significantly.

The physical and control parameters used both in the simulation and in laboratory tests are presented in Table I and Table II.

TABLE I
SYSTEM PARAMETERS

Parameter	Value
Switching frequency	$f_s = 10\ kHz$
Filter inductance	$L_f = 1.8\ mH$
Filter capacitor	$C_f = 27\ \mu F$
Inductor ESR	$R = 0.1\ \Omega$
Linear load	$R_l = 68\ \Omega$
Nonlinear load	$C_{NL} = 235\ \mu F$ $R_{NL} = 184\ \Omega$ $L_{NL} = 0.084\ mH$

TABLE II
CURRENT REGULATOR PARAMETERS

Parameter	Value
Proportional gain w/o lead	$k_{pI} = 6.42$
Proportional and lead gains @ω_n = 4000π rad/s	$\begin{cases} k_{pI} = 11.56 \\ k_L = 0.475 \end{cases}$
Proportional and lead gains @ω_n = 6000π rad/s	$\begin{cases} k_{pI} = 16.82 \\ k_L = 0.868 \end{cases}$

As voltage decoupling is performed, higher damping is achieved with less overshoot for a given bandwidth. Moreover, the system becomes not dependent on the load impedance and almost zero steady-state error can be achieved even with a simple P controller [4]. For this reason, the design of the current controller is based on the decoupled system. As a first approximation and ease of design, the decoupling of the capacitor voltage is considered to be ideal. This means $G_{dec}(z)$ is supposed to be designed such that computation and PWM delays are compensated for on the decoupling path. A simple P controller and a RL load modelled in the discrete-time domain are considered [10], as shown in the block diagram of Fig. 3. This simplified model of the physical plant can be used because, decoupling ideally the controlled states, determines no dependence on the load.

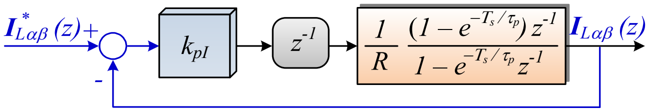
$I_{L\alpha\beta}^{*}(z)$
+
-
k_{pI}
z^{-1}
$\frac{1}{R}\ \frac{(1-e^{-T_s/\tau_p})\,z^{-1}}{1-e^{-T_s/\tau_p}z^{-1}}$
$I_{L\alpha\beta}(z)$

Fig. 3. Model of a RL load including the lag introduced by PWM update, with time constant $\tau_p = L_f/R_f$

The closed-loop TF of the inner current loop system in Fig. 3 is:

$$\frac{I(z)}{I^{*}(z)} = \frac{k_{pI}b}{z^2 - az + k_{pI}b}, \tag{1}$$

where $b = (1 - e^{-T_s/\tau_p})/R;\ a = e^{-T_s/\tau_p}$.

For the system parameters in Table I, the root locus is shown in Fig. 4. It can be stated that, because of the delay, there is a limitation in the gain to achieve a system with enough damping. There are two poles and just one variable (k_{pI}) that can change their locations. It is clear that it is not possible to place the roots at any desired location. The designed gain to achieve a damping of $\xi = 0.707$ is $k_{pI} = 6.09$, as presented in Table II.

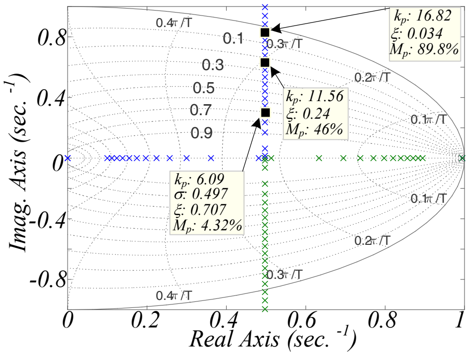

Fig. 4. Root locus of RL load including the lag introduced by PWM update

To increase the system bandwidth and still achieve a reasonable damped closed-loop system, it is possible to design a lead compensator as shown in Fig. 5, also referred to as ‘Delay prediction and Feedback’ [5].

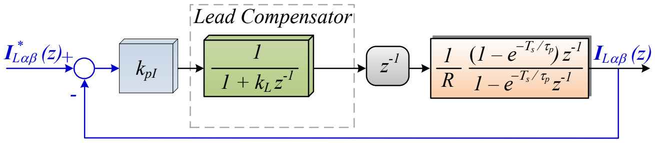
Lead Compensator
$I_{L\alpha\beta}^{*}(z)$
+
-
k_{pI}
$\frac{1}{1+k_L z^{-1}}$
z^{-1}
$\frac{1}{R}\ \frac{(1-e^{-T_s/\tau_p})\,z^{-1}}{1-e^{-T_s/\tau_p}z^{-1}}$
$I_{L\alpha\beta}(z)$

Fig. 5. Model of RL load including the lag introduced by PWM update, with the model of the lead compensator $G_L(z) = 1/(1 + k_L z^{-1})$

The closed-loop TF becomes

$$\frac{I(z)}{I^*(z)} = \frac{k_{pI}b}{(z+k_L)(z-a)+k_{pI}b}. \tag{2}$$

The poles of this TF must satisfy the following relationship

$$\begin{aligned} z^2-(p_1+p_2)z+p_1p_2 \\ = z^2+(k_L-a)z-k_La+k_{pI}b, \end{aligned} \tag{3}$$

where p_1, p_2 are the desired pole locations, defined as

$$p_{1,2} = e^{-\xi\omega_n T_s}[\cos(\omega_d T_s) \pm j\sin(\omega_d T_s)], \quad \omega_d = \omega_n\sqrt{1-\xi^2}$$

Solving the system leads to

$$\begin{cases} k_L = a-(p_1+p_2) \\ k_{pI} = (p_1p_2+k_La)/b. \end{cases} \tag{4}$$

For the case $\omega_n = 2\pi 2000\ rad/s$ and $\xi = 0.707$, the poles are located at $p_{1,2} = 0.2595 \pm j0.3171$. The controller and lead compensator gains for two natural frequencies are also presented in Table II. The resulted root locus with the lead compensator $k_L = 0.475$ is shown in Fig. 6. The poles location is more on the left compared to the previous case, which means the system is faster. Therefore, the proposed technique provides a higher bandwidth for the same damping factor.

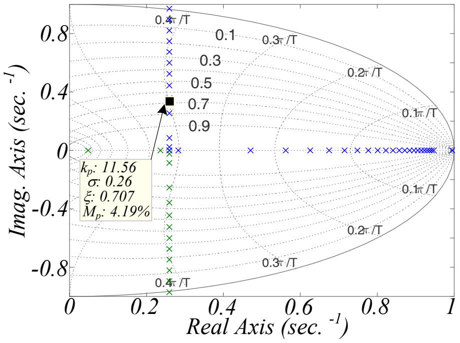

Fig. 6. Root locus of RL load including the lag introduced by PWM update, with the lead compensator and $k_L = 0.475$

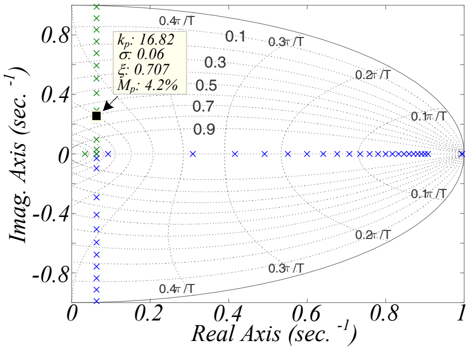

Fig. 7. Root locus of RL load including the lag introduced by PWM update, with the lead compensator and $k_L = 0.868$

The system is even faster when the controller is designed for a wider bandwidth, e.g. $\omega_n = 2\pi 3000\ rad/s$ and $\xi = 0.707$. In this case, solving the system of equations in (4) gives $k_L = 0.868$ and $k_{pI} = 16.82$. The root locus for $k_L = 0.868$ shows the closed-loop poles are located at $p_{1,2} = 0.0632 \pm j0.254$ (see Fig. 8).

A key observation is that the system with the lead compensator is much more damped around the desired bandwidth, as can be seen in Fig. 8.

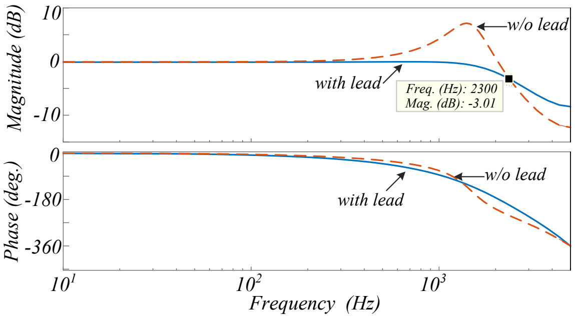

Fig. 8. Frequency response analysis with and w/o lead compensator, $k_L = 0.475$

The sensitivity to changes in the physical plant parameters, i.e. the filter inductor L_f and its equivalent series resistance R, is investigated (see Table I for the nominal values). The system is less sensitive to variation of R (see Fig. 9) than to changes in L_f. The eigenvalue migration as the inductance value changes is shown in Fig. 10.

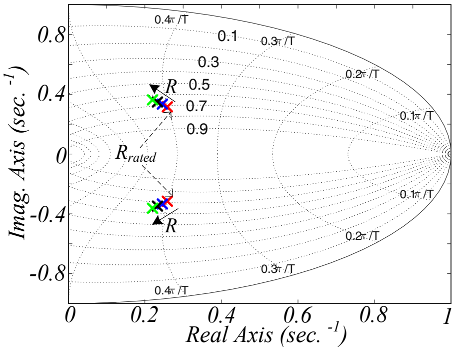

Fig. 9. Eigenvalue migration as a function of variation in $R_{rated} = 0.1\ \Omega \rightarrow R = 2\ \Omega$

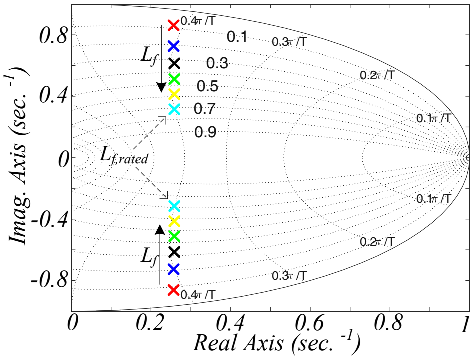

Fig. 10. Eigenvalue migration as a function of variation in $L = 0.9\ mH \rightarrow L_{rated} = 1.8\ mH$

IV. VOLTAGE REGULATOR DESIGN

The voltage regulator is based on PR controllers with a lead compensator structure

$$G_v(s) = k_{pV} + \sum_{h=1,5,7} k_{iV,h} \frac{s\cos(\varphi_h) - h\omega_1\sin(\varphi_h)}{s^2+(h\omega_1)^2}. \tag{5}$$

The proportional gain k_{pV} determines the bandwidth of the voltage regulator, and is designed for a bandwidth around 300 Hz. It is possible to achieve such a wide bandwidth because the inner current loop bandwidth can be increased by means of the lead compensator structure.

The lead angles at each harmonic frequency are set such that the trajectories of the open loop system on the Nyquist diagram, with the PR regulators at fundamental, 5th and 7th harmonics, guarantee a sensitivity peak η higher than a threshold value [4]. In this work the threshold has been set to $\eta = 0.6$ at no-load condition. After calculating the phase-lead angles, the fundamental resonant gain $k_{iV,1}$ is selected in order to have a fast response to changes in the fundamental component. According to the methodology presented in [4], (5) can be rewritten just for the resonant controller at fundamental, leading to the second-order system

$$G_v(s) = k_{pV}\frac{s^2 + \frac{k_{iV,1}}{k_{pV}}\cos(\varphi_1)s + \left[\omega_1^2 - \frac{k_{iV,1}}{k_{pV}}\omega_1\sin(\varphi_1)\right]}{s^2 + \omega_1^2}. \tag{6}$$

The pair of zeros of the PR controller in (6) are then moved as furthest as possible from the right half plane. This corresponds to the critically damped solution of the numerator equation, such that the pair of zeros of $G_v(s)$ are coincident. This corresponds to design $k_{iV,1}$ according to

$$k_{iV,1} \geq K\frac{2k_{pV}\mathfrak{z}_{crit}\omega_1}{\cos(\varphi_1)}, \tag{7}$$

where the lower bound of the inequality refers to $K = 1$, with the damping factor $\mathfrak{z}_{crit} = 1$. For the lead angle at fundamental frequency $\varphi_1 = 3.3°$, the gain is $k_{iV,1} = 53.5$. The upper bound is set by $k_{iV,1}$ values which do not significantly degrade the relative stability of the closed-loop system.

The harmonic resonant gains are selected to fulfill the requirements set by the IEC 62040 standard for UPS systems (see Table III).

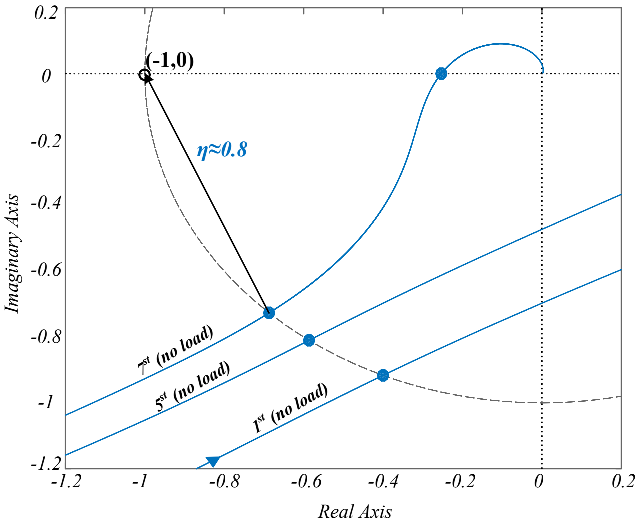

Fig. 11. Nyquist diagram of the system at no-load condition (command tracking of the reference voltage)

In Fig. 11 the Nyquist diagram of the system in Fig. 2 with the parameters of Table II is shown. The sensitivity peak is almost equal to 0.8 at no-load condition with all the harmonic resonators activated. It must be noted the harmonic resonators at 5th and 7th do not intersect the unit circle since the voltage loop bandwidth is set much higher than the highest harmonic order resonant filter.

TABLE III
VOLTAGE REGULATOR PARAMETERS

Parameter	Value
Proportional gain	$k_{pV} = 0.085$
Integral gain @50Hz	$k_{iV} = 53.5$
Integral gain @250Hz	$k_{iVh5} = 15$
Integral gain @350Hz	$k_{iVh7} = 15$

I. ANTI-WIND UP DESIGN

A discrete anti-wind up scheme must be implemented to avoid the saturation of the integral term in the voltage regulator. No anti-wind up scheme is needed for the current loop since a P controller is used as regulator. The anti-wind up scheme is shown in Fig. 12.

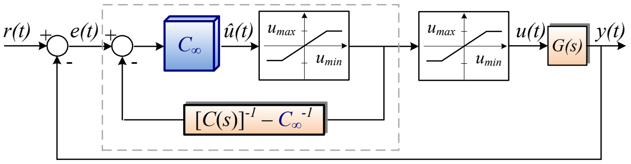

Fig. 12. Anti-wind up scheme based on [11]

According to [11], the controller $C(s)$ should be: i) biproper, i.e. zero relative degree between the TF numerator and denominator; and ii) minimum phase. If this is the case, the controller can be split into a direct feedthrough term (C_∞) and a strictly proper transfer function $\bar{C}(s)$

$$C(s) = C_\infty + \bar{C}(s). \tag{8}$$

For the particular case of an ideal PR controller

$$C_\infty = k_{pV}; \qquad \bar{C}(s) = k_{iV}\frac{s}{s^2 + \omega_o^2}$$

$$C(s) = k_{pV} + k_{iV}\frac{s}{s^2 + \omega_o^2} \tag{9}$$

In normal operation ($u_{min} < \hat{u}(t) < u_{max}$), the closed-loop TF (within the dotted line in Fig. 12) is equal to $C(s)$. During saturation the input to the controller states is bounded.

As the anti-wind up scheme is implemented in the discrete-time domain, interesting issues arise. In general, the discrete-time implementation of the feedback path in normal operation (without the saturation block) takes the form in Fig. 13. If $b_0 \neq 0$, an algebraic loop arises. This is directly related to the discretization method used for $\bar{C}(s)$.

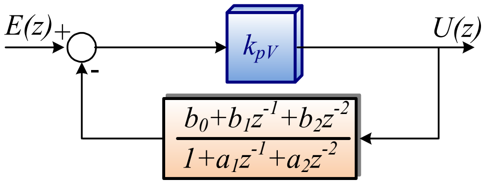

Fig. 13. Anti-wind up implementation in the discrete-time domain during normal operation

A possibility to avoid the algebraic loop can be to use as discretization methods Zero-Order Hold (ZOH), Forward Euler (FE) or Zero-Pole Matching (ZPM), which assure $b_0 = 0$. However, the performance of the voltage controller is degraded if FE is used as discretization method [12] (zero steady-state error is not achieved). This can be seen in Fig. 14, where the frequency response of the controller discretized with these methods is shown. The gain at resonant frequency is no more infinite if FE is used as discretization method.

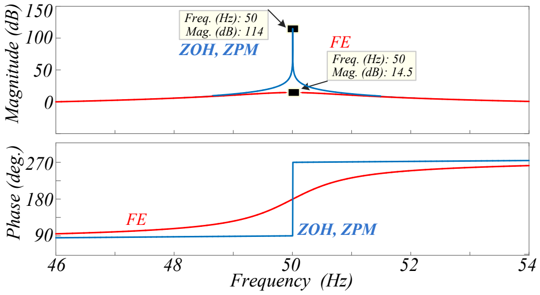

Fig. 14. Frequency response of the resonant controller using ZOH, ZPM and FE

II. EXPERIMENTAL RESULTS

The power system of Fig. 1 was tested to check the theoretical analysis presented. For this purpose, a low scale test-bed has been built using a Danfoss 2.2 kW converter, driven by a dSpace DS1006 platform. The LC filter parameters and operational information are presented in Table I. In all the tests voltage decoupling is performed as shown in Fig. 2.

A. Current regulator tests

In order to compare the proportional gain with/without lead compensator schemes in terms of dynamic response, a step change of the inductor current is performed. In order to achieve approximately zero steady-state error with different control structures, the reference is multiplied by a constant ($I_{refgain}$), which is equivalent to multiply by a gain the closed-loop TF of the inductor current. It should be noted that the dynamics of the system with the current loop only, i.e. voltage loop disabled and current reference generated manually, is not affected by this gain, which is also significantly lower as the bandwidth is widen. For the system with the proportional gain only (see Fig. 3), the step response is degraded as k_{pI} is increased (see Fig. 15 and Fig. 16). This result also shows that due to additional losses the setup has more damping than expected. In Fig. 17 and Fig. 20 the step response is even less damped and more oscillatory for $k_{pI} = 16.82$. Nevertheless, it is clear that there is a limitation in bandwidth due to the system delay.

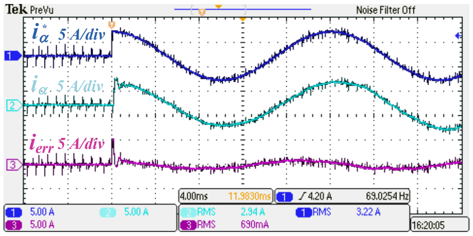

Fig. 15. Step response – P controller: **$k_{pI} = 11.56$**, reference (5 A/div), real (5 A/div) and inductor current error (5 A/div) (α-axis), **time scale (4 ms/div)**

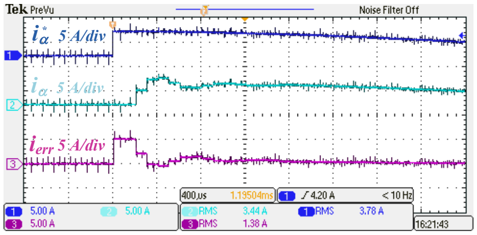

Fig. 16. Step response – P controller: **$k_{pI} = 11.56$**, reference (5 A/div), real (5 A/div) and inductor current error (5 A/div) (α-axis), **time scale (400 µs/div)**

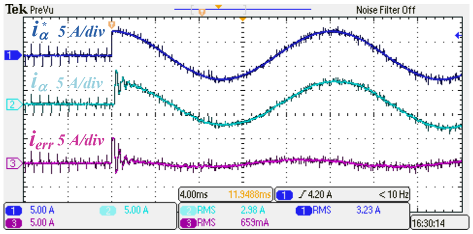

Fig. 17. Step response – P controller: **$k_{pI} = 16.82$**, reference (5 A/div), real (5 A/div) and inductor current error (5 A/div) (α-axis), **time scale (4 ms/div)**

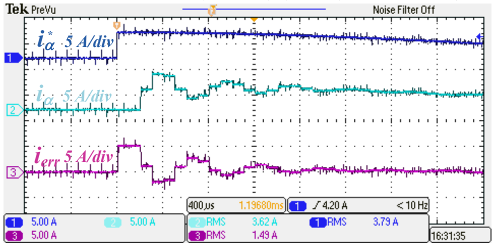

Fig. 18. Step response – P controller: **$k_{pI} = 16.82$**, reference (5 A/div), real (5 A/div) and inductor current error (5 A/div) (α-axis), **time scale (400 µs/div)**

If the control structure with a lead compensator is used (see Fig. 5), the bandwidth can be increased in comparison to the case with just the proportional controller for the same k_{pI} value, without degrading the dynamic performance. The step response for $\omega_n = 4000\pi\ rad/s$, i.e. $k_{pI} = 11.56$, is less oscillatory, as shown in Fig. 19 and Fig. 20. As the proportional gain is designed to achieve $\omega_n = 6000\pi\ rad/s$, i.e. $k_{pI} = 16.82$ (see Fig. 21 and Fig. 22), the step response is more damped than the one in Fig. 17.

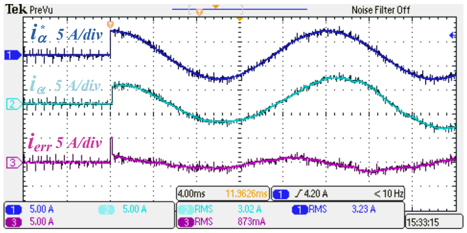

Fig. 19. Step response – P controller with lead compensator: **$k_{pI} = 11.56$**, **$k_L = 0.475$**, reference (5 A/div), real (5 A/div) and inductor current error (5 A/div) (α-axis), time scale (4 ms/div)

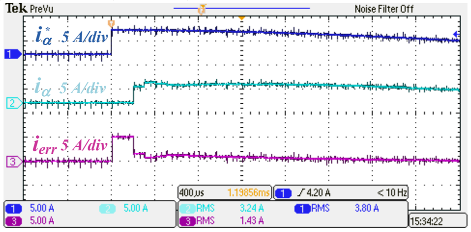

Fig. 20. Step response – P controller with lead compensator: **$k_{pI} = 16.82$**, **$k_L = 0.868$**, reference (5 A/div), real (5 A/div) and inductor current error (5 A/div) (α-axis), **time scale (400 µs/div)**

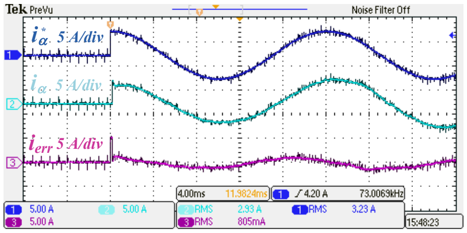

Fig. 21. Step response – P controller with lead compensator: $\boldsymbol{k_{pI} = 11.56}$, $\boldsymbol{k_L = 0.475}$, reference (5 A/div), real (5 A/div) and inductor current error (5 A/div) (α-axis), **time scale (4 ms/div)**

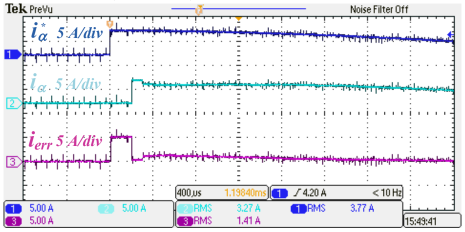

Fig. 22. Step response – P controller with lead compensator: $\boldsymbol{k_{pI} = 16.82}$, $\boldsymbol{k_L = 0.868}$, reference (5 A/div), real (5 A/div) and inductor current error (5 A/div) (α-axis), **time scale (400 µs/div)**

B. *Voltage regulator tests*

All the following results (Fig. 23 and Fig. 24) regarding the voltage loop are obtained with voltage decoupling, P controller as current regulator, lead compensator and the anti-wind up scheme proposed in the previous section. The parameters of the system are presented in Table I. In Fig. 23 a 100% linear step load change is shown. The results obtained are compared to the envelope of the voltage deviation v_{dev} as reported in the IEC 62040 standard for UPS systems [see Fig. 24]. It can be seen that the system reaches steady-state in less than half a cycle after the load step change. The dynamic response is within the limits imposed by the standard.

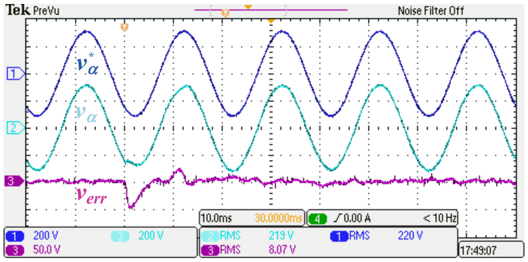

Fig. 23. Linear step load changing (0 – 100%): reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis), **time scale (10 ms/div)**

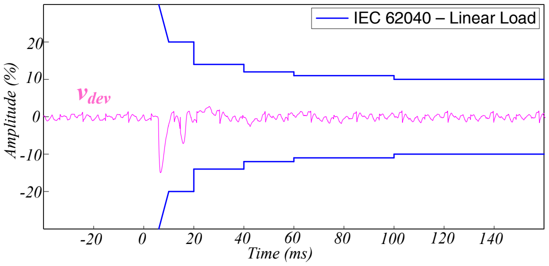

Fig. 24. Linear step load changing (0 – 100%): Dynamic characteristics according to IEC 62040 standard for linear loads: overvoltage ($\boldsymbol{v_{dev} > 0}$) and undervoltage ($\boldsymbol{v_{dev} < 0}$)

A diode bridge rectifier with an LC output filter supplying a resistive load is used as nonlinear load. Its parameters are presented in Table I. A 100% nonlinear step load change is performed with the harmonic compensators (HC) tuned at 5th and 7th harmonics (see Fig. 25). The results are in accordance with the standard IEC 62040 even for linear loads, as can be seen in Fig. 26.

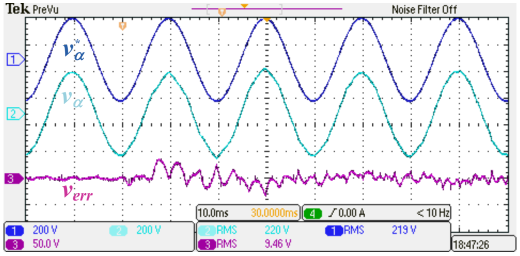

Fig. 25. Nonlinear step load changing (0 – 100%): reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis), **time scale (10 ms/div)**

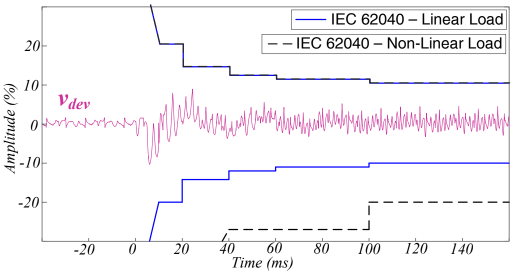

Fig. 26. Nonlinear step load changing (0 – 100%): Dynamic characteristics according to IEC 62040 standard for linear loads: overvoltage ($\boldsymbol{v_{dev} > 0}$) and undervoltage ($\boldsymbol{v_{dev} < 0}$)

The effects of the anti-wind up scheme are shown in Fig. 27 and Fig. 28. As the anti-wind up scheme is implemented, a step change of the reference voltage results in a less oscillatory response.

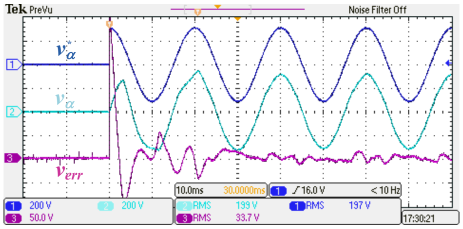

Fig. 27. Step response of the reference voltage: without anti-windup scheme, reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis), **time scale (10 ms/div)**

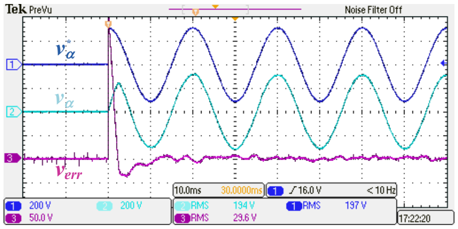

Fig. 28. Step response of the reference voltage: with anti-wind up scheme, reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis), **time scale (10 ms/div)**

III. CONCLUSIONS

Recent approaches in the control of power converters working in islanding mode have proved that state-feedback decoupling permits to achieve better dynamic response. In this context, the proposed work investigates other design and implementation features related to the islanding microgrid application.

Firstly, in order to enhance the current controller dynamics, a lead compensator is introduced in the current loop. Its feasibility to enhance bandwidth and damping has been shown. This improvement in the inner current control permits to increase the bandwidth of the voltage loop and include resonant controllers for steady-state harmonic rejection in presence of nonlinear loads. As the bandwidth of the voltage loop is increased, an anti-wind up scheme becomes even more important. The proposed design in the discrete-time domain avoids algebraic loops, which could arise depending on the discretization method.

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