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***Abstract*— State feedback decoupling allows to achieve a better dynamics for Voltage Source Inverters operating in isolated microgrids or UPS systems. The design of current and voltage regulators is performed in the discrete-time domain since provides better accuracy and allows direct pole placement. As the bandwidth of the innermost loop is mainly limited by computation and PWM delays, a structure based on a lead compensator is proposed to overcome this limitation. The design of the voltage regulator is based on the Nyquist criterion, verifying to guarantee a high sensitivity peak. Discrete-time domain implementation issues of an anti-wind up scheme are discussed as well. Laboratory tests in compliance with the standard for UPS systems are performed to verify the theoretical analysis.**

Keywords—voltage and current regulators; power quality; microgrids

I. INTRODUCTION

The increasing share of renewable energy sources interfaced via power converters requires even more severe dynamics performance of voltage and current regulators. With reference to hierarchical control in microgrids [1], the performance of the overall control system can degrade significantly if the inner loops at primary control level have poor dynamics. The primary control of voltage source inverters for islanded applications usually consists of cascaded loops, the innermost one being the current regulator. This latter is responsible for dynamics and characterized by a bandwidth as wider as possible, mainly limited by computation and PWM delays in digital implementations. On the other hand, the outer voltage loop tracks the commanded reference with a much slower dynamics. A possible design choice consists in selecting the inductor current and capacitor voltage as state variables. The coupling between the two controlled states significantly degrades the performance of the inner regulators.

For the above reasons, an active control action to decouple the controlled states is needed. The damping of the system and command tracking capability are significantly improved, even with just a proportional controller as current regulator. Ideally, the system becomes not dependent on the disturbance, i.e. the output current. In practice still the computation and PWM delays that are not compensated for on the decoupling path do not allow to ideally decouple the states, such that the state feedback decoupling action is less effective.

The design of the regulators can be performed in the continuous-time domain with Laplace-domain models, which can be useful to provide a general perception of system dynamics [2]. Subsequently, some discretization method is used for digital implementation of the regulators. However, the mapping from the *s*-domain to the *z*-domain can introduce some discrepancy in the poles location [3], in particular for discretization of high-frequency harmonic compensators. On the other hand, the direct design of digital compensators in the discrete-time domain provides more accuracy. In fact, the use of Impulse Invariant Z-transform allows to treat the latch/zero-order hold effect and time lag accurately [4], without the need of using approximated rational transfer functions for modelling the system delays [5]. Other advantages are the following: i) design for direct pole-placement [6]; ii) improved dynamic performance and robustness of the regulators [7], especially if the current regulator is designed to achieve wide bandwidth [8]; iii) ease of implementation to track commanded arbitrary trajectories. According to the previous discussion, direct design in the discrete-time domain can be considered convenient.

As recently proved in [9], the state feedback decoupling action can be improved by leading the capacitor voltage on the state feedback decoupling path. However, the analysis is performed in the continuous-time domain and the possibility to widen the current loop bandwidth by means of a lead compensator on the forward path is not investigated.

This paper is organized as follows. In Section II the system is described with focus on its block diagram representation. In Section III the current regulator is designed in the discrete-time domain along with the lead compensator to achieve a wider bandwidth. In Section IV the tuning of the voltage regulator is performed by means of Nyquist criterion. The design of an anti-wind up scheme is also proposed. Finally, in Section V results from laboratory tests are shown to support the theoretical analysis.

II. SYSTEM DESCRIPTION

In standalone applications, the VSI is equipped with an LC filter at its output. In general, it operates in voltage control mode with the capacitor voltage and inductor currents being the controlled states.

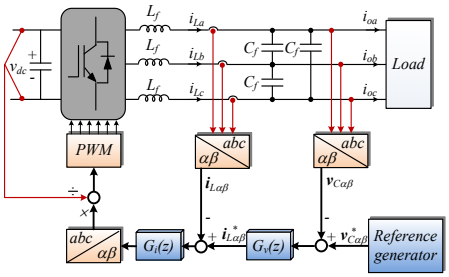

Fig. 1. Block diagram of a three phase VSI with voltage and current loops

In Fig. 1 the block diagram including a three-phase inverter with its inner loops is presented. The aim of the inner current loop is to track the commands from the outer voltage loop and ensure fast dynamic disturbance rejection within its bandwidth [10].

The simplified block diagram of the closed-loop system in the continuous-time domain is shown in Fig. 2, where $\boldsymbol{V}^*_{C\alpha\beta}$ and $\boldsymbol{I}^*_{L\alpha\beta}$ are the voltage and current reference vectors and $\boldsymbol{I}_{o\alpha\beta}$ is the output current vector, which acts as a disturbance to the system. $G_i(s)$ and $G_v(s)$ represent the current and voltage regulators transfer functions (TF) in the continuous-time domain. A first order Padé approximation of the type $G_{PWM}(s) \cong [1-(T_d/2)s]/[1+(T_d/2)s]$ is used to model the computation and PWM delays, where $T_d = 1.5/f_s$, being f_s the switching frequency. $G_{dec}(s)$ is the TF related to the decoupling of the cross-coupling states.

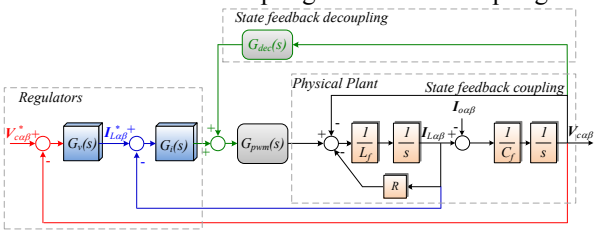

Fig. 2. Simplified block diagram of the closed-loop system in the continuos-time domain

A similar closed-loop diagram can be derived in the discrete-time domain, as shown in Fig. 3. Compared to Fig. 2, the system delays are exactly modelled by one sample delay due to the implemented regular sample symmetrical PWM strategy [11] and the latch interface from the digital compensators to the physical plant.

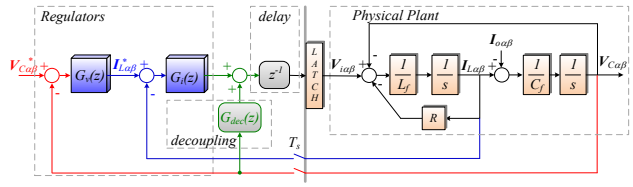

Fig. 3. Simplified block diagram of the closed-loop system in the discrete-time domain

III. Current Regulator Design

The design of the controllers is based on serial tuning which means that initially the innermost loop must be tuned, i.e. the current loop in this case. To provide a general perception of the effects of voltage decoupling, the analysis is firstly made in the continuous-time domain. Moreover, the system parameters in Table I are used for analysis.

TABLE I. System Paramters

Parameter	Value
Switching frequency	$f_s = 10\ kHz$
Filter inductance	$L_f = 1.8\ mH$
Filter capacitor	$C_f = 27\ \mu F$
Inductor ESR	$R_f = 0.1\ \Omega$
Linear load	$R_l = 68\ \Omega$
Non linear load	$C_{NL} = 235\ \mu F$ $R_{NL} = 155\ \Omega$ $L_{NL} = 0.084\ mH$

A. Continuous-time domain modelling

The proportional gain k_{pI} was selected to achieve the desired bandwidth (f_{bw}). By neglecting the delays of the system, the regulator gain can be calculated by

$$k_{pI} = 2\pi f_{bw} L_f.$$

For the overall delay of the system $T_d = 1.5T_s = 150\ \mu s$, a bandwidth of $1\ kHz$, this gain is approximately $k_{pI} = 11.32$. With reference to the root locus in Fig. 4, it can be noticed that as the gain is increased, i.e. the bandwidth is widen, higher damping is achieved. This is in contrast with the results where computation and PWM delays are not neglected.

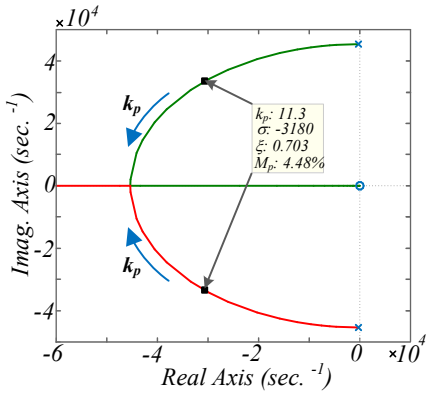

Fig. 4. Root locus for the inner current loop with P regulator and without voltage decoupling: x - open loop poles; ■ closed-loop poles for $\boldsymbol{k_{pI}} = \mathbf{11.32}$; o - zeros

When computation and PWM delays are considered, the regulator gain for the same bandwidth is $k_{pI} = 5.61$.

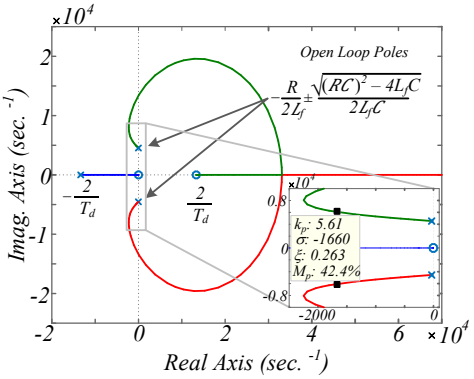

Fig. 5. Root locus for the inner current loop with P regulator and without voltage decoupling: x - open loop poles; ■ closed-loop poles for $\boldsymbol{k_{pI}} = \mathbf{5.61}$; o - zeros

From the root locus in Fig. 5, it can be seen that if the states are not decoupled the system has low damping and high overshoot. This is true whatever gain is selected. However, as expected, increasing the gain effectively reduces the system damping.

If voltage decoupling is performed (see Fig. 6), the order of the system is lowered by one degree and higher damping is achieved with less overshoot for the same bandwidth.

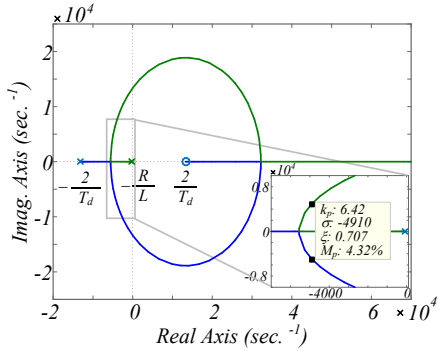

Fig. 6. Root locus for the inner current loop with P regulator and voltage decoupling: x – open loop poles; ■ closed-loop poles for $\boldsymbol{k_{pI} = 6.42}$; o – zeros

B. *Discrete-time domain modelling*

With reference to Fig. 3, the input voltage is the latched manipulated input to the physical system. A simple P controller and a RL load modelled in the discrete-time domain are considered [8], as shown in the block diagram of Fig. 7. This model can be used for analysis since decoupling ideally the controlled states determines no dependence on the load.

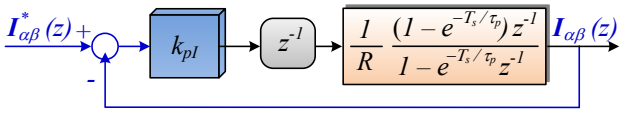

Fig. 7. Simplified block diagram of the current loop closed-loop system in the discrete-time domain

The closed-loop TF of the inner current loop system in Fig. 7 is

$$\frac{I(z)}{I^*(z)} = \frac{k_{pI}b}{z^2 - az + k_{pI}b}.$$

Where $b = (1 - e^{-\frac{T_s}{\tau_p}})/R; a = e^{-\frac{T_s}{\tau_p}}$.

The root locus is shown in Fig. 8.

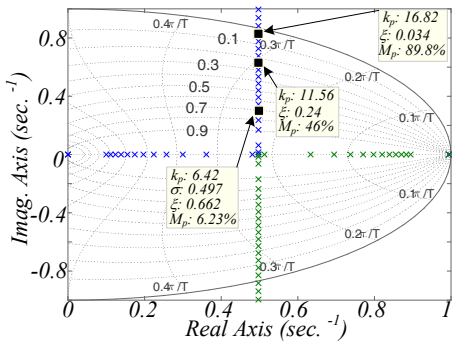

Fig. 8. Root locus of RL load including the lag introduced by PWM update

Because of the delay, there is a limitation in the gain to achieve a system with enough damping. Since there are two poles and just one variable (k_{pI}) that can change their locations, it is not possible to place the roots at any desired location. The designed gain to achieve a damping of $\xi = 0.662$ is $k_{pI} = 6.42$, as reported in Table II.

To widen the system bandwidth and still achieve a reasonable damped closed-loop system, a lead compensator as shown in Fig. 9 is designed, also referred to as 'Delay prediction and Feedback' [12].

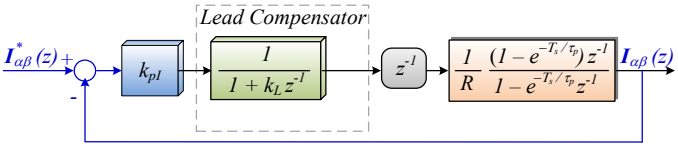

Fig. 9. Model of RL load including the lag introduced by PWM update, with the model of the lead compensator $G_L = 1/(1 + k_L z^{-1})$

The closed-loop TF becomes

$$\frac{I(z)}{I^*(z)} = \frac{k_{pI}b}{(z + k_L)(z - a) + k_{pI}b}.$$

The poles of this TF must satisfy the relationship

$$z^2 - (p_1 + p_2)z + p_1p_2 = z^2 + (k_L - a)z - k_La + k_{pI}b.$$

Where p_1, p_2 are the desired pole locations, defined as

$$p_{1,2} = e^{-\xi\omega_n T_s}[\cos(\omega_d T_s) \pm jsin(\omega_d T_s)]$$
$$\omega_d = \omega_n\sqrt{1-\xi^2}.$$

Solving the system leads to

$$k_L = a - (p_1 + p_2)$$
$$k_{pI} = (p_1p_2 + k_La)/b.$$

Given $\omega_n = 2\pi 3000\, rad/s$ and $\xi = 0.707$, the poles are located at $p_{1,2} = 0.0632 \pm j0.254$. The controller and lead compensator gains are also presented in Table II. The corresponding root locus with the lead compensator $k_L = 0.868$ is shown in Fig. 10. The poles location is more on the left compared to Fig. 8, which means the system is faster. Therefore, the proposed technique provides a wider bandwidth for almost the same damping factor.

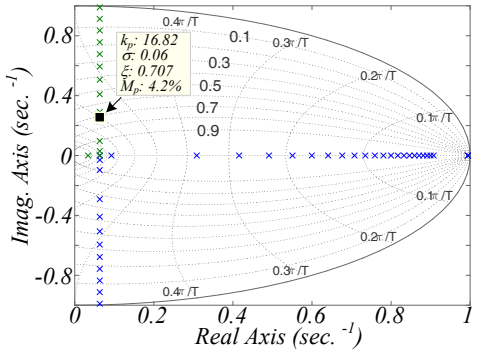

Fig. 10. Root locus of RL load including the lag introduced by PWM update, with the lead compensator: $k_L = 0.868$

TABLE II. CURRENT REGULATOR PARAMETERS

Parameter	Value
Proportional gain w/o lead	$k_{pI} = 6.42$
Proportional and lead gains @$\omega_n = 4000\pi$ rad/s	$\begin{cases} k_{pI} = 16.82 \\ k_L = 0.868 \end{cases}$

IV. VOLTAGE REGULATOR DESIGN

The voltage regulator is based on PR controllers with a lead compensator structure. The proportional gain k_{pV} determines the bandwidth of the voltage regulator, and is designed for a bandwidth around 300 Hz. It is possible to achieve such a wide bandwidth because the inner current loop bandwidth can be increased by means of the lead compensator structure. The design criteria is based on [9], such that the trajectories of the open loop system on the Nyquist diagram, with the PR regulators at fundamental, 5th and 7th harmonics, guarantee a sensitivity peak η higher than a threshold value, e.g. $\eta = 0.4$ in this work. The voltage regulator parameters are shown in Table III.

TABLE III. VOLTAGE REGULATOR PARAMETERS

Parameter		Value	
Proportional gain		$k_{pV} = 0.06$	
Integral gains and lead angles	@50Hz	$k_{iV,1} = 40$	$\varphi_1 = 3.3°$
	@250Hz	$k_{iV,5} = 15$	$\varphi_5 = 37°$
	@350Hz	$k_{iV,7} = 15$	$\varphi_7 = 44°$

The Nyquist diagram with the harmonic compensators at 5th and 7th harmonics is shown in Fig. 11. The sensitivity peak is higher than 0.4, thus fulfilling the design requirements.

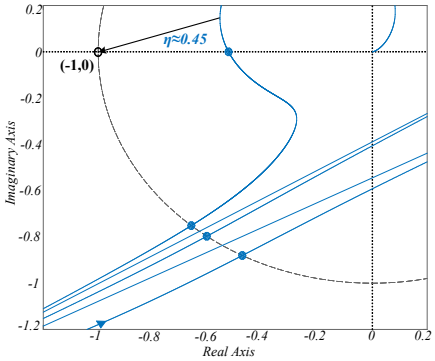

Fig. 11. Nyquist diagram of the system in Fig. 3

A discrete anti-wind up scheme must be implemented to avoid the saturation of the integral term in the voltage regulator. No anti-wind up scheme is needed for the current loop since a P controller is used as regulator. The anti-wind up scheme is shown in Fig. 12 [13].

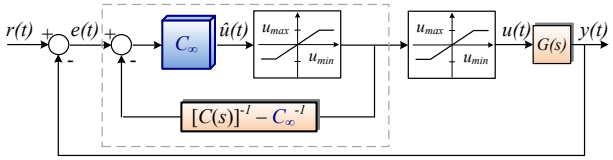

Fig. 12. Anti-wind up scheme based on [13]

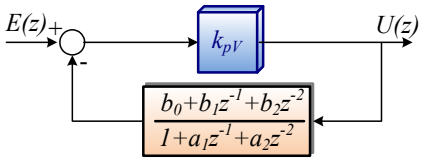

Fig. 13. Anti-wind up implementation in the discrete-time domain during normal operation

According to [13], the controller $C(s)$ should be: i) biproper, i.e. zero relative degree between the TF numerator and denominator; and ii) minimum phase. If this is the case, the controller can be split into a direct feedthrough term (C_∞) and a strictly proper transfer function $\bar{C}(s)$:

$$C(s) = C_\infty + \bar{C}(s)$$

For the particular case of an ideal PR controller:

$$C_\infty = k_{pV}; \qquad \bar{C}(s) = k_{iV}\frac{s}{s^2 + \omega_o^2}$$

$$C(s) = k_{pV} + k_{iV}\frac{s}{s^2 + \omega_o^2}$$

In normal operation ($u_{min} < \hat{u}(t) < u_{max}$), the closed-loop TF (within the dotted line in Fig. 12) is equal to $C(s)$. During saturation the input to the controller states is bounded.

As the anti-wind up scheme is implemented in the discrete-time domain, some interesting issues arise. In general, the discrete-time implementation of the feedback path in normal operation (without the saturation block) takes the form in Fig. 13. If $b_0 \neq 0$, an algebraic loop arises. This is directly related to the discretization method used for $\bar{C}(s)$.

A possibility to avoid the algebraic loop can be to use as discretization methods Zero-Order Hold (ZOH), Forward Euler (FE) or Zero-Pole Matching (ZPM), which assure $b_0 = 0$. However, the performance of the voltage controller is degraded if FE is used as discretization method [14] (zero steady-state error is not achieved). This can be seen in Fig. 14, where the frequency response of the controller discretized with these methods is shown. The gain at resonant frequency is no more infinite if FE is used as discretization method.

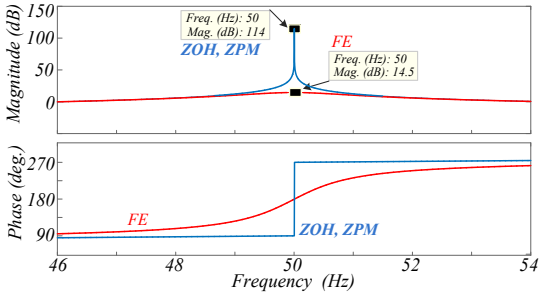

Fig. 14. Frequency response of the resonant controller using ZOH, ZPM and FE

V. EXPERIMENTAL RESULTS

The power system of Fig. 1 was tested to check the theoretical analysis presented. For this purpose, a low scale test-bed has been built using a Danfoss 2.2 kW converter, driven by a dSpace DS1006 platform. The LC filter

parameters and operational information are presented in Table I. In all the tests voltage decoupling is performed as shown in Fig. 3.

In order to compare the proportional gain with/without lead compensator schemes in terms of dynamic response, a step change of the inductor current is performed. For the system with the proportional gain only (see Fig. 7), the step response is degraded as k_{pI} is increased [see Fig. 15(a)]. This result also shows that due to additional losses the setup has more damping than expected. In Fig. 15(b) the step response is even less damped and more oscillatory for $k_{pI} = 11.56$. Nevertheless, it is clear that there is a limitation in bandwidth due to the system delay.

If the control structure with a lead compensator is used (see Fig. 9), the bandwidth can be increased in comparison to the case with just the proportional controller for the same k_{pI} value, without degrading the dynamic performance. The step response for $\omega_n = 6000\pi\ rad/s$, i.e. $k_{pI} = 16.82$, is less oscillatory, as shown in Fig. 16(a).

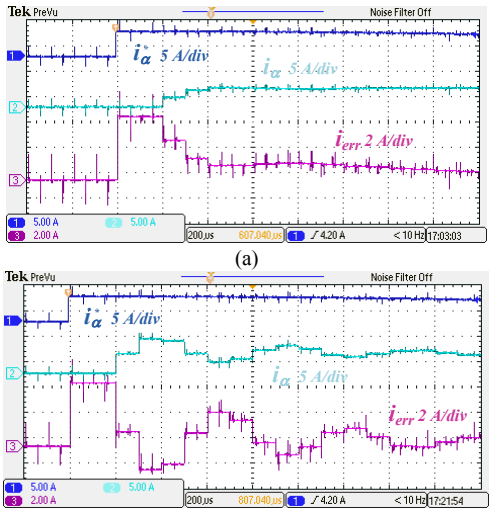

Fig. 15. Step response – P controller: (a) $k_{pI} = 6.42$, reference (5 A/div), real (5 A/div) and inductor current error (2 A/div) (α-axis); (b) $k_{pI} = 16.82$, reference (5 A/div), real (5 A/div) and inductor current error (2 A/div) (α-axis)

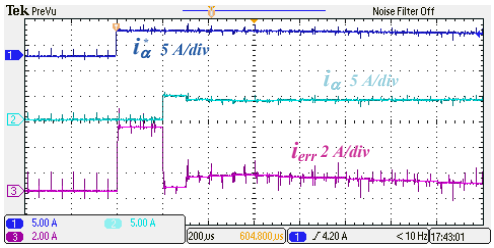

Fig. 16. Step response – P controller with lead compensator: $k_{pI} = 16.82$, $k_L = 0.868$, reference (5 A/div), real (5 A/div) and inductor current error (2 A/div) (α-axis).

All the following results (Fig. 17 and Fig. 18) regarding the voltage loop are obtained with voltage decoupling, P controller as current regulator, lead compensator and the anti-wind up scheme proposed in the previous section.

In Fig. 17(a) a 100% linear step load change is shown. The results obtained are compared to the envelope of the voltage deviation v_{dev} as reported in the IEC 62040 standard for UPS systems [see Fig. 17(b)]. It can be seen that the system reaches steady-state in less than half a cycle after the load step change. The dynamic response is within the limits imposed by the standard.

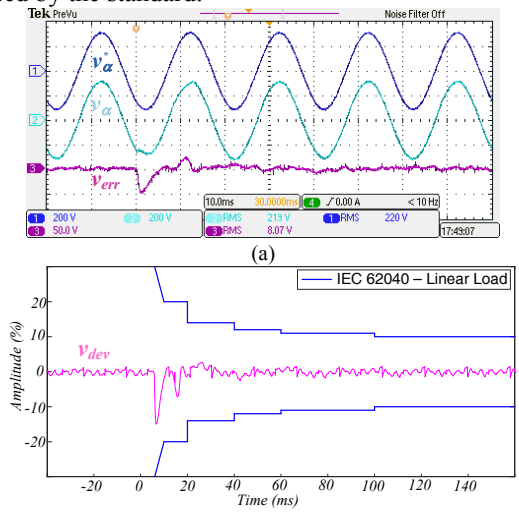

Fig. 17. Linear step load changing (0 – 100%): (a) reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis); (b) Dynamic characteristics according to IEC 62040 standard for linear loads: overvoltage ($v_{dev} > 0$) and undervoltage ($v_{dev} < 0$)

A diode bridge rectifier with an LC output filter supplying a resistive load is used as non-linear load. Its parameters are presented in Table I. A 100% non-linear step load change is performed with the harmonic compensator (HC) at fundamental only [see Fig. 18(a)]. Subsequently, the test is performed with the HC tuned at 5th and 7th harmonics [see Fig. 18(b)]. The results are in accordance with the standard IEC 62040 even for linear loads.

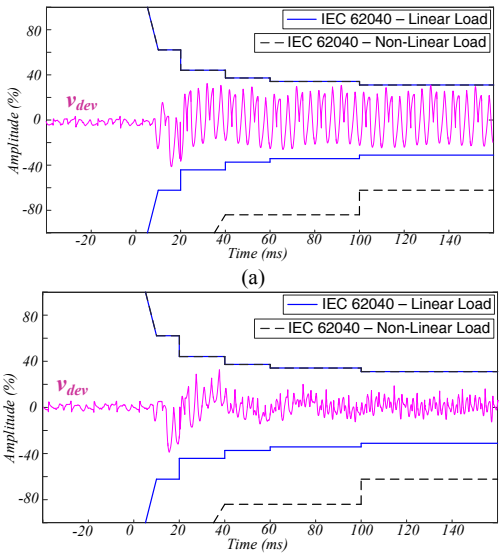

Fig. 18. Step response of the reference voltage: (a) without anti-windup scheme, reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis); (b) with anti-wind up scheme, reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis)

VI. CONCLUSIONS

An active control action based on state feedback decoupling has demonstrated to achieve better dynamics of power converters for stand-alone applications. The analysis proposed investigates other design and implementation features related to the islanding application. Firstly, in order to enhance the current regulator dynamics, a lead compensator structure is added in the forward loop. Its feasibility to widen the system bandwidth while still achieve high damping has been demonstrated. This improvement in the inner current control allows to widen the bandwidth of the voltage loop. As the bandwidth of the voltage loop is increased, an anti-wind up scheme becomes even more important. The proposed design in the discrete-time domain avoids algebraic loops, which could arise depending on the discretization method.

Experimental tests based on step response and step load change have been performed to verify the compliance with the standard IEC 62040 for UPS systems.

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