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Control Architecture for Paralleled Current-Source-Inverter (CSI) based Uninterruptible Power Systems (UPS)

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Abstract—This paper describes a theoretical and simulation study on a control strategy for the parallel operation of three-phase current source inverters (CSI), to be applied to uninterruptible power systems (UPS). A circulating current suppression strategy for parallel CSIs is proposed in this paper based on an auxiliary current control loop used to modify the reference currents by compensating the error currents between parallel inverters. The proposed method is coordinated together with droop and virtual impedance control. In this paper, droop control is used to generate the reference voltage of each inverter, and the virtual impedance is used to fix the output impedance of the inverters. In addition, a secondary control is used in order to recover the voltage deviation caused by the virtual impedance, and the auxiliary current control loop is added to acquire a better average current sharing performance among parallel CSIs, which can effectively suppress the circulating current. Simulation results are presented in order to verify the effectiveness of the proposed control methodology.

Keywords—parallel; current source inverter; circulating current; uninterruptible power system

I. INTRODUCTION

The current-source inverter (CSI) offers advantages over voltage source inverter (VSI) in terms of inherent boosting and short-circuit protection capabilities, direct output current controllability, and ac-side simpler filter structure [1], [2]. These features make it attractive in many UPS applications [3], such as high speed elevators, high-power electric drives and distributed generation systems as an interface between the utility grid and distributed power sources [4].

The topology of CSI is shown in Fig.1. It consists six IGBTs and six diodes to avoid current flowing from AC side to DC side. But with the rapid developments of the reverse-blocking IGBTs, the CSI may become a potentially predominant choice due to reduced conduction losses [5].

As the rating of switching devices is often limited or constrained by technical or economic considerations, parallel

architecture is often adopted to increase the power rating [6], [7]. In a parallel system, one of the main problems is the circulating current [7].

A traditional current-sharing solution is the frequency and voltage droop method with the feature of wireless control among UPS units [8], [9]. But the droop-method performance is particularly sensitive to the output impedance of the parallel inverters [9]. Virtual impedance is proposed in [10] to modify the output impedance, contributing to good power-sharing accuracy. However, in a practical paralleled inverters system, the parameters of the inverters, line impedance, and so forth, are unknown. Therefore, it is difficult to design proper virtual impedance for inverter which prepares to connect into system [11]. And if poorly designed or implemented, the virtual impedance method may introduce current distortions and therefore adversely affect the system stability and dynamics [12].

There are many reviews on the control strategies in inverter-based applications. The role of the controller in parallel inverters is to have good current sharing while maintain the system stability. Also the controller must achieve synchronization, and to guarantee that the frequency and the voltage are within the allowed limits, the control strategies can be classified into centralized, master-slave and decentralized and distributed control strategies.

The main disadvantage of the centralized strategy is the single point of failure and the need for sending the reference voltage to all the inverters in the network, which requires high bandwidth communication link. Additionally, the system is sensitive to nonlinear loads.

The master slave control strategy is classified as a quasi-decentralized control which can be a compromise between the centralized and the decentralized control strategy.

In the distributed control strategy, the average unit current can be determined by measuring the total load current and then divide this current by the number of units in the system [13].

There are excellent features of the current/power sharing, the load sharing is forced during transient and the circulating currents are reduced.

One of the most widely used decentralized control is the Droop control. The main idea is to regulate the voltage and the frequency by regulating the reactive and the active power respectively which can be sensed locally. The Droop control method has many desirable features such as expandability, modularity, redundancy, and flexibility. There are as well some drawbacks such as, slow transient response and possibility of circulating current. And the performance of droop-method is sensitive to the output impedance of the inverters.

In order to solve the problems of above mentioned control strategies, this paper presents a control method based on a third current control loop with droop and virtual impedance control. This method can be seen as a combination of droop control and distributed control. In the control strategy, the droop control is used to generate the reference voltage of each inverter, and the virtual impedance is used to regulate the output impedance of the inverters combined with a secondary control to recover the voltage drop, and a third output current control loop is added to analysis the current difference between parallel inverters, this concept is based on the distributed control strategy. And it is like another secondary control to compensate the output current of each inverter with the error current, finally to reach the purpose of average current-sharing between parallel inverters. More details will be introduced in section III.

This paper is organized as follows: In Section II, the circulating current analysis for paralleled current source inverters is discussed. Then a control method based on a third current control loop with droop and virtual impedance control is presented in Section III. In Section IV, simulation results are implemented which verify the effectiveness of the presented method. The conclusions are given in Section V.

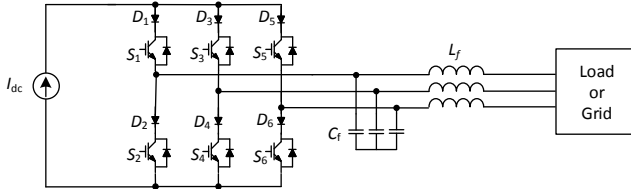


Fig. 1. Topology of the current source inverter.

II. THE PROPOSED CONTROL STRATEGY

A. The analysis of circulating current

This paper takes a system of two parallel-connected CSIs for an example to analyze the circulating current. The circulating current will flow from one inverter to another through the common AC bus. Figure 2 shows the probably circulating current path when IGBTs S_{12} and S_{21} are turned on. The circulating current will flow through the blue line, then across the solid red line or dotted red line based on the IGBTs which are in ON state. The parallel three-phase inverters considering the output impedances can be simplified as Fig.3 because of the similar principle of three-phase and single-phase inverters. In Fig.3, Z_1 and Z_2 are the output impedances of the

two parallel inverters respectively, Z_L is the load impedance, E_1 and E_2 are the outputs voltage of the two inverters, I_1 and I_2 are the output currents, E_o is the load voltage and I_o is the load current. According to literature [14], the circulating current I_{cir} can be defined as (1). Assuming that the output impedances of the parallel inverters are equal to each other, $Z_1=Z_2=Z$, then based on Fig.3, the circulating current can be calculated as (2). In a practical system, Z_1 and Z_2 will be different because of the different parameters of filters and line impedances or stray parameters. So virtual impedance can be used to modify the output impedance of the parallel inverters.

$$I_{cir} = (I_1 - I_2) / 2 \quad (1)$$

$$I_{cir} = (E_1 - E_2) / 2Z \quad (2)$$

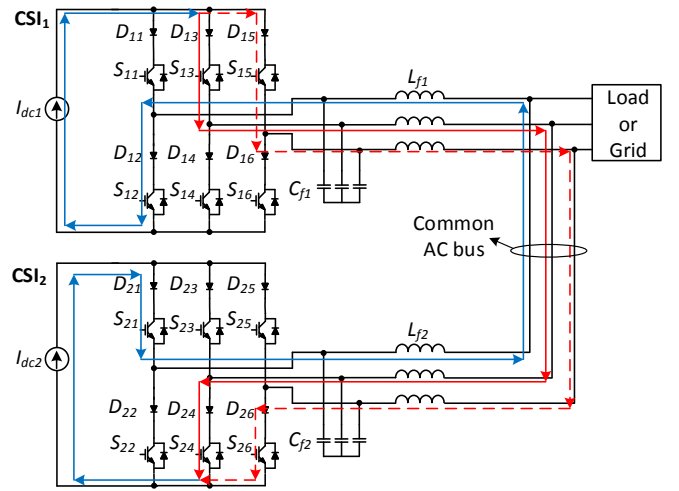


Fig. 2. The circulating current path in two parallel CSIs.

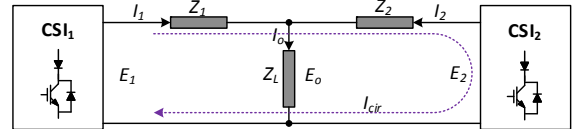


Fig.3. Equivalent circuit of two parallel CSIs.

B. The proposed control strategy

Figure 4 shows the block diagram of the control architecture for one of the parallel three-phase CSIs, the other one CSI will use the same control principle. In the control architecture, droop control is used to generate the reference voltage, the virtual impedance is used to modify the output impedance of the inverters, and in order to increase the stability of the droop control, at the meantime, a secondary control is added to recover the output voltage. R_{vl} and L_{vl} are the virtual resistor and virtual inductor respectively. The proposed auxiliary current control loop is marked with purple line. The basic concept is to appropriately revise the reference current from voltage control loop by sum of the error currents of d-axis and q-axis currents between the two parallel inverters which are named I_{doffx} and I_{qoffx} , $x=1,2$. With this compensation, new reference currents will be generated.

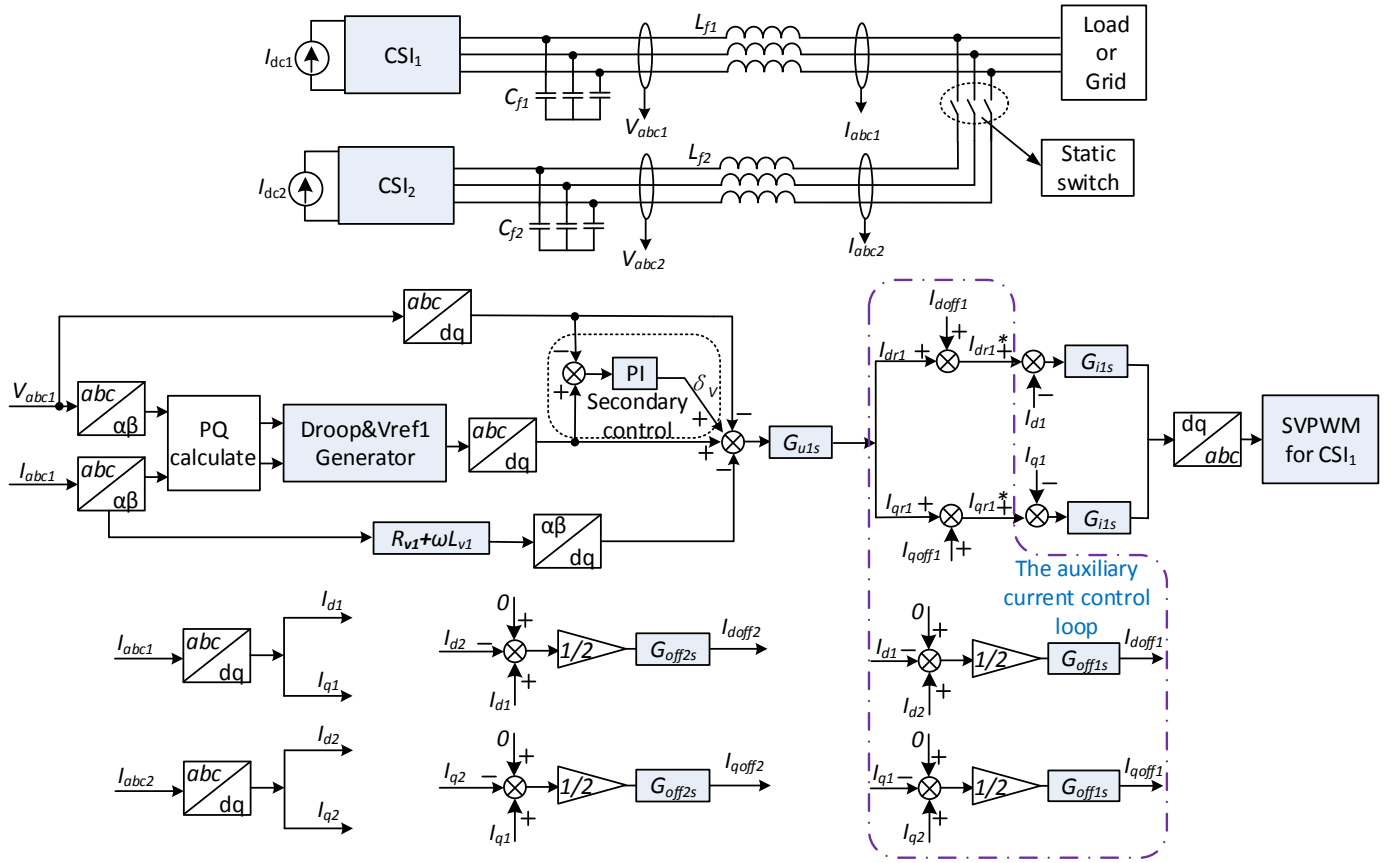


Fig. 4. The control architecture of parallel CSIs.

Take the generation of I_{doff1} and I_{qoff1} for example. I_{d1} , I_{q1} , I_{d2} and I_{q2} are the d-axis and q-axis currents from the Clark and Park transformation of the output currents I_{abc1} , I_{abc2} of CSI1 and CSI2. I_{dr1} , I_{qr1} , I_{dr2} and I_{qr2} are the reference currents from the outer voltage control loop. I_{dr1}^* , I_{qr1}^* , I_{dr2}^* and I_{qr2}^* are the new reference currents after compensation with the error current between the real output currents of CSI1 and CSI2. With (3) and (4), the d-axis error current I_{doff1} and q-axis error current I_{qoff1} between CSI1 and CSI2 are obtained. Note that this calculation is in the controller of CSI1, so I_{d1} and I_{q1} are in the position of dividend in (3) and (4). Then the error currents between I_{d1} , I_{d2} , I_{q1} and I_{q2} will be compared with 0 because if there is no circulating current between parallel inverters, the error currents I_{doffx} and I_{qoffx} ($x=1,2$) will be 0, and the other one purpose is to define the direction of the compensation. The gain “1/2” is from the circulating current calculation formula (1). And G_{offxs} ($x=1,2$) is the controller in the auxiliary current control loop. For example, if $I_{d1} > I_{d2}$, the direction of compensation should be decreasing I_{dr1} and increasing I_{dr2} . Based on (3) and (5), the calculation results will be $I_{doff1} < 0$, $I_{doff2} > 0$. Institute (3) to (7), (5) to (9), compared with I_{dr1} , I_{dr2} , the new d-axis reference current I_{dr1}^* will be decreased, and I_{dr2}^* will be increased which indicates the right compensation direction. With proper controller design in the current compensation loop, the circulating current can be effectively suppressed.

$$[0 - (I_{d1} - I_{d2})] / 2 = I_{doff1} \quad (3)$$

$$[0 - (I_{q1} - I_{q2})] / 2 = I_{qoff1} \quad (4)$$

$$[0 - (I_{d2} - I_{d1})] / 2 = I_{doff2} \quad (5)$$

$$[0 - (I_{q2} - I_{q1})] / 2 = I_{qoff2} \quad (6)$$

$$I_{dr1} + I_{doff1} = I_{dr1}^* \quad (7)$$

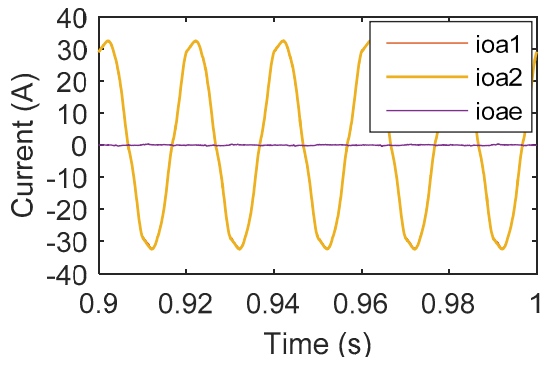
$$I_{qr1} + I_{qoff1} = I_{qr1}^* \quad (8)$$

$$I_{dr2} + I_{doff2} = I_{dr2}^* \quad (9)$$

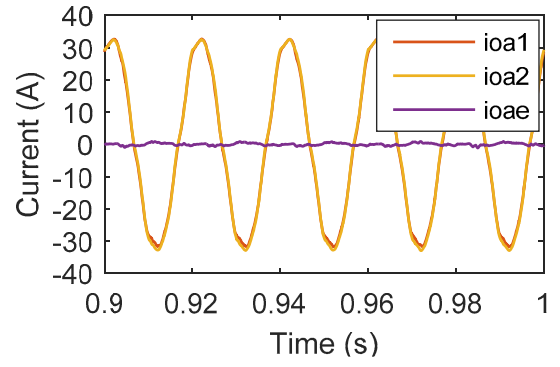
$$I_{qr2} + I_{qoff2} = I_{qr2}^* \quad (10)$$

III. SIMULATION RESULTS

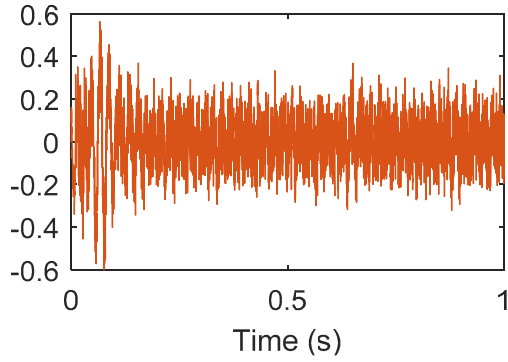
In order to verify the effectiveness of the proposed control strategy, a simulation model consists of two parallel-connected CSIs was built in Matlab/Simulink, using the proposed control strategy. Both of the linear and nonlinear loads were considered in the simulation. The nonlinear load was a rectifier connected with a resistor (5Ω) and a capacitor (235μF). The maximum phase current of each inverter will be 32.5A with the linear load. The simulation results with linear load are shown in Fig.5~Fig.6, and Fig.7~Fig.8 are the simulation results when nonlinear load is connected. Figure 5 and Fig.7 are the simulation waveforms with the proposed control strategy,



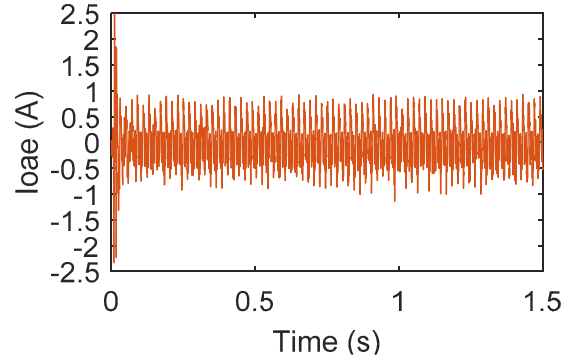
(a)



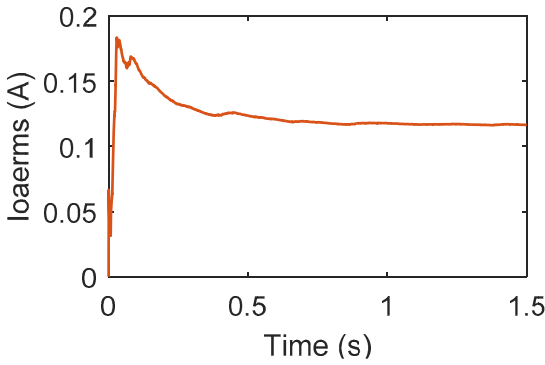
(a)



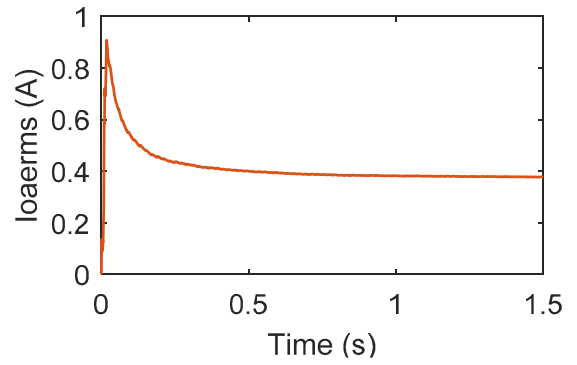
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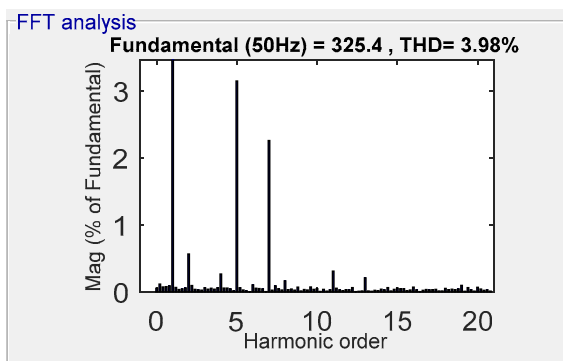
(b)



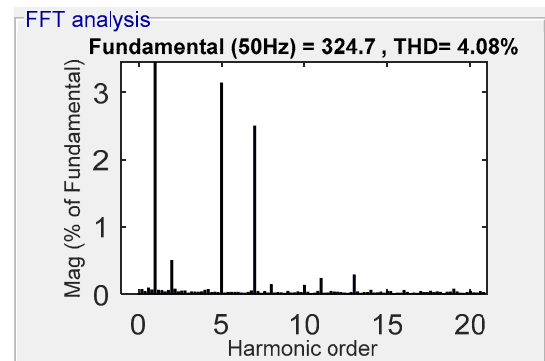
(c)



(c)



(d)

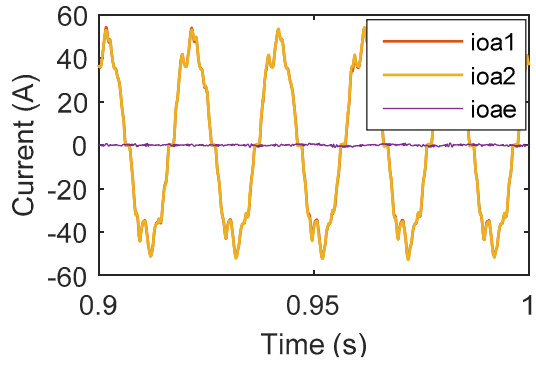


(d)

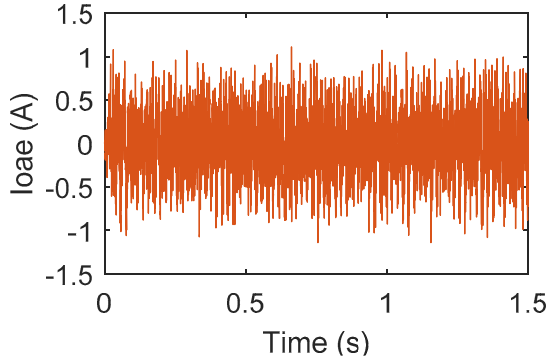
Fig. 5: Simulation results with the compensation control strategy when linear load is connected.

Fig. 6: Simulation results without the compensation control strategy when linear load is connected

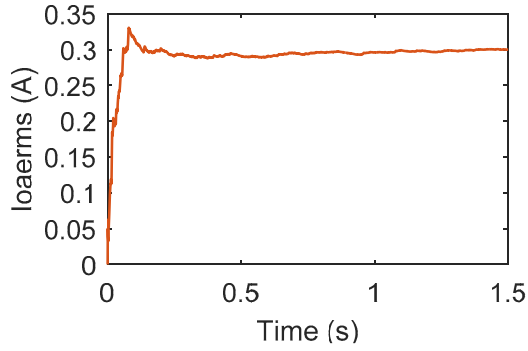
(a) The A phase currents and the circulating current between parallel CSIs. (b) The zoomed in A phase circulating current. (c) The RMS value of the A phase circulating current. (d) The THD analysis of the output voltage.



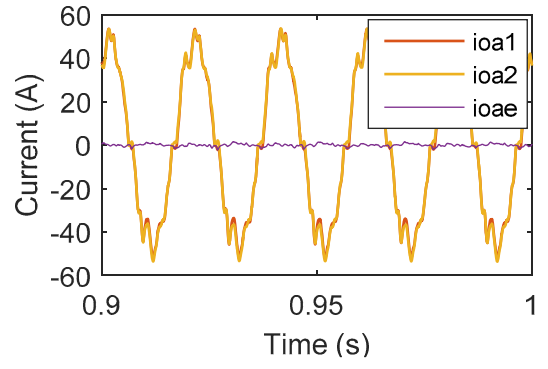
(a)



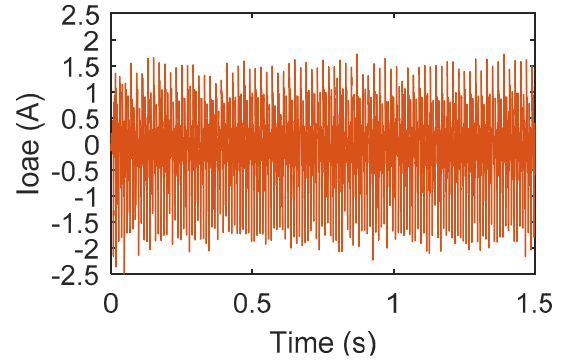
(b)



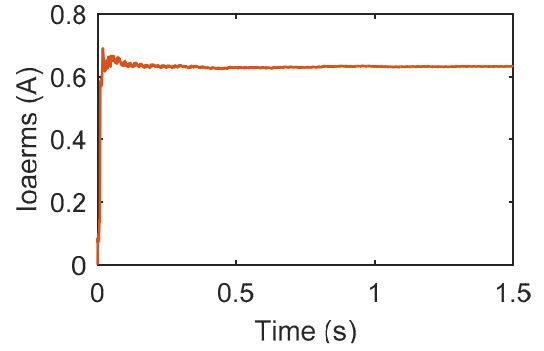
(c)



(a)



(b)



(c)

Fig. 7. Simulation results with the compensation control strategy when nonlinear load is connected.

(a) The A phase currents and the circulating current among parallel CSIs. (b) The zoomed in A phase circulating current. (c) The RMS value of the A phase circulating current.

Fig.6 and Fig.8 are the waveforms with the conventional control method.

Compared with the conventional droop and virtual impedance control method, the circulating current can be effectively suppressed with both linear and nonlinear load using the proposed control strategy. When the parallel CSIs supplied a linear load, the RMS value of the circulating current is about 120 mA, the number will be about 300mA when sharing a nonlinear load. It is much smaller than the conventional strategy as shown in the simulation waveforms. Therefore, a better average current-sharing performance is obtained.

Fig. 8. Simulation results without the compensation control strategy when nonlinear load is connected.

IV. CONCLUSION

Parallel inverters are widely used in the UPS applications for high power demand, and the average current-sharing scheme is necessary. A control strategy based on an auxiliary current control loop with droop and virtual impedance control is proposed in this paper. It combined the concept of droop control and the distributed control strategy. Simulation has been done when parallel-connected inverters were sharing linear or nonlinear load. The results demonstrate that, the circulating current among the parallel CSIs can be effectively suppressed, and the average current-sharing is realized.

REFERENCES

- [1] Z. Bai, X. Ruan, and Z. Zhang, "A Generic Six-Step Direct PWM (SS-DPWM) Scheme for Current Source Converter," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 659 - 666, Mar. 2010.
- [2] R. Guedouani, B. Fiala, E. M. Berkouk, and M. S. Boucherit, "Modeling and control of multilevel three-phase PWM current source inverter," in *Proc. IEEE ACEMP 2011*, Sep. 8–10, pp. 455 - 460.
- [3] D. C. Pham, S. Huang, and K. Huang, "Modeling and Simulation of Current Source Inverters with Space Vector Modulation," in *Proc. IEEE ICEMS 2010*, Oct. 10–13, pp. 320 - 325.
- [4] Z. Bai, Z. Zhang, and X. Ruan, "A Natural Soft-Commutation PWM Scheme for Current Source Converter and Its Logic Implementation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2772 - 2779, Jul. 2011.
- [5] C. Klumpner, "A new single-stage current source inverter for photovoltaic and fuel cell applications using reverse blocking IGBTs," in *Proc. IEEE PESC 2007*, Jun. 17–21, pp. 1683–1689.
- [6] T. B. Lazzarin, G. A. T. Bauer, and I. Barbi, "A control strategy for parallel operation of single-phase voltage source inverters: Analysis, design and experimental result," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2194–2204, Jun. 2013.
- [7] F. Wang, Y. Wang, Q. Gao, C. wang, and Y. liu, "A Control Strategy for Suppressing Circulating Currents in Parallel-Connected PMSM Drives With Individual DC Links," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1680–1691, Feb. 2016.
- [8] J. M. Guerrero, J. Matas, L. G. Vicuna, M. Castilla, and J. Miret, "Wireless-control strategy for parallel operation of distributed-generation inverters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1461–1470, Oct. 2006.
- [9] Y. Zhang, M. Yu, F. Liu, and Y. Kang, "Instantaneous Current-Sharing Control Strategy for Parallel Operation of UPS Modules Using Virtual Impedance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 432–440, Jan. 2013.
- [10] J. M. Guerrero, L. G. Vicuna, J. Matas, M. Castilla, and J. Miret, "Output impedance design of parallel-connected UPS inverters with wireless load-sharing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1126–1135, Aug. 2005.
- [11] H. Shi, F. Zhuo, D. Zhang, Z. Geng, and F. Wang, "Adaptive Implementation Strategy of Virtual Impedance for Paralleled Inverters UPS," in *Proc. IEEE ECCE 2014*, Sep. 14–18, pp. 158–162.
- [12] J. He, and Y. Li, "Analysis, Design, and Implementation of Virtual Impedance for Power Electronics Interfaced Distributed Generation," *IEEE Trans. Ind. Applica.*, vol. 47, no. 6, pp. 2525–2538, Nov. 2011.
- [13] M. Prodanovic, T. C. Green, and H. Mansir, "Survey of control methods for three-phase inverters in parallel connection," *IEEE Conference Publication (475)* 472–477.
- [14] H. Cai, R. Zhao, and H. Yang, "Study on Ideal Operation Status of Parallel Inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2964–2969, Nov. 2008.