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A Component-Reduced Zero-Voltage Switching Three-Level DC-DC Converter

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***Abstract*—The basic Zero-Voltage Switching (ZVS) three-level DC-DC converter has one clamping capacitor to realize the ZVS of the switches, and two clamping diodes to clamp the voltage of the clamping capacitor. In order to reduce the reverse recovery loss of the diode as well as its cost, this paper proposes to remove one of the clamping diodes in basic ZVS three-level DC-DC converter. With less components, the proposed converter can still have a stable clamping capacitor voltage, which is clamped at half of the dc link voltage. Moreover, the ZVS performance will be influenced by removing the clamping diode. But as long as the clamping capacitor is properly selected, the degradation of the ZVS performance can be neglected. The impact of the clamping capacitor on the ZVS performance is mathematically analyzed as well.**

I. Introduction

Three-level (TL) DC-DC converter was first proposed around 1992 for medium voltage application [1, 2], where the basic topology has two clamping diodes. The clamping diodes can clamp the voltage of the switches at half of the dc bus votlage (V_{in}) as a maximum value, so the voltage stress of the switches is only half of V_{in}. But with only two clamping diodes, the switche voltage can only be discharged to $\frac{V_{in}}{4}$ by resonance with the leakage inductance of the tansformer during turn on transient, which means $\frac{V_{in}}{4}$ on the output capacitor of the switches will be discharged by hard switching. Then, a clamping capacitor was introduced by Canales to decouple the affect between the inner and outer switches [3], as shown in Fig. 1(a). Because the clamping capacitor has much larger capacitance than the output capacitors of the switches, one of the switch voltage will be clamped at $\frac{V_{in}}{2}$ and the voltage of the other one can be discharged to zero by resonance with the leakage inducance. Then, the classical Phase Shift Control (PSC) can be applied into the converter just like the phase shift full bridge converter. After that, a lot of efforts have been made to improve the efficiency of the converter, and the main idea is to realize zero current switching (ZCS) in the lagging switches [4–9]. However, all the methods for ZCS need extra components to be added to the converter, which may introduce higher cost, complexity, and failure rate.

Additionally, research effort has also been made to the reliability aspect of the ZVS TL DC-DC converter. The two clamping diodes are removed from the converter in [10], and meanwhile the ZVS feature is still retained. Nevertheless, due to the lack of the clamping diodes, the flying capacitor voltage cannot be passively clamped to $\frac{V_{in}}{2}$ and a feedback control is needed to maintain its value. Thus, an extra isolated voltage sensor is necessary, which will introduce higher cost to the system. Instead, this paper proposes to remove only one of the clamping diodes, and retain the other one to passively clamp the voltage of the clamping capacitor. Therefore, no feedback control or voltage sensor is needed for the voltage balancing of the clamping capacitor. Moreover, with less components, the proposed converter can still retain the ZVS performance as long as the clamping capacitor is properly selected. The impact of the clamping capacitor on the ZVS performance is mathematically analyzed.

II. Operation Principle

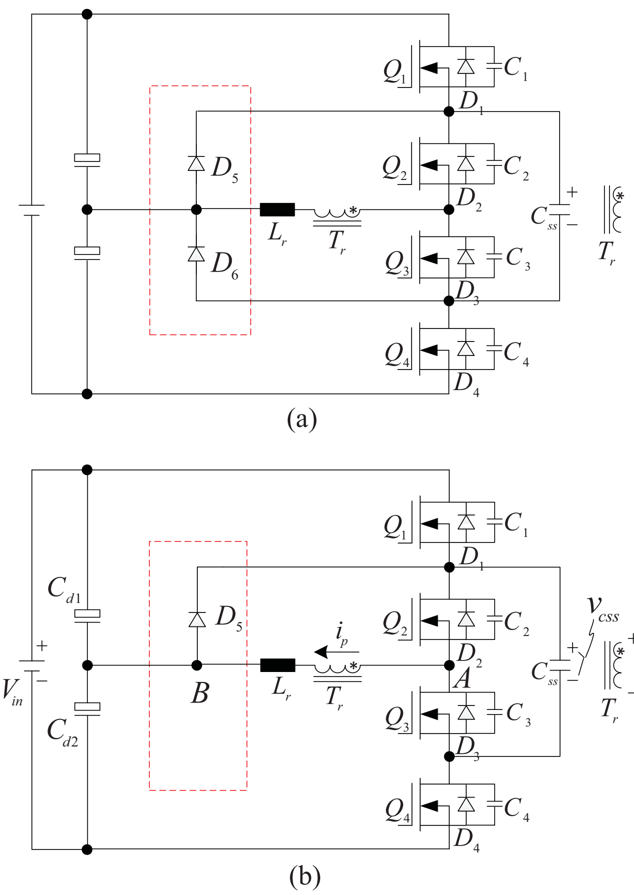


Fig. 1. (a) the basic ZVS TL DC-DC converter [3] (b) the proposed ZVS TL DC-DC converter.

The proposed ZVS TL DC-DC converter is shown in Fig 1(b), which is composed of power devices $Q_1 \sim Q_4$

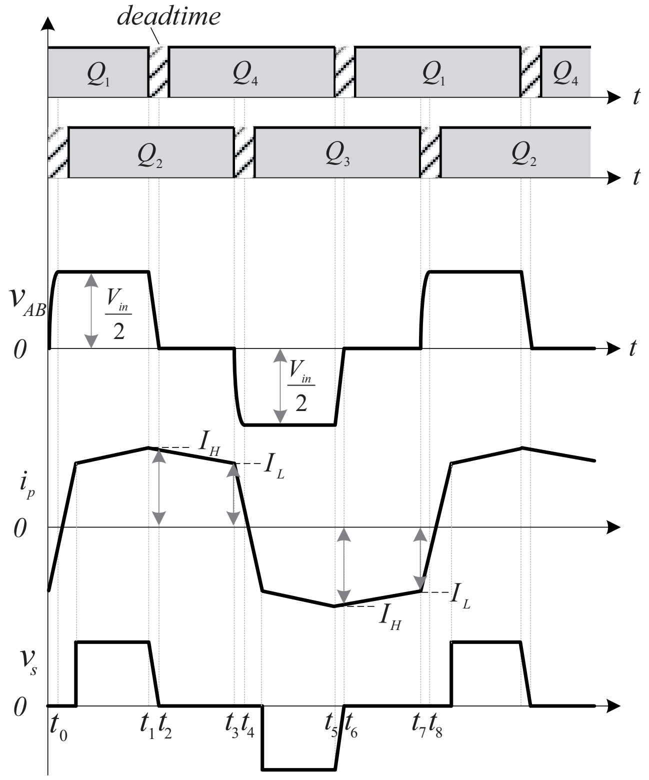


Fig. 2. Principle waveforms of the proposed converter.

with anti-parallel diodes $D_1 \sim D_4$ and parasitic output capacitors $C_1 \sim C_4$, clamping diode D_5, clamping capacitor C_{ss}, dividing capacitors C_{d1} and C_{d2}, transformer T_r, and leakage inductance L_r. Besides, i_p is the transformer current of the primary winding, v_{css} is the voltage of C_{ss}, and v_s is the transformer voltage on secondary side. Compared with the basic ZVS TL DC-DC converter shown in Fig. 1(a), the clamping diode D_6 is removed. In order to simplify the analysis, the secondary side of the transformer is not shown here, because it has no difference between the basic and the proposed converters.

The principle waveforms of the proposed converter are shown in Fig. 2. As seen, the phase shift modulation is employed, which divides a switching cycle into eight patterns, and the equivalent circuits in each pattern are shown in Fig. 3. The switch patterns are the same between the basic and proposed topologies except patterns (g) and (h). In pattern (g), the current is supposed to freewheel through Q_3 and D_6 as a zero pattern in the basic topology. But because D_6 is removed in the proposed topology, the current will circulate through Q_3, C_{ss}, Q_1, and C_{d1}. Despite, this pattern is still a zero pattern, because the voltage of C_{ss} approximates to $\frac{V_{in}}{2}$ and thereby the V_{AB} is still close to zero. In pattern (h), C_{ss} is supposed to be clamped by Q_1, D_6, and C_{d1} in the basic topology, while in the proposed topology, C_{ss} will be discharged for the freewheeling of the leakage inductance current. Overall, the charging of C_{ss} only happens during $t_2 \sim t_3$, where the voltage of C_{ss} is clamped to $\frac{V_{in}}{2}$ by D_5 and Q_4. While in other patterns, C_{ss} is only discharged, thus its voltage is passively kept at $\frac{V_{in}}{2}$ with a negative variation ΔV_{css}.

Soft-switching of $Q_1 \sim Q_4$ is another crucial factor to measure performace of the proposed converter. Actually, the function of the two clamping diodes is to clamp the maximum voltage of $Q_1 \sim Q_4$ to $\frac{V_{in}}{2}$, which has no direct impact on the switching performance. So as long as the clamping capacitor C_{ss} has a constant voltage $\frac{V_{in}}{2}$, the switching performance of $Q_1 \sim Q_4$ will be the same between the basic and proposed converters. But as analyzed above, due to the charging/discharging, C_{ss} will have a minus variation ΔV. As a result, in pattern $[t_1,\, t_2]$ the output capacitor C_4 of Q_4 can not be discharged to zero. Because $V_{C4}+V_{css}$ will be clamped to $\frac{V_{in}}{2}$ by D_5 and C_{d2}, V_{C4} can only decrease to $|\Delta V_{css}|$ by the resonance with the leakage inductance. While the ZVS of Q_1, Q_2 and Q_3 will not be influenced, because there is no diode clamping during the discharging of C_1, C_2, and C_3, as shown in pattern $[t_5,\, t_6]$, $[t_7,\, t_8]$, and $[t_3,\, t_4]$, respectively.

III. THEROTICAL ANALYSIS

The voltage variation of C_{ss} could affect the soft swithing performance of Q_4, which is therefore analyzed as following. The charging of C_{ss} only happens in pattern (b), and the voltage of C_{ss} is clamped at $\frac{V_{in}}{2}$. The discharging happens in four patterns $[t_1,\, t_2]$, $[t_5,\, t_6]$, $[t_6,\, t_7]$ and $[t_7,\, t_8]$. The equivalent circuits of the three patterns are redrawn in a simplier way as shown in Fig. 4 (a), (b), (c) and (d).

In pattern $[t_1,\, t_2]$, C_{ss} is paralleled with C_3. Because $C_{ss} \gg C_3$, the charging of C_3 can be neglected. Thus the amount of discharge in C_{ss} equals to C_4. Since the voltage of C_4 is dischaged from $\frac{V_{in}}{2}$ to 0 in this pattern, the voltage reduction in this pattern can be obtained as,

$$\Delta V_{css,1} = \frac{C_{oss} * \frac{V_{in}}{2}}{C_{ss}} \tag{1}$$

where C_{oss} is the value of the output capacitors $C_1 \sim C_4$. Actually, because $C_{ss} \gg C_4$ and $C_3 \approx C_4$, the discharging current of C_{ss} approximately equals to $\frac{i_p}{2}$, assuming i_p would not have big variation in this short duration in zero pattern. Then the voltage reduction in this pattern can also be derived as,

$$\Delta V_{css,1} = \frac{\frac{I_H}{2} * (t_2 - t_1)}{C_{ss}} = \frac{I_H * (t_2 - t_1)}{2 * C_{ss}} \tag{2}$$

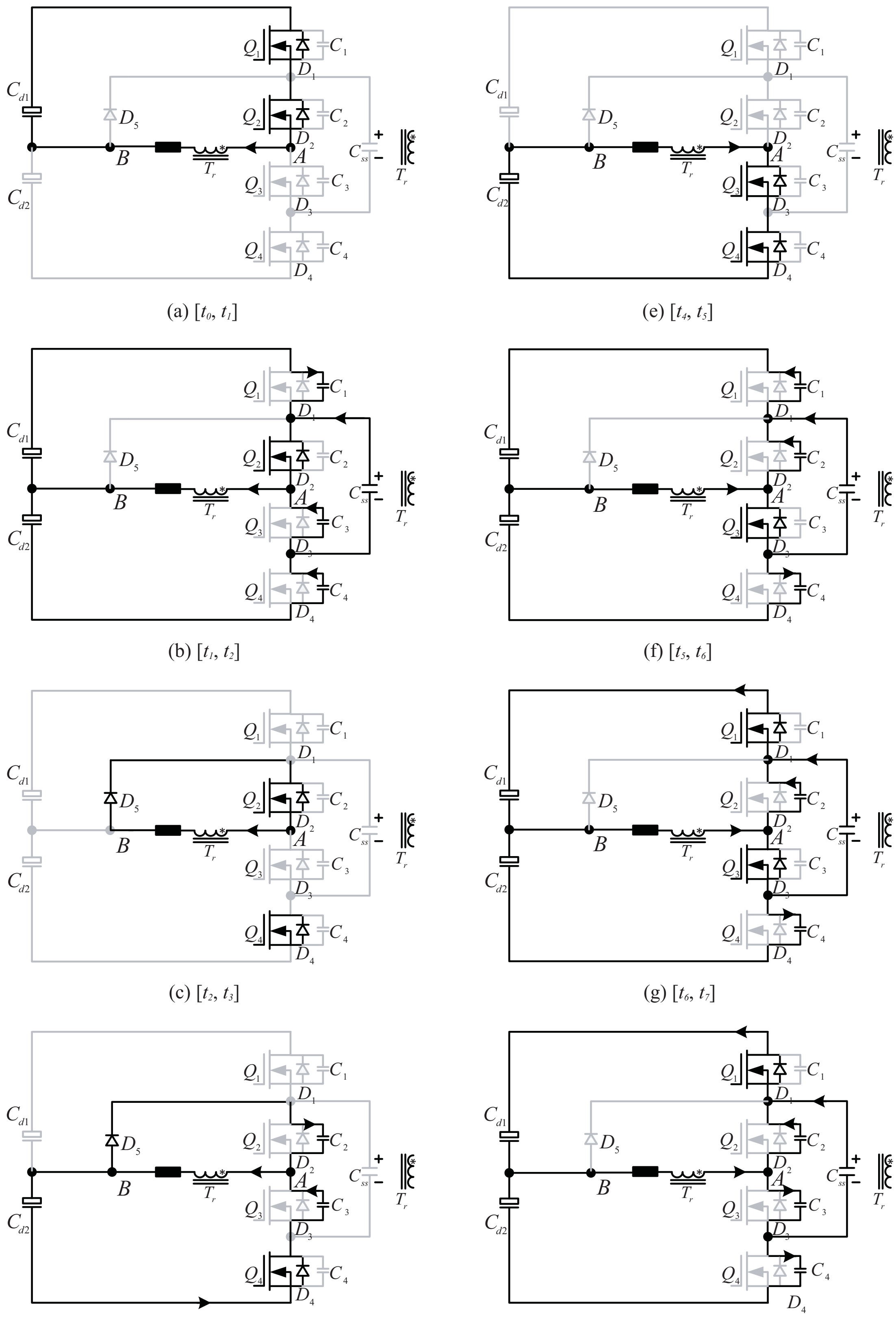
where I_H is the larger peak value of i_p, as shown in Fig. 2.

In pattern $[t_5,\, t_6]$, C_{ss} is paralleled with C_2, which is similar to the circuit in pattern $[t_1,\, t_2]$. Thus, the discharging current of C_{ss} approximately equals to $\frac{i_p}{2}$. Similarly, i_p would have negligible variation in this short duration in zero pattern. Then, the voltage reduction in this pattern can be obtained as,

$$\Delta V_{css,2} = \frac{(I_H + I_L) * (t_6 - t_5)}{4 * C_{ss}} \tag{3}$$

where I_L is the lower peak value of i_p.

In pattern $[t_6,\, t_7]$, C_4 is clamped by C_{ss}, the diode and the dc bus voltage. Thus, the charging current of C_4 can be neglected, and thereby the discharging current of C_{ss}



(a) $[t_0, t_1]$

(b) $[t_1, t_2]$

(c) $[t_2, t_3]$

(d) $[t_3, t_4]$

(e) $[t_4, t_5]$

(f) $[t_5, t_6]$

(g) $[t_6, t_7]$

(h) $[t_7, t_8]$

Fig. 3. Equivalent circuits in each pattern according to Fig. 2.

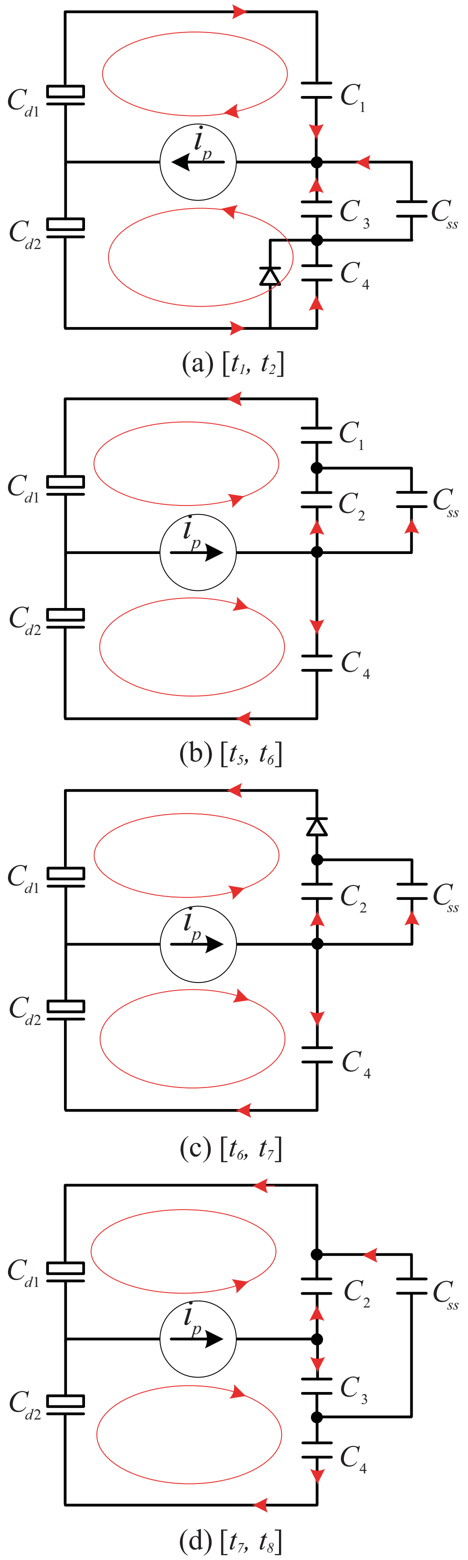


Fig. 4. The simplified equivalent circuits of (a) switch pattern [t_1, t_2], (b) switch pattern [t_5, t_6], (c) switch pattern [t_6, t_7], and (d) switch pattern [t_7, t_8] to illustrate the discharging of C_{ss}.

approximates to i_p. The voltage reduction in this pattern can be obtained as,

$$\Delta V_{css,3} = \frac{\frac{I_H+I_L}{2} * (t_7 - t_6)}{C_{ss}} \tag{4}$$

It is easy to obtain,

$$t_7 - t_6 \approx \frac{(1-D)T}{2} \tag{5}$$

where D is the duty cycle and T is the switching period of the converter. Subtituting (5) into (4), then (6) is obtained.

$$\Delta V_{css,3} = \frac{(I_H + I_L) * (1-D)T}{4 * C_{ss}} \tag{6}$$

In pattern [t_7, t_8], i_p is shared by C_2 and C_3. Because $C_2 = C_3$ and the summation of their voltage is clamped by C_{ss}, thus the discharging current of C_2 equals to $\frac{i_p}{2}$. Meanwhile, the C_4 is clamped by the dc bus voltage and C_{ss}, so the charging current of C_4 can be neglected, which means the charging current of C_{d1} approximately equals to i_p. Then according to Kirchhoff's current law, the discharging current of C_{ss} approximates to $\frac{i_p}{2}$. Besides, i_p will decreases from I_L to 0. Thus, the voltage reduction in this pattern can be approximately calculated as,

$$\Delta V_{css,4} = \frac{\frac{I_L}{4} * (t_8 - t_7)}{C_{ss}} = \frac{I_L * (t_8 - t_7)}{4 * C_{ss}} \tag{7}$$

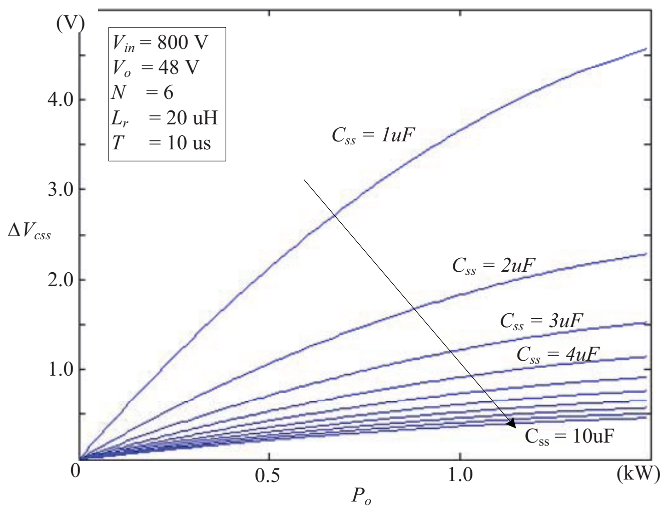


Fig. 5. ΔV_{css} vs P_o results to show the ZVS performance of the proposed converter at (a) full load (b) 20 % load.

Because $(1-D)T \gg (t_2-t_1), (t_6-t_5), (t_8-t_7)$, therefore, the total voltage variation can be obtained as,

$$\Delta V_{css} \approx \Delta V_{css,3} = \frac{(I_H + I_L) * (1-D)T}{4 * C_{ss}} \tag{8}$$

Assuming the ripple of the output current is zero, (9) can be obtained.

$$I_H = I_L = \frac{I_o}{n} \tag{9}$$

where I_o is the output current and n is the turns ratio of the transformer. Considering the loss of duty cycle during the leakage inductance current commutation, the duty cycle can be calculated as,

$$D = \frac{V_o * n}{V_{in}/2} + \frac{L_r * \frac{2*I_o}{n}}{V_{in}/2 * T/2} \tag{10}$$

where V_o is the output voltage. Besides, the output power can be easily expressed as,

$$P_o = V_o * i_o \tag{11}$$

Substituting (9),(10), and (11) into (8), it results in,

$$\Delta V_{css} \approx \frac{n * I_o * V_{in} * T^2 - 2 * n^2 * P_o * T^2 - 8 * L_r * {I_o}^2 * T}{2 * n^2 * V_{in} * C_{ss} * T} \tag{12}$$

Thus, the voltage variation of C_{ss} can be affected by the load, switching period, turn ratio of the transformer, leakage inductance, and capacitance of C_{ss}. ΔV_{css} as a function of P_o is shown in Fig. 5, where the conditions are listed in the figure and the arrow points to the direction of the C_{ss} increasing. As seen, ΔV_{css} will increase as P_o increases but decrease as C_{ss} increases. In the condition listed in the figure, ΔV_{css} will be 0.5 V as a maximum value when the power is 1.5 kW and $C_{ss} = 10uF$, where the turn on loss of Q_4 is expected to be very small.

IV. SIMULATION RESULTS

Simulation results are obtained to verify the feasibility of the proposed converter and the theoretical analysis, where the secondary side of the transformer is a full bridge diode rectifier with LC filter. The parameters are listed in Table I.

TABLE I. PARAMETERS USED FOR SIMULATIONS.

Parameters	Values
Nominal power	1500 W
DC bus voltage V_{in}	800 V
Output voltage v_o	48 V
Turn ratio of the transformer	6:1
Leakage inductance L_r	20 μH
Switching frequency f_s	100 kHz
Capacitance of C_{ss}	10 μF
Output filter inductor L_o	5 μH
Output filter capacitor C_o	1000 μF

As seen in Fig.6, the clamping capacitor C_{ss} is passively clamped at 400 V with a voltage varation 0.5 V, which matches with the mathematical derivation in Section III as shown in Fig. 5. Besides, the ZVS switching performance of Q_1 does not degrade, while that of Q_4 changes as illustrated later. The zoomed figures of Q_1 and Q_4 in their turn on transient

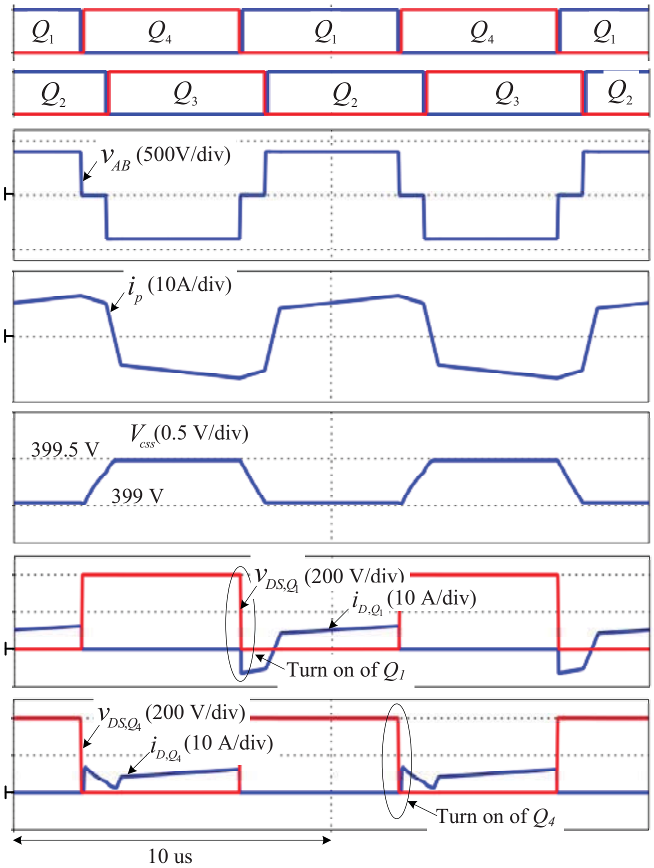


Fig. 6. Simulated results to show the voltage variation of the C_{ss} and ZVS performance of Q_1 and Q_4 in the proposed converter.

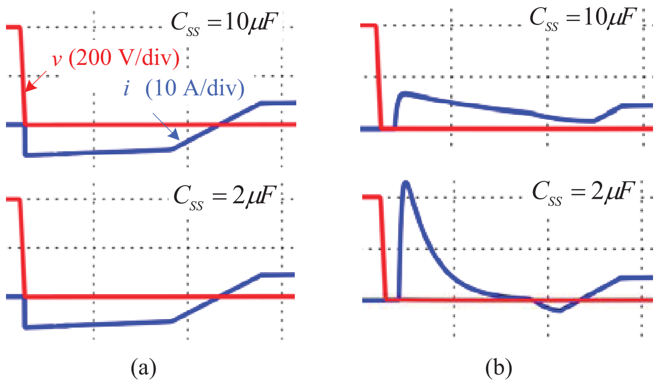


Fig. 7. Impact of the C_{ss} on the ZVS performance of (a) Q_1 and (b) Q_4 in proposed converter.

are shown in Fig. 7, where two cases with different C_{ss} are taken for comparison. Fig. 7(a) indicates that the ZVS performance of Q_1 will not degrade although D_6 is removed. Fig. 7(b) however illustates that the capacitance of C_{ss} affects the ZVS performance of Q_4 relatively significantly. Due to the clamping of Q_5, the output capacitor of Q_4 will retain ΔV_{css} after resonance with the leakage inductance during the turn on transient. Then this amount of voltage will be discharged by hard switching. As analyzed in Section III, a smaller C_{ss} will lead to larger ΔV_{css}, thus a larger discharging current is observed in the bottom subfigure of Fig. 7(b). Despite, in the condition listed in Table I, a 10 μF C_{ss} can ensure a low ΔV_{css} of 0.5 V, so the hard switching of Q_4 at this voltage level can be neglected.

V. CONCLUSIONS

A new ZVS three-level DC-DC converter is proposed, which has a reduced number of clamping diodes compared with the classical topology. So the cost and power loss due to the reverse recovery of the diode are expected to be lower, and the reliability of the converter is expected to be improved. Although one diode is removed, the proposed converter can still have the clamping capacitor votlage passively clamped at half of the dc bus votlage. Moreover, the proposed converter retains the ZVS performance as the classical topology by properly sizing the clamping capacitor. The impact of the clamping capacitor on the ZVS performance is mathematically analyzed. The feasibility of the proposed converter is verified by a case study of 1.5 kW three-level converter.

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