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Published in:
Proceedings of IECON 2016: 42nd Annual Conference of the IEEE Industrial Electronics Society

DOI (link to publication from Publisher):
10.1109/IECON.2016.7793891

Publication date:
2016

Document Version
Early version, also known as pre-print

Elimination of Zero Sequence Circulating Current Between Parallel Operating Three-level Inverters

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***Abstract*—In order to suppress the zero sequence circulating currents (ZSCCs) between parallel operating three level voltage source inverters with common AC and DC buses, a common mode voltage reduction PWM (CMVR-PWM) technique and neural point potentials (NPPs) control based method is proposed in this paper. An equivalent model of ZSCC is developed, and two excitation sources of ZSCC, differences of common mode voltages (CMVs) and NPPs between paralleled inverters, are analyzed. A CMVR-PWM method is investigated to reduce the CMV, and a simple electric circuit is adopted to control the NPPs. With this two strategies, ZSCCs between parallel inverters can be eliminated effectively. This strategy has the advantage of without carrier synchronization and can be utilized to parallel operating inverters with different types of filter. Simulation result validate the proposed ZSCC elimination schemes.**

I. INTRODUCTION

In the past few years, renewable energy generation is increasing developed, especially the photovoltaic power generation and wind power generation [1]. Three phase voltage source inverter (VSI) is an important equipment for renewable energy sources connecting to utility grid. Because of the limitation of existing devices, switching frequency and many other constraining factors, inverters parallel operating is an attractive solution to extend power capacity of inverters. It also has the advantage of good fault-tolerant ability and can be used in the application of high reliability situation. However, when the inverters are connected with AC and DC bused directly, circulating currents are generated due to the small total impedance within the zero-sequence circuit of parallel inverter systems and causes some problems, such as unbalanced current distribution, output current distortion and system loss increasing etc.

In order to reduce the ZSCC, many researches have been carried out in the past few years. Before 2002, methods concerning ZSCC between parallel inverters with common AC and DC buses are *high impedance methods*[2][3] and *synchronized control methods*[4][5]. However, in the high impedance approach, the overall parallel system is bulky and costly because of additional reactors in main circuit. The synchronized control approach is not suitable for modular inverters design. When more inverters are in parallel operating, the system becomes very complicated to design and control. In 2002, Z.Ye analyzed the model of ZSCC between parallel operating inverters, and pointed out that the exciting source is the difference of CMVs. The ZSCC feedback control is also investigated [6]. Then, many hybrid methods are developed. *Increasing impedance and reduce CMV methods* [7-10]: In [7], a common mode choking coil is used to increase the impedance of ZSCC, and DPWM method is utilized to reduce the CMV. In [8-10], interleaving inductance and DPWM methods are used. However, there are open loop control methods. And carrier synchronization is essential. *Method of Reduce CMV and ZSCC feedback control* [11-15]: In these papers, AZPWM, RSPWM and SHEPWM are used to reduce the amplitude or frequency of the CMV fluctuations, and ZSCC feedback control, similar with [6], is utilized. However, for two level inverters, the CMV reduced PWM will cause big harmonic current distortion and carrier synchronization is also essential. The approaches mentioned above are focus on two-level inverters. But the approaches for three level inverters are very few. For three level inverters, the exciting sources are more complicated, including CMV, neural point potential and hybrid source. For instance, the CMVs of three level inverters with SVPWM or DPWM method are step change, and have many harmonic components. With regard to the elimination of high-frequency and low-frequency harmonic composition of ZSCCs, [16-17] proposed a modified LCL filter to eliminate the former, and a ZSCC control loops to suppress the latter. Moreover, a modified modulation method with two level SVPWM similarly modulating wave is used to reduce the high-frequency components of ZSCC caused by CMV. This approach can be effective to eliminate the ZSCC of three level inverters, and carrier synchronization is not essential. However, this approach can only be used in the situation of inverters with LCL or LLCL filters.

In order to suppress the ZSCCs of parallel operating three level inverters with common both AC and DC buses, this paper proposes an CMVR-PWM and ZSCC feedback control based method. A CMVR-PWM method is proposed to eliminate the high-frequency components, and ZSCC feedback control is put forward to suppress the low-frequency components. Furthermore, the ZSCC feedback control is carried out by the control of the NPPs. The effectiveness of the proposed strategy is validated by simulation. Compared to the existing strategies, this strategy has the advantage of without carrier

Supported by "the Fundamental Research Funds for the Central Universities" (ZYGX2015J075).

synchronization and can be utilized to inverters with different types of filter.

II. Modeling of Zero Sequence Circulating Current

This paper considers two three-phase three-level T-type VSIs parallel operating for example. As illustrated in Fig.1, two inverters with the same structures are connected with both DC and AC power supply directly. C denotes the DC-bus capacitor. L_{v1} and L_{v2} are the inverter side filter inductance. L_{g1} and L_{g2} are the grid side filter inductance. R_1, R_2, R_{g1} and R_{g2} are equivalent series resistance (ESR) of three-phase inductance L_1, L_2, L_{g1} and L_{g2} respectively. C_f denotes the filter capacitor. O_1 and O_2 denote the neural point of inverter 1# and inverter 2# respectively. n denotes the potential of the star point of utility grid.

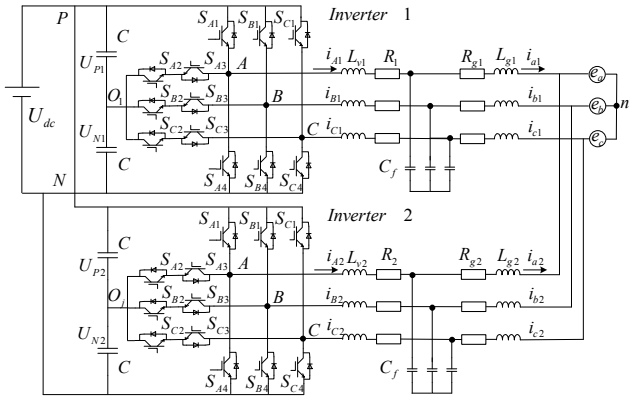


Fig.1 Structure of proposed parallel system

In order to simplify explanation, assume that the inductor current and the dc bus voltage are constant in a switch cycle, and ignore the influence of dead time. According to the Kirchhoff's Voltage Law (KVL), the following equation can be obtained:

$$\begin{aligned}&\frac{U_{dc}}{2}-\frac{\Delta U_1}{2}+U_{m1O1}+L_{v1}\frac{di_{m1}}{dt}+R_1 i_{m1}+L_{g1}\frac{di_{n1}}{dt}+R_{g1}i_{n1}=\\&\frac{U_{dc}}{2}-\frac{\Delta U_2}{2}+U_{m2O2}+L_{v2}\frac{di_{m2}}{dt}+R_2 i_{m2}+L_{g2}\frac{di_{n2}}{dt}+R_{g2}i_{n2}\end{aligned} \tag{1}$$

Where, i_{mj} is the inverter-side phase current of the jth inverter; i_{nj} is the grid-side phase current of the jth inverter; U_{mjOj} is the voltage of phase leg mj to the neural point Oj; $\Delta U_1=U_{P1}-U_{N1}$ and $\Delta U_2=U_{P2}-U_{N2}$ represent the voltage difference of the DC capacitor; $m\in\{A,B,C\}$; $n\in$ {a, b, c}; $j\in\{1,2\}$.

According to the definition of ZSCC[6], the ZSCC of the proposed parallel system can be obtained as follows:

$$\begin{aligned}&i_{01}=(i_{A1}+i_{B1}+i_{C1})=(i_{a1}+i_{b1}+i_{c1})=-i_{02}\\&=-(i_{A2}+i_{B2}+i_{C2})=-(i_{a2}+i_{b2}+i_{c2})\end{aligned} \tag{2}$$

Where, i_{0j} denotes the ZSCC of inverter j^{th}.

CMV of the inverter is defined as the potential of the star point n of the load to the neural point O. It can be expressed as follows:

$$U_{nOj}=\frac{U_{AjOj}+U_{BjOj}+U_{CjOj}}{3} \tag{3}$$

Where, U_{nOj} is the CMV of the j^{th} inverter.

The following ZSCC equation can be obtained by adding the three equations from (1) together and substituted by (2) and (3):

$$\begin{aligned}&(L_{v1}+L_{g1}+L_{v2}+L_{g2})\frac{di_0}{dt}+(R_1+R_{g1}+R_2+R_{g2})i_0\\&=\frac{3}{2}(\Delta U_1-\Delta U_2)+3(U_{nO2}-U_{nO1})\end{aligned} \tag{4}$$

As $\Delta U_1=U_{P1}-U_{N1}$, $\Delta U_2=U_{P2}-U_{N2}$, $U_{dc}=U_{P1}+U_{N1}$ and $U_{dc}=U_{P2}+U_{N2}$, the following equation can be obtained:

$$\begin{aligned}&(L_{v1}+L_{g1}+L_{v2}+L_{g2})\frac{di_{01}}{dt}+(R_1+R_{g1}+R_2+R_{g2})i_{01}\\&=3(U_{N2}-U_{N1})+3(U_{nO2}-U_{nO1})\end{aligned} \tag{5}$$

According to (5), the transform function of ZSCC can be obtained as follows:

$$i_{01}(s)=\frac{3(U_{N2}(s)-U_{N1}(s))+3(U_{nO2}(s)-U_{nO1}(s))}{(L_{v1}+L_{g1}+L_{v2}+L_{g2})s+(R_1+R_{g1}+R_2+R_{g2})} \tag{6}$$

Formula (4) or (5) is the differential equation model of ZSCC between paralleled inverters. The equivalent circuit of circulating current can be obtained, as shown in Fig.2.

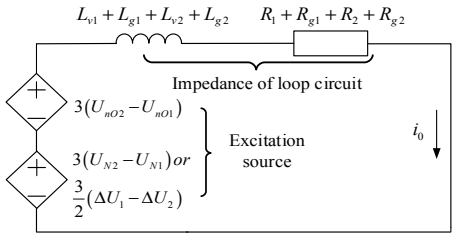


Fig.2. Equivalent circuit of ZSCC

According to the analysis above, the following conclusions can be obtained:

1)The ZSCC is related to the impedance of loop circuit and the excitation source.

2)Since the ESR of the inductance is very small and the inductance of loop circuit can provide high impedance only in high frequency, the loop circuit of ZSCC is characteristic as a low-pass-filter.

3)Differences of CMVs and NPPs between parallel inverters are the excitation sources.

4)ZSCC can be eliminated by the method of increasing the impedance of loop circuit and decreasing the excitation sources.

Since the approach of increasing the impedance of loop circuit always makes the system costly and bulky. This paper investigates the approach of decreasing the excitation sources.

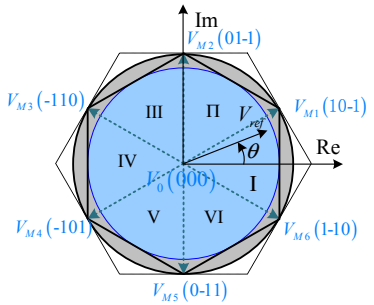
III. Strategy of Zero Sequence Circulating Current Elimination

According to the analysis in Section II, the excitation sources of ZSCC are the differences of CMVs and NPPs between paralleled inverters. The strategy of zero sequence circulating current elimination is based on CMVR-PWM and Neural point potentials control.

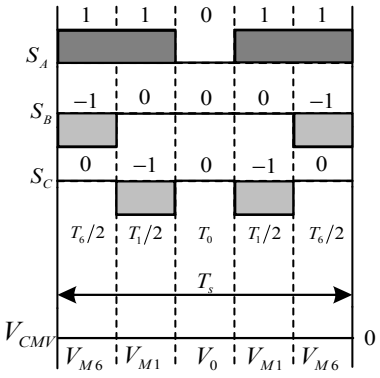
A. CMVR-PWM

In order to acquire a good performance of output voltage waveform, the voltage of neural points must maintain at approximate $U_{dc}/2$, thus, the neural point voltages error must be very small and the difference of CMVs is the primary cause of ZSCC. However, the CMV will change for 6 times in a switching period when standard SVPWM method is adopted, and it give rise to big ZSCC.

According to the analytical result in [18], a CMVR-PWM method--2MV1Z(which takes two adjacent medium vectors and a zero vector to synthesize the target vector), can eliminate CMV effectively. This paper will use 2MV1Z method to decrease the excitation sources.



(a) Voltage vector space



(b) Pulse pattern

Fig.3. Voltage vector space and pulse pattern of 2MV1Z

Vector space of 2MV1Z method is shown in Fig.3(a), its voltage vector space is consisted by six medium vectors and a zero vector and the five stage pulse pattern is adopted. As we can see from the Fig.3(b) that zero CMV can keep at zero in a switching period. Its pulse patterns in every sector are summarized in Table I.

TABLE I. Pulse Patterns of 2MV1Z Method

Sector	θ	Pulse Pattern
I	-30° < θ ≤ 30°	1-10 →10-1 →000 →10-1 →1-10
II	30° < θ ≤ 90°	10-1 →01-1 →000 →01-1 →10-1
III	90° < θ ≤ 150°	01-1 →-110 →000 →-110 →01-1
IV	150° < θ ≤ 210°	-110 →-101 →000 →-101 →-110
V	210° < θ ≤ 270°	-101 → 0-11 →000 →0-11 →-101
VI	270° < θ ≤ 330°	0-11 →1-10 →000 →1-10 →0-11

In order to evaluate the other performance of 2MV1Z, DC voltage utilization rate and harmonic distortion factor will be discussed.

DC voltage utilization rate is an important indicator for the performance of a modulation algorithm. It represents the magnitude range of reference output for AC voltage at a certain DC voltage. Linear modulation ratio M, defined in (7), is commonly used to evaluate DC voltage utilization rate. Bigger values of M indicate better performance.

$$M = \frac{\sqrt{3}\,|V_{ref}\,|}{U_{dc}} \tag{7}$$

According to (7), the linear modulation ratio of standard three-level and two-level SVPWM are range from 0 to 1.

The reference vector that the 2MV1Z algorithm constructs must be within the solid hexagonal zone. Its linear modulation area is the incircle (the blue zone in Fig.3(a)) within the solid hexagonal zone. Thus, the linear modulation ratio of the 2MV1Z algorithm can be obtained:

$$0 \le M_{2MV1Z} \le \frac{\sqrt{3}}{2} \tag{8}$$

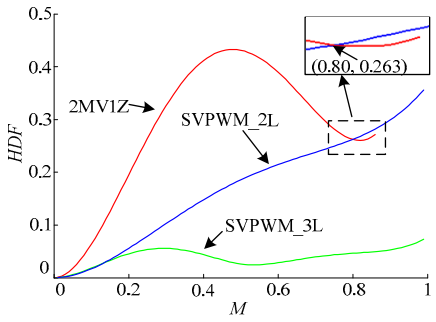


Fig.4. HDF curves of all the discussed PWM methods

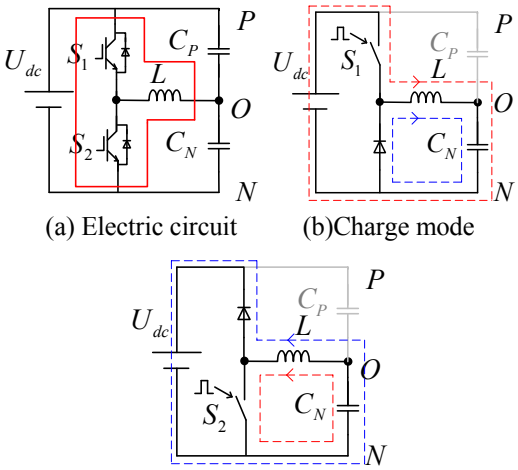
Harmonic Distortion Factor (HDF) is defined in [20] to evaluate the harmonic component of AC current output. Smaller values of HDF indicate better performance. HDF analysis is a carrier-based PWM tool which is widely utilized to illustrate and compare the performance characteristics of

various PWM methods. HDFs of two-level and three-level SVPWM are introduced to compare with 2MV1Z.

As shown in Fig.4, the HDF of each method is unique. In the full linear modulation range, the three-level SVPWM methods provide lower HDF than the 2MV1Z methods. And the HDF performance of three-level SVPWM is better than two-level SVPWM. For M>0.8, the 2MV1Z methods even shows a better performance than two-level SVPWM method.

B. *Neural point potentials control*

As discussed above, 2MV1Z method is utility to reduce CMV and eliminate the ZSCC by decreasing the differences of CMVs between parallel operating inverters. Although it can maintain the CMV at zero most of the time, the ZSCC caused by the random and non-designed CMV fluctuations(caused by the dead time) may accumulate. So, zero sequence circulating current feedback control is essential.



(a) Electric circuit (b)Charge mode

(c)Discharge mode

Fig.5. The neural point potentials control circuit

According to the conclusion in Section II, another exciting source is the differences of the NPPs. Although it should be very small for good voltage waveform, it can be used to eliminate the ZSCC by adjusting its magnitude and action time. In this paper, an electric circuit, as shown in Fig.5, is used to control the NPPs.

As shown in Fig.5(a), the NPP control circuit is consist of two IGBTs (S_1 and S_2) and an inductance (L). The two IGBTs operate in complementary mode. When S_2 is off, the equivalent circuit is shown in Fig.5(b), C_N can be charged via L by controlling S_1 with PWM method, and the NPP will arise. Similarly, When S_1 is off, the equivalent circuit is shown in Fig.5(c), C_N can be discharged via L by controlling S_2 with PWM method, and the NPP will be lowered. Since the sum of the voltages of capacitor is equal to U_{dc}, the upper capacitor C_P can be seen as parallel with C_N. So, the electric circuit is a typical Buck/Boost bidirectional circuit and it is very easy to design the parameter of inductance L.

According to (4) and Fig.5, when the ZSCC is bigger than zero, the process to eliminate the ZSCC is shown as follow:

Case 1: $i_0 > 0 \rightarrow$ turn S_2 off $\rightarrow$ control $S_1 \rightarrow U_{N1} \uparrow \rightarrow U_{P1} \downarrow \rightarrow \Delta U \downarrow \rightarrow i_0 \downarrow$

Similarly, when the ZSCC is smaller than zero, the process to eliminate the ZSCC is shown as follow:

Case 2: $i_0 < 0 \rightarrow$ turn S_1 off $\rightarrow$ control $S_2 \rightarrow U_{N1} \downarrow \rightarrow U_{P1} \uparrow \rightarrow \Delta U \uparrow \rightarrow i_0 \downarrow$

C. *Control strategy for ZSCC elimination*

In conclusion, zero sequence circulating current feedback control is executed by this simple NPP control circuit. It is worth mentioning that ΔU must be limited in a small range to avoid distorting output voltage waveform. Controlling zero sequence circulating current is mainly by changing action time of ΔU.

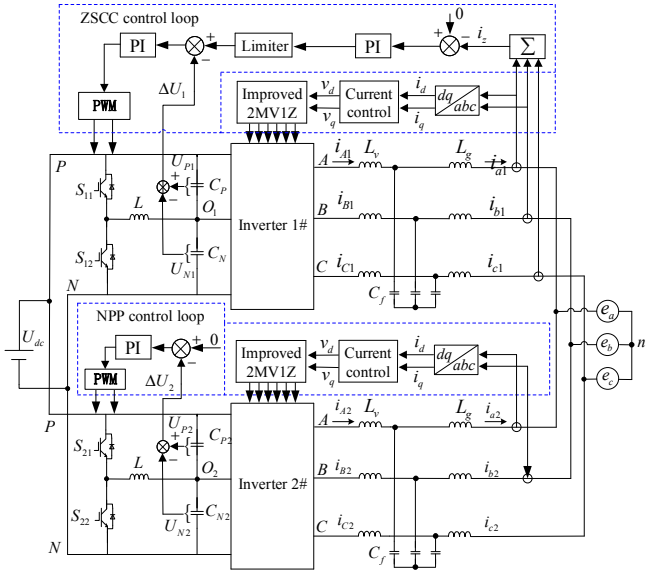


Fig.6. Block diagram of ZSCC feedback control

Block diagram of ZSCC feedback control is shown in Fig.6. For the three phase inverter, ZSCC is the sum of three gird-side currents. So, three current sensors are essential. ZSCC control loop is a double loop, inner loop is the neural point potentials control loop, outer loop is the zero sequence circulating current control loop. The set point of outer loop is zero, and the output of outer loop controller is set as the set value of inner loop via a limiter. The control command of the total control loop is the duty cycle of the switches in electric circuit. This double-loop design can realize the control of the NPP and ZSCC. Note that when N inverters paralleled, just N-1 inverters should control ZSCCs, the ZSCC control of the N^{th} inverter is not essential [6]. Furthermore, each ZSCC control loops are implemented within individual inverters, and does not need any additional interconnected circuits, even carrier synchronization busses. It is very convenient for modular design.

As from Fig,2 and Fig.6, there is no C_f in the ZSCC model and control loop. So, the proposed method is not affected by C_f. That means that the proposed method can be utilized to the applications of paralleled inverters with different types of filter.

Taking inverter 1# as example, we consider the effect of ΔU_1 on the i_{01}, the ΔU_1 and (U_{nO2}- U_{nO1}) can be seen as disturbances. In order to simplify the analysis, disturbances can be regarded as zero. So, the control block diagram is shown in Fig.7.

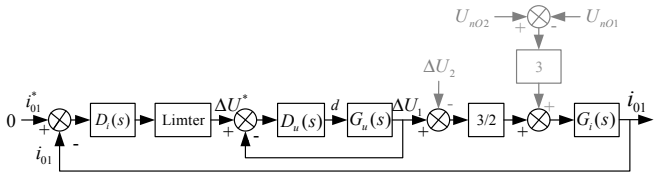


Fig.7. the control block diagram

$G_i(s)$ can be obtained from (5), and $G_u(s)$ is the typical transform function of Buck/Boost bidirectional circuit. The controller adopts Proportional-Integral(PI) control. The control loop, shown in Fig.7, is a typical cascade control and parameters of PI can be easily obtained. The control bandwidth of the zero sequence circulating current can be designed to be high and a strong loop suppressing the ZSCC can be achieved.

IV. Simulation Result

A MATLAB/Simulink model is set up to verify the analytical results. Inverters parameters and control parameters are shown in Table II.

TABLE II. Parameters of Simulink Model

Parameters	Value
Rated power	10kW
DC voltage	U_{dc}=600V
Grid frequency	50Hz
AC voltage	220V(line to line)
Switching frequency	10kHz
Inverter side inductance	L_{v1}= L_{v2}=1.2mH
Grid side inductance	L_{g1}= L_{g2}=0.2mH
Filter capacitor	C_{f1}= C_{f2}=20μF
Damping Resistance	0.5Ω(in series with C_f)
Buck/Boost inductance	1mH

In order to valid the effective of the proposed strategy of ZSCC elimination, a simulation result is shown in Fig.8 and Fig.9.

Fig.8 shows the simulated waveforms of 2MV1Z method without ZSCC control. The phase currents are distorted by ZSCC. And the ZSCC is fluctuation in low frequency. The high frequent parts of ZSCC are eliminated effectively by 2MV1Z method.

Fig.9 shows the simulated currents of 2MV1Z method with ZSCC control. It can be seen that the ZSCC is almost completely eliminated and the phase currents shows very well. The RMS value of i_{01} in Fig.9 is 329mA. The total harmonic distortion of i_{a1} is 2.09%, the total harmonic distortion of i_{a2} is 2.16%.

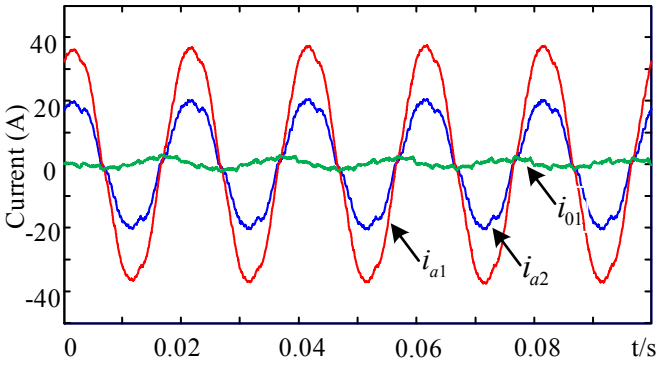


Fig.8. Simulated currents of 2MV1Z method without ZSCC control

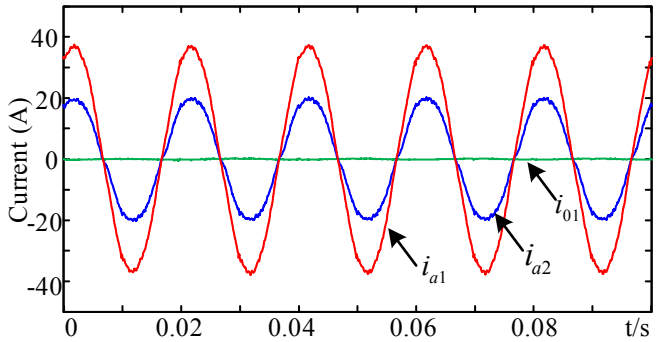


Fig.9. Simulated currents of 2MV1Z method with ZSCC control

V. Conclusion

This paper proposed a ZSCC eliminating method for parallel operating three level inverters with common both AC and DC buses. A CMVR-PWM is investigated to reduce the CMV, and a simple electric circuit is adopted to control the neural point potentials. ZSCC between paralleled inverters is eliminated effectively with these two strategies. Simulation result validated the proposed ZSCC elimination schemes. This method has the advantage of simple implementation and carrier synchronization is not essential. Furthermore, the application of this method is not limited by the filter, it can be utilized to the applications of paralleled inverters with different types of filter.

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