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A Multi-Pulse Front-End Rectifier System with Electronic Phase-Shifting for Harmonic Mitigation in Motor Drive Applications

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***Abstract*—In this paper, an electronic phase-shifting strategy has been optimized for a multi-parallel configuration of line-commutated rectifiers with a common dc-bus voltage used in motor drive application. This feature makes the performance of the system independent of the load profile and maximizes its harmonic reduction ability. To further reduce the generated low order harmonics, a dc-link current modulation scheme and its phase shift values of multi-drive systems have been optimized. Analysis and simulations have been carried out to verify the proposed method.**

Keywords—active filter; adjustable speed drive; electronic inductor; harmonic elimination; rectifier

I. INTRODUCTION

Modern power electronics have revolutionized the course of motor drive industry by introducing the Adjustable Speed Drive (ASD) technology (also known as Variable Speed Drives (VSD) or Frequency Converters (FC)). An ASD improves energy efficiency of a system by controlling the speed of motor at an optimal speed and/or torque. Hence, the energy consumption of the motor is reduced from full power to a partial power for the same performance (i.e., speed and/or torque). However, ASD systems have witnessed as one of the major sources of harmonics, which may deteriorate the grid power quality. From a power quality point of view, the generation of current harmonics from an ASD system has become a major concern as they may lead to high losses and stability issues in the grid [1],[2].

Typically, the majority of three-phase motor drive applications are equipped with a double-stage power converter. As Fig. 1(a) shows, the first stage employs a three-phase line commutated rectifier such as diode-rectifier (DR) or Silicon Controlled Rectifier (SCR) to perform AC to DC conversion and a voltage source inverter to convert DC back to AC at the demanded voltage and frequency. This configuration provides a unidirectional power flow and is the most common topology employed in industrial and commercial drives. Employing line commutated rectifier at the front-end stage imposes high level of input current harmonics. Although many harmonic mitigation solutions have been introduced [3], [4], most ASD manufacturers are still using conventional passive filtering technique (e.g., using inductor at ac-side or dc-side as shown in Fig. 1(a)) as a simple, reliable and an effective solution to some extent [4].

With the global shift towards energy saving, more ASD systems are adopted as an energy efficient solution. However, the undesirable effect of generated harmonics can be substantially elevated when the number of industrial drives is increased at the Point of Common Coupling (PCC). Therefore more advanced filtering method is required rather than using passive inductors (Fig. 1 (a)). Notably, a proper arrangement of these nonlinear loads can contribute to an effective harmonic mitigation [5]-[8]. In fact, this idea was first introduced in multi-pulse rectifiers using phase-shifting transformers [10]. Many ASD manufacturers advocate the use of 12-pulse or 18-pulse phase-shifting transformer, mainly because of its simplicity and reliability [10], [11].

Transformer-based multi-pulse rectifiers significantly impair the power density of ASD systems and are costly. In addition, their performance depends on the load profile. For instance depending on the output power level a 12-pulse rectifier system can obtain a Total Harmonic Distortion (THD_i) in the range of $10\% < THD_i < 15\%$ [7], [10], [11]. In the real-world situation most ASD systems operate in partial loading conditions depending on the application demands, locations and even safety margins. Operating at partial loading conditions adversely affect the ASD system THD_i as the effective impedance of the passive filter is proportional to the load current (output power). Therefore, the input current THD_i and power factor (λ) will be worsened when the rectifier is partially loaded. Fig. 1(b) exemplifies the input current waveforms of a conventional ASD system under different loading conditions when the passive filter inductor is placed at the dc-side. In practice the inductance value is selected in the range of 3-5% (e.g., L_{dc} = 2 mH) [12]. Thus, maintaining the THD_i and the power factor (λ) independent of the load profile is very beneficial.

In this paper an electronic phase-shifting method (transformer-less) is proposed based on having multiple line-commutated rectifiers. The proposed topology has a common dc-bus, which makes it suitable for single and multi-drive configuration especially for medium and high power applications where employing a phase-shifting transformer is

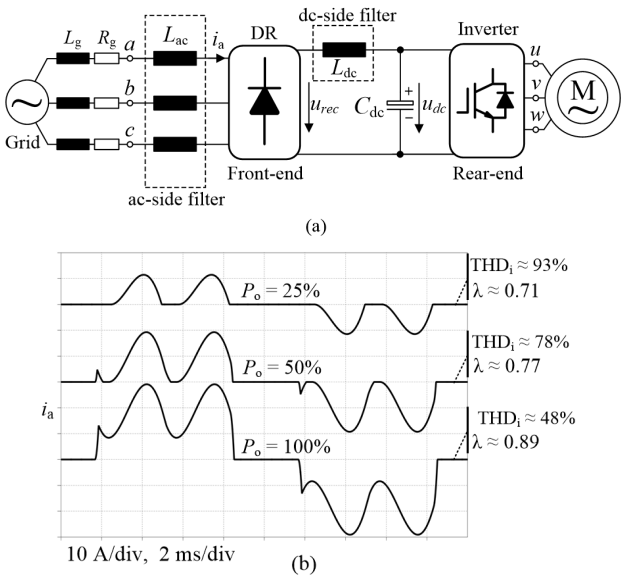

Fig. 1: Standard adjustable speed drive system with double stage conversion: (a) system block diagram, (b) input current waveforms at different loading conditions when dc-side passive filtering is utilized (L_{dc} = 2 mH, see Table I for the applied system parameters).

quite bulky. In addition, a current modulation technique at the dc-link using Electronic Inductor (EI) technique is employed which substantially improves the input current quality. The proposed technique is an enhanced method based on previous introduced strategies by the authors in [5]-[8], [12]. The introduction of a common dc-bus in this method makes the performance of the system independent of the load profile. The proposed controller and topology have been analyzed and simulated in order to verify the proper operation of the multi-rectifier system.

II. Proposed Harmonic Mitigation Method

The proposed method comprises of two features as illustrated in Fig. 2. First, an electronic phase-shifting is proposed based on using multiple line-commutated rectifiers with a common dc-bus. The phase-shifting capability can improve the input current quality. Secondly, a current modulation technique is applied, which can further reduce the low order harmonics and significantly improve the current THD$_i$. The novel advantage of the proposed topology lies in its configuration and control strategy, which enables the system to operate properly with a common dc-link (see Fig. 2(b)). The new configuration with the common dc-bus not only can improve the current quality at different loading conditions, but also can share the dc-link current among different numbers of motor drives (Fig. 2(a)).

A. Electronic Phase Shifting Technique

The harmonic elimination based on phase-shifting the input currents is a well-known technique which traditionally has been employed in multi-pulse rectifier systems using phase-shifting transformers [10], [11]. The novelty of the proposed method is applying the same principle excluding the use of

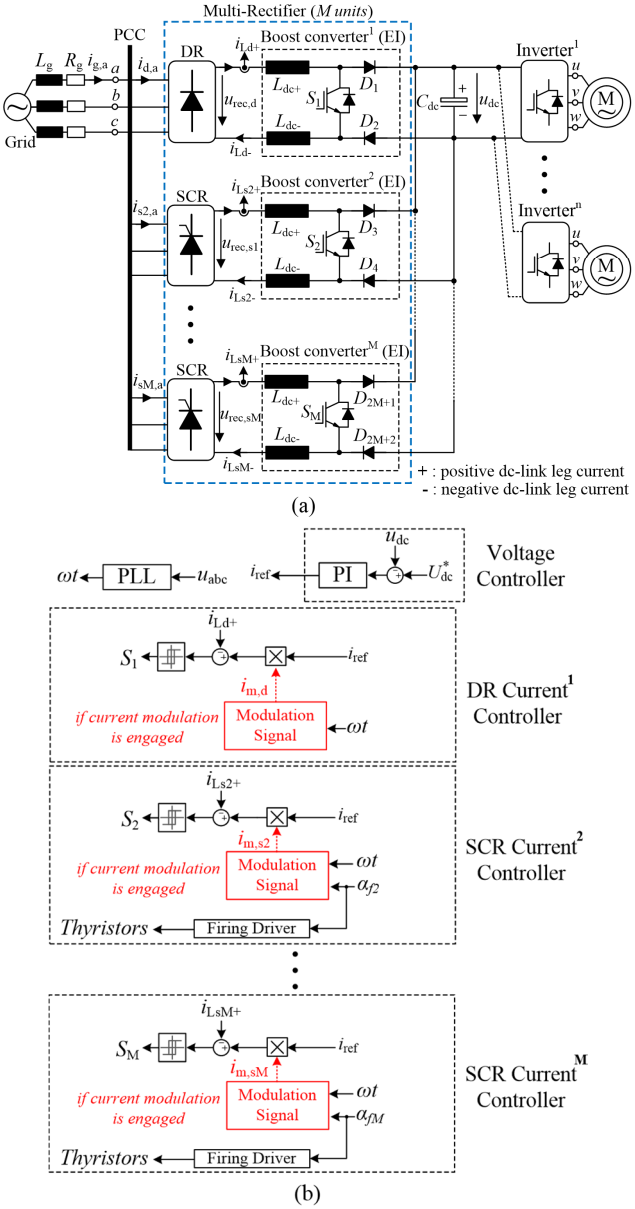

Fig. 2. The proposed multi-rectifier system with electronic phase-shifting: (a) circuit block diagram, (b) applied control strategy.

bulky phase-shifting transformer. As Fig. 3(a) shows, two line-commutated rectifiers (i.e., M = 2) have been used to perform a phase-shifting among the input currents. By applying different firing angles (α_f) to the Silicon Controlled Rectifier (SCR) the input currents will be phase-shifted and it is possible to reduce specific low order harmonics. Notably, since the firing angle of the first unit is always zero (α_{f1} = 0), a Diode Rectifier (DR) is selected (i.e., $i_{s1,abc} = i_{d,abc}$).

Here at the dc-side of each rectifier a dc-dc converter is installed. Controlling the dc-link current by incorporating a dc-dc converter enables to emulate the behavior of an ideal infinite inductor [5]-[8]. Fig. 3(a) shows a simplified representation of the proposed method, which the dc-dc converter will operate as a current source. Basically, by controlling the dc-link current at

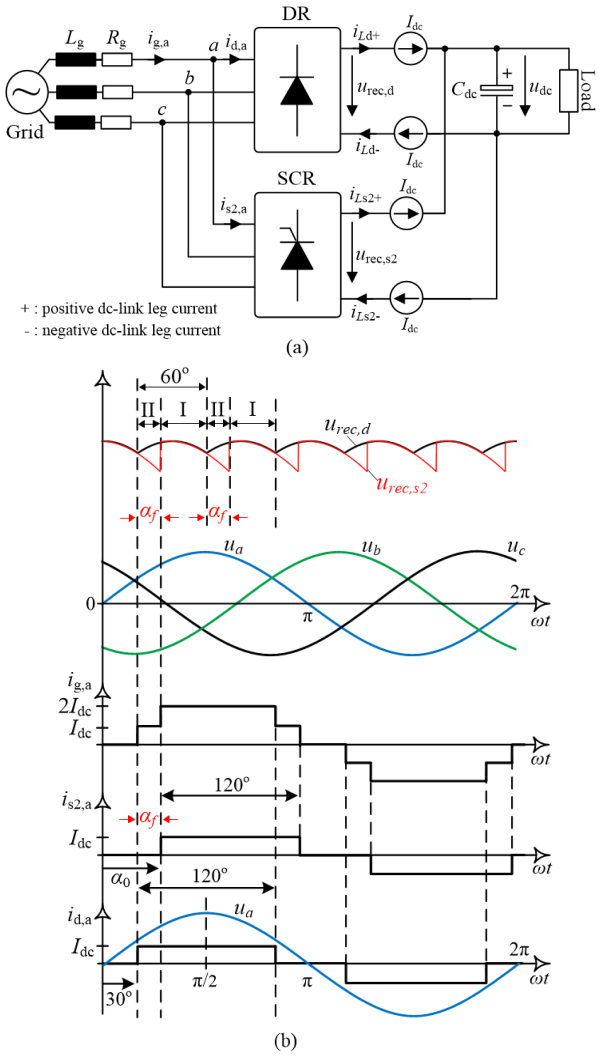

Fig. 3. Simplified representation of the proposed method: (a) schematic with ideal current sources at the dc-link, (b) stair-case waveform of the total input current ($i_{g,a}$) based on electronic phase-shifting (α_f) and flat current control of each rectifier.

a constant level (i.e., I_{dc}) the input current of each rectifier (i.e., $i_{d,a}$ and $i_{s2,a}$) will be a square-wave with 120 degrees conduction (Fig. 3(b)). As it can be seen from Fig. 3(b), applying a phase-shift (α_f) using the SCR will generate a multilevel total input current $i_{g,abc}$. In fact, by applying a suitable phase-shift to the SCR unit certain harmonic orders (h^{th}) can completely be eliminated (i.e., $\alpha_f = 180^o/h$). This has been validated as one of simulation cases in Section III.

To achieve the maximum harmonic reduction performance, the current drawn by each rectifier should be at the same level (i.e., $I_{Ld} = I_{Ls2} = I_{dc}$). Since the motors mostly operate at different partial loading conditions, having a common dc-bus and controlling the dc-link current can ensure such behavior. However, having a phase-shift of the controlled rectifier changes the rectified voltage ($u_{rec,sM}$) and makes the controlling of all rectifiers at same current level quite challenging due to presence of circulating currents. The proposed solution applies a passive method in order to minimize the circulating current.

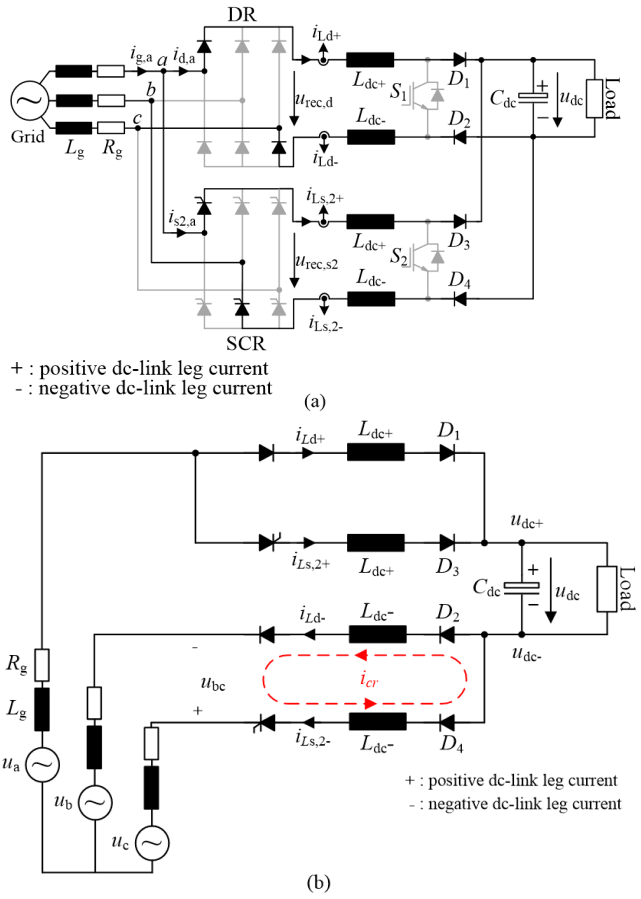

Fig. 4. Circuit diagram of the proposed rectifier system in operating Mode II: (a) circuit diagram when both switches S_1 and S_2 are in OFF-state, (b) simplified circuit diagram of the system showing the voltage difference across the negative dc-link legs and circulating current.

The passive method is based on utilizing extra inductors at negative dc-link leg of each rectifier (i.e., L_{dc-}). The operation modes are briefly explained for two parallel connected rectifier units as shown in Fig. 3(a). The operation modes can be generally analyzed as two modes, which is Mode I where both units have the same input voltage while in the second mode the rectifiers are connected to different input voltages.

Mode I ($\alpha_f \rightarrow 60^o$): In this time interval the same phase voltages (e.g., u_a & u_b) appear across both rectifiers. In this situation as it can be seen from Fig. 3(b) the rectified voltage across both rectifiers are equal (e.g., $u_{rec,d} = u_{rec,s1} = u_{ab}$). In this interval, there are four possible switching states based on S_1 and S_2. When at least one of the switches is in the ON-state, the rectifiers are separated from each other because of the blocking diodes D_1-D_4. Therefore, the circulating currents are prevented and each boost converter controls the dc-link currents. The current sharing in the last switching state can be an issue as both switches are in the OFF-state and the capacitor (C_{dc}) is connected to both rectifiers. However, since both rectifier units are connected to the same phase voltages, applying the proposed passive and active current control methods can keep the current at its reference value. Notably, the extra inductors (L_{dc-}) and the diodes in the negative dc-link

leg (D_2 and D_4). This means that any mismatch between the passive components should be prevented in order to ensure a better performance of the system. However, as it is shown in Section III, even under significant mismatch condition the proposed controller can maintain the dc-link current at its reference value to some extent.

Mode II ($0 \rightarrow \alpha_f$ /$60^o \rightarrow 60^o+\alpha_f$): In this mode the negative dc-link leg of the DR conducts through another phase other than the one in Mode I (see Fig. 4(a)). For instance, if during Mode I the DR was conducting through u_{ab} during the second mode it starts conducting through u_{ac}. This is due to the fact that following Fig. 3(b), the phase voltage u_c becomes lower than u_b. However, the SCR unit, since the next firing event has not occurred, will keep conducting in the Mode I line-to-line voltage (i.e., $u_{rec,s2} = u_{ab}$). Thus the negative dc-link legs of the rectifiers are connected to different phase voltages (e.g., u_b and u_c) while the positive legs are connected to the same voltage (e.g., u_a) as it is shown in Fig. 4(a). As mentioned, the current sharing can be an issue if both switches S_1 and S_2 are in the OFF-state. The simplified circuit diagram of this switching state is shown in Fig. 4(b). Thus, during this interval and switching state, the current through the negative dc-link legs are influenced by the magnitudes of the phase voltages u_b and u_c. On the other hand, the current through the positive dc-link legs are the same. The rate of current change of the dc-link current through the positive legs of the rectifiers are given as,

$$u_a - u_{dc+} = L_{dc+}\frac{di_{Ld+}}{dt} = L_{dc+}\frac{di_{Ls,2+}}{dt} \tag{1}$$

During this time interval, the input voltage across the SCR u_{ab}, is less than the input voltage across the DR u_{ac} (see Fig. 3(b)). The difference in the input voltages gives different di/dt values for the negative dc-link currents as,

$$\begin{aligned} &u_{ab} < u_{ac} \\ &L_{dc+}\frac{di_{Ls,2+}}{dt} + u_{dc} + L_{dc-}\frac{di_{Ls,2-}}{dt} < L_{dc+}\frac{di_{Ld+}}{dt} + u_{dc} + L_{dc-}\frac{di_{Ld-}}{dt} \end{aligned} \tag{2}$$

Following (1) and considering identical inductors,

$$\frac{di_{Ls,2-}}{dt} < \frac{di_{Ld-}}{dt} \tag{3}$$

This means that the rates of the current changes in the negative legs of the rectifiers are different while the di/dt values of the positive legs are the same. This issue has been elaborated more based on u_{bc} across the negative dc-link legs of the rectifiers as shown in Fig. 4(b). As the diodes D_2 and D_4 conduct, the circulating current i_{cr} is affected by u_{bc}. During this time interval and the switching time (i.e., S_1 and S_2 = 0), $u_{bc} > 0$, thus di_{cr}/dt is positive as,

$$u_{bc} = L_{dc-}\frac{di_{cr}}{dt} + L_{dc-}\frac{di_{cr}}{dt} = 2L_{dc-}\frac{di_{cr}}{dt} > 0 \tag{4}$$

Therefore, following (3) and (4) at the end of the switching state i_{Ld-} and $i_{Ls,2-}$ may have different magnitudes. The difference in the inductor currents depends on the dc-link inductor values. These currents will be adjusted during the next switching states when at least one of the switches S_1 and S_2 is turned on. This issue has been simulated and analyzed further in Section III.

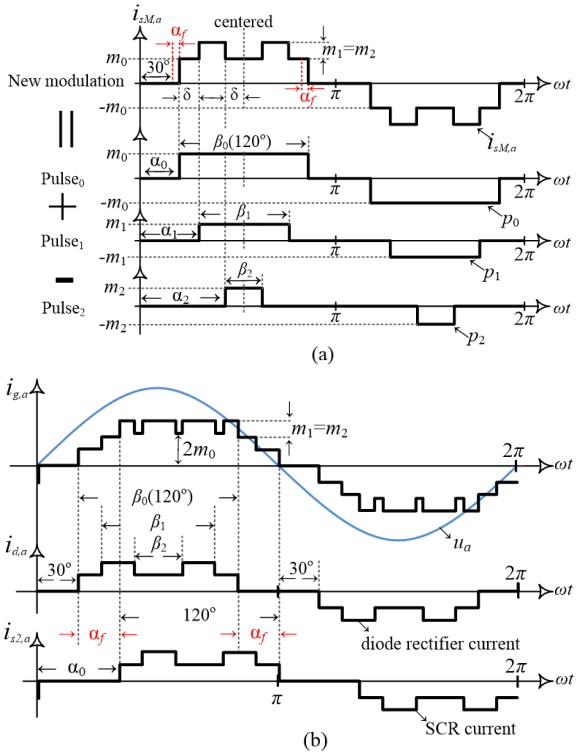

Fig. 5. Conceptual illustrations of the applied multi-pulse modulation scheme for harmonic elimination: (a) detailed analysis, (b) typical waveforms in generating multi-level current waveform at the grid-side current (i_g) [5]-[8].

B. Current Modulation Method

The current modulation method is based on the calculation of a pre-programmed switching pattern for the DC-link current to achieve the elimination of specific harmonics in the grid currents [5]. In this approach, a DC-link current modulation scheme is generated by adding or subtracting the phase-displaced current levels. Fig. 5(a) illustrates the principle of this multi-pulse modulation scheme ($i_{sM,a} = p_0 + p_1 - p_2$).

As it is shown in Fig. 5(a), the new modulation signal $i_{sM,a}$ consists of flat signals p_0, p_1, and p_2 with a conduction angle of β_0 (120°), β_1, and β_2, a phase-shift of α_0, α_1, and α_2 and a magnitude of m_0, m_1, and m_2, correspondingly. Hence, following the Fourier series, the harmonic components of the square-wave signals (i.e., p_0, p_1, and p_2) can be expressed as,

$$p_i^h(t) = a_i^h \cos(h\omega t) + b_i^h \sin(h\omega t) \tag{5}$$

in which, i = 0, 1, 2, and h = 1, 3, 5, 7, … is the harmonic order, ω the fundamental grid angular frequency, a_i^h and b_i^h are the Fourier coefficients that are given by,

$$\begin{cases} a_i^h = \dfrac{2m_i}{h\pi}\left[-\sin(h\alpha_i) + \sin(h\alpha_i + h\beta_i)\right] \\ b_i^h = \dfrac{2m_i}{h\pi}\left[\cos(h\alpha_i) - \cos(h\alpha_i + h\beta_i)\right] \end{cases} \tag{6}$$

Notably, in the case of having only flat current modulation (i.e., Fig. 3(b)) $m_1 = m_2 = 0$. Subsequently, according to the superposition principle and Fig. 5(a), the harmonic components of the modulation signal (i.e., i_{sM}) can be obtained as,

$$\begin{aligned} i^h_{sM,ph}(t) &= (a^h_0 + a^h_1 - a^h_2)\cos(h(\omega t - \theta_{ph})) + \dots \\ &\dots (b^h_0 + b^h_1 - b^h_2)\sin(h(\omega t - \theta_{ph})) \end{aligned} \quad (7)$$

in which $ph = a$, b, and c with $\theta_a = 0$, $\theta_b = -120$, and $\theta_c = 120$. As a result, the h-order harmonic magnitude ($I^h_{sM,ph}$) of the resultant DC-link modulation scheme can be expressed as,

$$I^h_{sM,ph} = \left[\left(a^h_0 + a^h_1 - a^h_2\right)^2 + \left(b^h_0 + b^h_1 - b^h_2\right)^2 \right]^{1/2} \quad (8)$$

Finally, the following condition should hold,

$$\begin{cases} \alpha_1 + \alpha_2 = 2\alpha_0 + 60^o \\ \alpha_0 < \alpha_1 < \alpha_2 < \alpha_0 + 60^o \end{cases} \quad (9)$$

As Fig. 5(b) shows, applying the above current modulation in conjunction with phase-shifting results in a multi-level current waveform at the grid side. In that case, the resultant total harmonics of the grid current ($i^h_{g,abc}(t)$) for parallel connected rectifier systems will become,

$$i^h_{g,abc}(t) = \sum_M i^h_{sM,abc}(t) \quad (10)$$

Hereafter, according to (6) and (8) it is possible to achieve harmonic cancellation by calculating the harmonic magnitude of the total input current and solving $I^h_g = 0 (h \neq 1)$ and $I^1_g = MI$ with MI being the desired Modulation Index.

In order to obtain more suitable solution to reduce the harmonics of interest, an optimization can be carried out. Using optimization allows applying the maximum allowable harmonic levels defined by the application or the grid code [14]. Moreover, the above multi-pulse current modulation can be extended by adding more current levels, which increase the flexibility of harmonic reduction approach [7].

III. Results

In this section the proposed method is validated through numerical simulations. Table I shows the list of the applied parameters in the system. As it can be seen from Table I, an RC snubber branch is considered for SCR units. In practice, to avoid SCR unit failure and to reduce the overvoltage to a reasonable limit, an RC snubber branch is connected across each thyristor. However, the presence of the snubber circuit causes current spikes in the SCR current at the point of commutation. In order to damp the current spikes, small AC-side inductors are placed in series prior to the SCR units (i.e., L_{scr}). Here, two different cases are considered. In the first case study, the performance of the proposed current control technique in balancing the dc-link currents is analyzed based on the extra added inductors (L_{dc-}). Secondly, the advantage of the proposed topology in improving the input current quality is addressed for different situations and number of the modular units (M).

Table I. Parameters of the Multi-Rectifier System

Symbol	Parameter	Value
u_{abc}	Grid phase voltage	230 Vrms
f_g	Grid frequency	50 Hz
L_g, R_g	Grid impedance	0.1 mH, 0.1Ω
L_{scr}	SCR AC-side filter	0.18 mH
C_{snub}, R_{snub}	SCR snubber	100nF, 100 Ω
$L_{dc+} = L_{dc-}$	DC link inductor	1 mH
C_{dc}	DC link capacitor	0.5 mF
U_{dc}	Output voltage	700 Vdc
HB	Hysteresis band	0.5 A
$P_{O,total}$	Total output power	10 kW

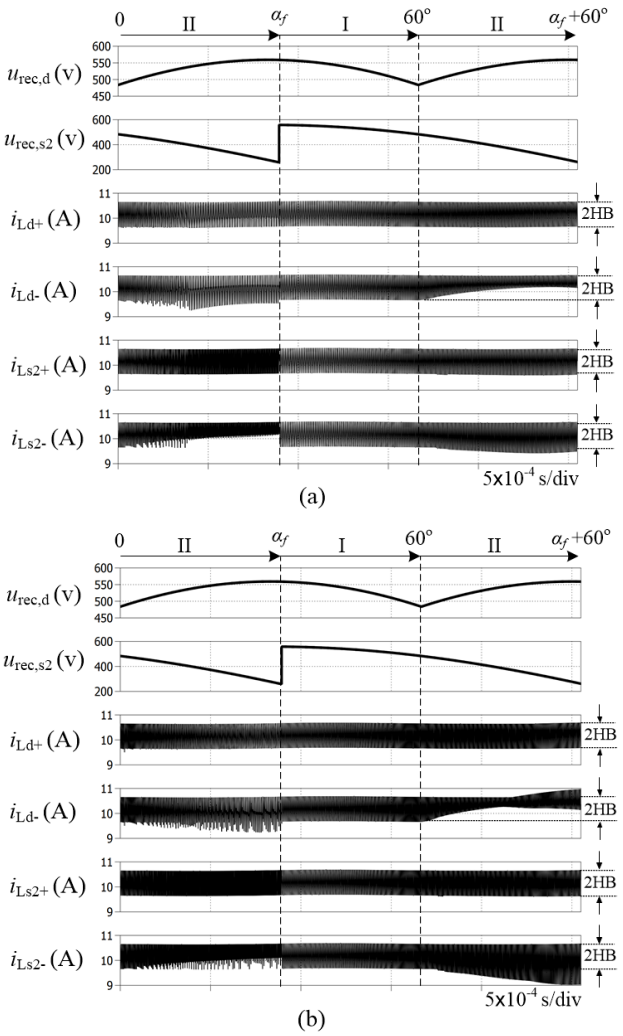

Fig. 6. The rectified voltages and dc-link currents waveforms for two parallel rectifiers: (a) under balanced condition when the positive and negative dc-link inductors are equal ($L_{dc+} = L_{dc-}$) and (b) when there is 50% mismatch between the positive and negative dc-link inductors ($L_{dc-} = 0.5L_{dc+}$).

Fig. 6 shows the rectified voltages and dc-link current waveforms at both positive and negative legs for two parallel rectifier units under balanced and unbalanced conditions. As it can be seen from Fig. 6(a), applying the proposed passive control method ($L_{dc+} = L_{dc-}$) when one current sensor is used at

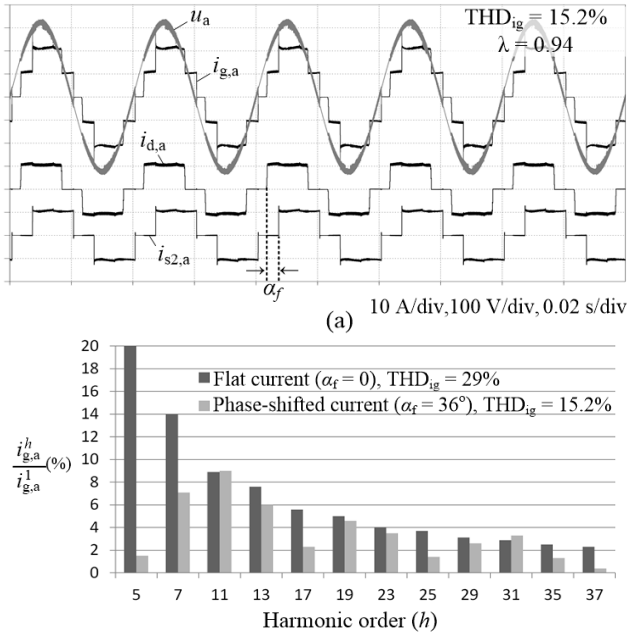

Fig. 7. Numerical simulations of two parallel rectifier units applying the phase-shifted current control technique with $\alpha_f = 36^o$ for 5th harmonic elimination at P_o = 100%: (a) input current waveforms, (b) comparison of harmonic distribution of total input current.

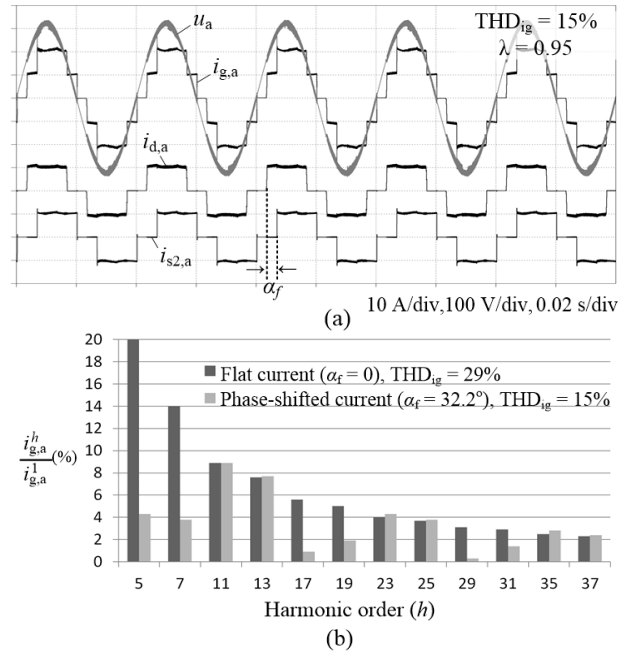

Fig. 8. Numerical simulations of two parallel rectifier units applying the phase-shifted current control technique with α_f = 32.2^o for minimum obtainable THD$_i$ at P_o = 100%: (a) input current waveforms, (b) comparison of harmonic distribution of total input current.

positive dc-link legs the currents are controlled within the Hysteresis Band (HB) and shared the currents equally between both converters. Conventionally when the firing angle

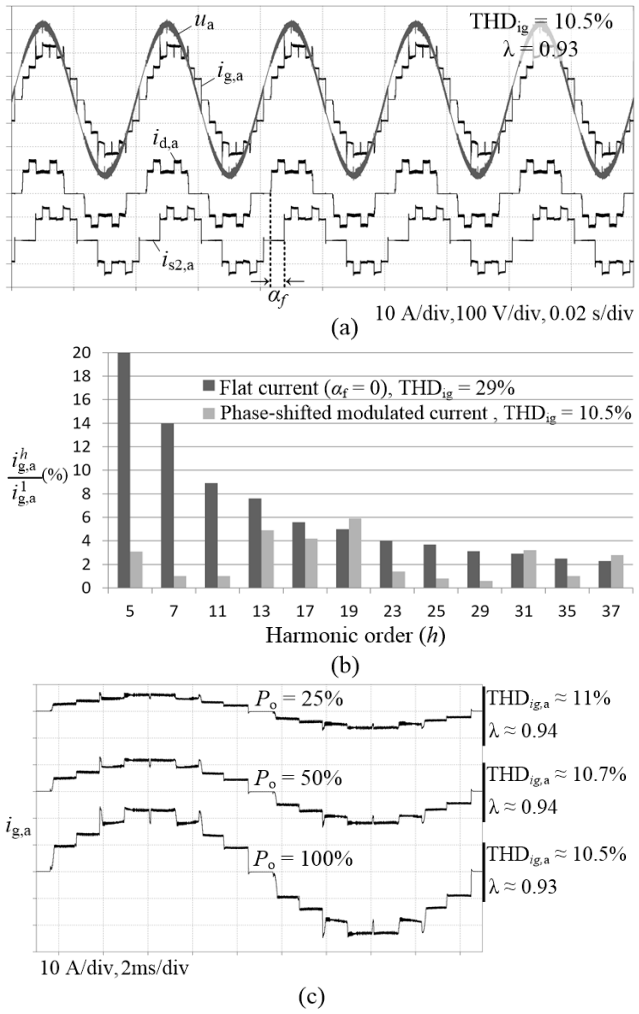

Fig. 9. Numerical simulation of two parallel rectifier units applying the phase-shifted ***modulated*** current control technique for minimum obtainable THD$_i$: (a) input current waveforms at P_o = 100% (10 kW), (b) comparison of harmonic distribution of total input current, (c) input current waveform at three different output power levels.

increases the boost converter draws more current in order to adjust the output voltage due to the reduction on the SCR rectified voltage [12]. The proposed configuration overcomes this problem which in return can enhance the harmonic reduction capability of the system. To further demonstrate the performance of the proposed technique the waveforms are illustrated in Fig. 6(b) for the case when there is a mismatch of 50% between the positive and negative dc-link inductors (i.e., $L_{dc-} = 0.5L_{dc+}$). As it can be seen, the negative dc-link currents of both rectifiers become unbalanced for the second operating mode. Although this is an extreme mismatch condition, it shows the importance of passive components parameters on the performance of the system as it is addressed in the previous section.

In order to show the performance of the proposed multi-pulse rectifier unit, the harmonic elimination capability of the system is evaluated under different configurations.

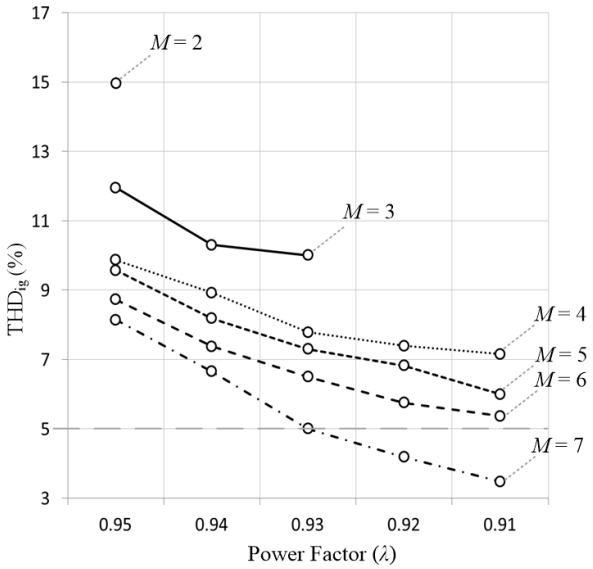

Fig. 10. Harmonic distortion of the total input current (THD_{ig}) optimized for different power factor values applying the phase-shifted current control scheme with respect to the number of connected modular rectifier units (M) at P_o = 100%.

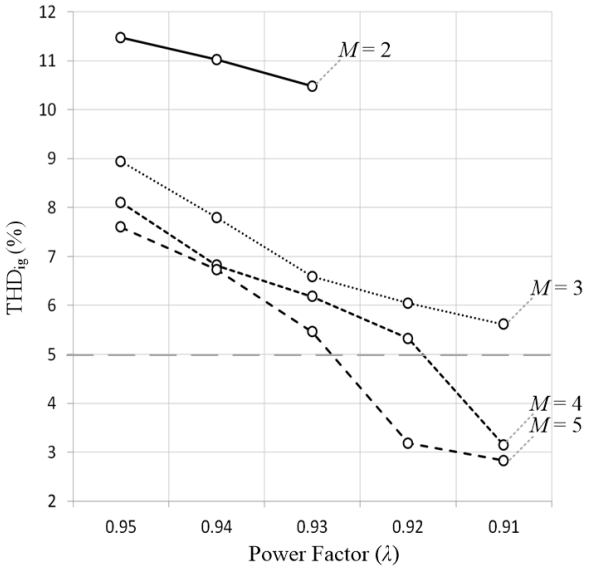

Fig. 12. Harmonic distortion of the total input current (THD_{ig}) optimized for different power factor values applying the phase-shifted ***modulated*** current control scheme with respect to number of the connected modular rectifier units (M) at P_o = 100%.

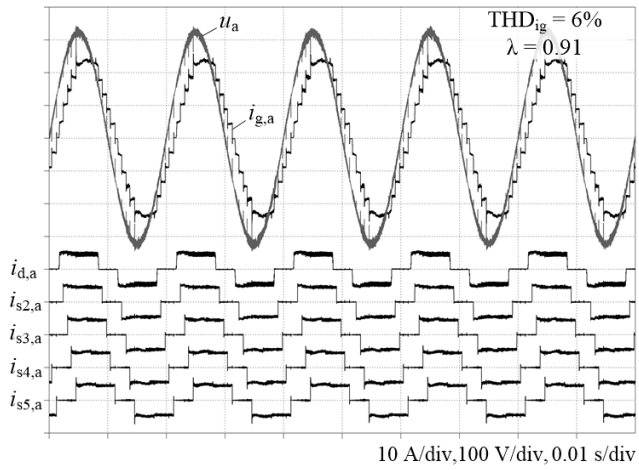

Fig. 11. Input current waveforms of five parallel rectifier units applying the phase-shifted current control technique for minimum obtainable THD_i at P_o = 100%.

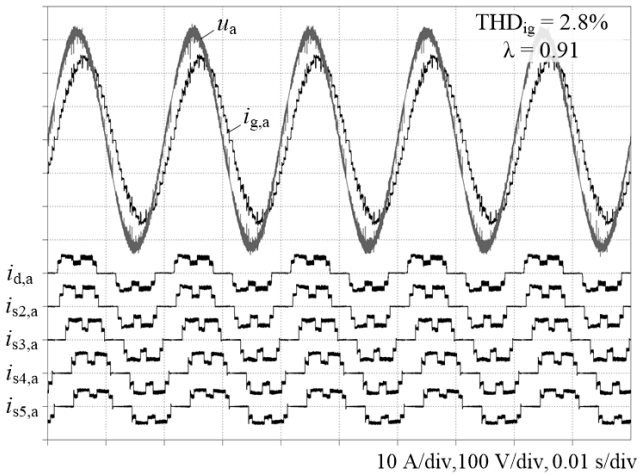

Fig. 13. Input current waveforms of five parallel rectifier units applying the phase-shifted ***modulated*** current control technique for minimum obtainable THD_i at P_o = 100%.

First, the harmonic performance is considered for two parallel units which only electronic phase-shifting is applied to the units following Fig. 3. The simulated results for the input currents of each rectifier units and the total input current at the PCC (i_g) are shown in Fig. 7 when a phase shift of $\alpha_f = 36^o$ is applied. Theoretically, applying this phase-shift should completely remove the 5th harmonic (i.e., 5x36° = 180°), however, the presence of non-ideal parameters especially the grid impedance slightly affects the applied phase-shift. As it can be seen from Fig. 7(b) applying 36° phase-shift almost eliminates the 5th harmonic order in the total input current (1.8%). This results in THD_i = 15.2% and power factor (λ) of 0.94. However, as it is depicted in Fig. 8, the minimum THD_i of 15% and power factor of λ = 0.95 can be obtained when α_f = 32.2° is considered.

Although using the phase-shifted current control can improve the input current quality, but in order to further reduce the THD_i, the current modulation scheme can be employed. Fig. 9 shows the obtained results for two parallel units when a pulse pattern along with the phase-shift is applied. Here, the control parameters are optimized for achieving the minimum possible THD_i. As it can be seen from Fig. 9(a) and (b) the THD_i is greatly improved from 15% in the flat dc-link current down to 10.5%. Notably, the parameters can be optimized based on different harmonic performance requirements [5]-[8]. In order to show the performance of the system under partial loading conditions, same phase-shifted current modulation is applied when the system is operating at three different output power levels (i.e., 100%, 50% and 25%). As it can be seen from Fig. 9(c), compared with Fig. 1, here the system

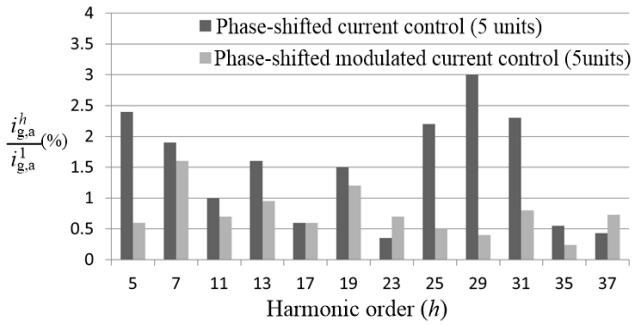

Fig. 14. Harmonic performance of the total input current in five modular rectifier units with phase-shifted current control (Fig. 11) and phase-shifted modulated current control (Fig. 13).

performance is kept almost the same both in terms of THD_i and power factor (λ).

The electronic phase-shifting technique has the advantage of being simple and cost-effective compared with the current modulation technique in which additional voltage sensors are required for the synchronization purpose. However, applying only phase shift cannot improve the input current quality as much as when it is combined with the modulation technique. But the performance of the system in improving the input current quality is highly dependent on the number of the connected rectifier units as well. Therefore, the performance of the phase-shifted flat current control can be comparable with the modulated current control technique if enough number of rectifiers is connected in parallel. In order to show this dependency, optimizations are conducted for having up to seven parallel rectifier units based on the minimum achievable THD_i and different power factors. The obtained results are illustrated in Fig. 10. As it can be seen with seven parallel units by only applying phase-shift current control the total input current THD_i can be reduced below 5% (i.e., $THD_{ig} = 3.5\%$ @ $\lambda = 0.91$) while the power factor is $0.91 < \lambda < 0.93$. As an example the waveforms of the rectifier unit input currents and the total input current for five parallel units, when the THD_i is 6% are depicted in Fig. 11.

In order to highlight the performance of the system with phase-shifted current modulation technique the optimization has been considered to obtain the minimum THD_i at different power factors for up to five parallel connected rectifier units (see Fig. 12). As it can be seen, the THD_i of the total input current can be reduced down to 2.8% when five rectifier units are utilized, while according to Fig. 13 with the same number of the units, when only phase-shifted current control is applied, the minimum achievable THD_i is 6%. This clearly differentiates the better performance of the system when the pulse pattern modulation strategy is used. Fig. 13 shows the rectifier units input currents and the total input current waveforms for the case of having a THD_i of 2.8%. Finally, the harmonic distribution of both cases is illustrated in Fig. 14 showing the better performance of the proposed current modulation technique.

IV. Conclusions

In this paper a new topology based on a multi-rectifier system is proposed for harmonic reduction. The proposed electronic phase-shifting technique (transformer-less) results in more compact and cost-effective multi-rectifier systems, which can be extended from low to high power for applications such as ASDs. Moreover, the active dc-link current control along with the current modulation further improves the total input current quality. Controlling the dc-link currents and sharing them among different number of drives leads to a novel advantage of having a common dc-bus voltage. This feature makes the rectifier units to draw equal amount of current from the grid, independent of the load profile, which maximizes the harmonic reduction capability of the system. The simulations and analysis verified the performance of the system which showed that applying the proposed multi-rectifier system with electronic phase-shifting (transformer-less) can significantly improve the input current quality compares with the traditional transformer-based rectifier systems.

References

[1] J.W. Gray and F. J. Haydock, "Industrial power quality considerations when installing adjustable speed drive systems," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 646-652, May/Jun 1996.

[2] D. Kumar and F. Zare, "Harmonic analysis of grid connected power electronic systems in low voltage distribution networks," *IEEE J. Emerg. Sel. Top. Power Electron*., vol. 4, no. 1, pp. 70-79, Jan. 2016.

[3] J. W. Kolar and T. Friedli, "The Essence of Three-Phase PFC Rectifier Systems - Part I," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 176-198, Jan. 2013.

[4] H. Y. Kanaan and K. Al-Haddad, "Three-Phase Current-Injection Rectifiers: Competitive Topologies for Power Factor Correction," *IEEE Trans. Ind. Electron. Magazine*, vol. 6, no. 3, pp. 24-40, Sept. 2012.

[5] P. Davari, Y. Yang, F. Zare, and F. Blaabjerg, "A multi-pulse pattern modulation scheme for harmonic mitigation in three-phase multi-motor drives," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 1, pp.174–185, Mar. 2016.

[6] Y. Yang, P. Davari, F. Zare, and F. Blaabjerg, "A dc-link modulation scheme with phase-shifted current control for harmonic cancellation in multi-drive applications," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1837-1840, Mar. 2016.

[7] P. Davari, F. Zare, and F. Blaabjerg, "Pulse pattern modulated strategy for harmonic current components reduction in three-phase AC-DC converters", *IEEE Trans. Ind. Appl.*, vol. pp, no. 99, pp. 1-11, in press, July/Aug 2016.

[8] P. Davari, Y. Yang, F. Zare, and F. Blaabjerg, "Predictive pulse pattern current modulation scheme for harmonic reduction in three-phase multi-drive systems", *IEEE Trans. Ind. Electron,* in press, 2016.

[9] S. Hansen, P. Nielsen, and F. Blaabjerg, "Harmonic cancellation by mixing nonlinear single-phase and three-phase loads," *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 152-159, Jan/Feb 2000.

[10] H. Akagi and K. Isozaki, "A hybrid active filter for a three-phase 12-pulse diode rectifier used as the front end of a medium-voltage motor drive," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 69-77, Jan. 2012.

[11] M. M. Swamy, "An electronically isolated 12-pulse autotransformer rectification scheme to improve input power factor and lower harmonic distortion in variable-frequency drives," *IEEE Trans. Ind. Appl.*, vol. 51, no. 5, pp. 3986–3994, Sept 2015.

[12] P. Davari, Y. Yang, F. Zare, and F. Blaabjerg, "Adjustable Speed Drives and Power Quality: Challenges and Cost-Effective Opportunities," in *Proc. of ECCE-Asia (IPEMC)*, 2016.

[13] H. Ertl and J. W. Kolar, "A constant output current three-phase diode bridge rectifier employing a novel "Electronic Smoothing Inductor", *IEEE Trans. Ind. Electron.*, vol. 52, pp. 454-461, 2005.

[14] Electromagnetic *compatibility (EMC) - Part 3-12: Limits - Limits for harmonic currents produced by equipment connected to public low-voltage systems with input current >16 A and ≤ 75 A per phase, IEC 61000-3-12, 2004.*