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Analysis of Three-Phase Rectifier Systems with Controlled DC-Link Current Under Unbalanced Grids

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***Abstract*—Voltage unbalance is the most common disturbance in distribution networks, which gives undesirable effects on many grid connected power electronics systems including Adjustable Speed Drive (ASD). Severe voltage unbalance can force conventional three-phase diode rectifiers into almost single-phase operation, which degrades the grid power quality and also imposes a significant negative impact on the ASD system. This major power quality issue affecting the conventional rectifiers can be attenuated by controlling the DC-link current based on an Electronic Inductor (EI) technique. The purpose of this paper is to analyze and compare the performance of an EI with a conventional three-phase rectifier under unbalanced grid conditions. Experimental and simulation results validate the proposed mathematical modelling.**

Keywords—power quality; harmonics; unbalanced grid; adjustable speed drive (ASD); conventional drive (CD); electronic inductor (EI)

I. INTRODUCTION

The advancement of power electronic devices and their decreasing price due to market demand have increased the use of Adjustable Speed Drive (ASD) systems as an effective energy saving solution in various industrial, commercial and residential applications [1]. Low cost diode rectifiers and Silicon Controlled Rectifier (SCR) are still very popular front-end topologies in ASD systems. Conventional In the Drive (CD) systems, the diode rectifier or SCR (Fig. 1(a)) can achieve high efficiency but may increase harmonics emission due to their non-linear characteristics. The current harmonics may cause low power quality and resonances at the grid side, hence challenge the stability in distribution networks. Therefore, a number of harmonic mitigation techniques have been developed such as passive filters [2], [3], multi-pulse transformer based rectifiers [4], [5] and active harmonic filtering techniques [6]-[8]. One of the harmonic mitigation techniques is based on a DC-link current control using an Electronic Inductor (EI) as it is shown in Fig. 1(b) [8]-[10]. EI is a simple technique, which can reduce the Total Harmonic Distortion (THD) and the power factor (λ) independent of the load profile. The performance of this method has been thoroughly analyzed as a single unit and multi-unit system under balanced grid conditions [10]-[12].

However, today distribution networks face a variety of different power quality issues such as voltage unbalance, background harmonic distortion, voltage sag, swell and line frequency variation and so on. Recent power quality surveys show that voltage unbalance is one of major problems in many

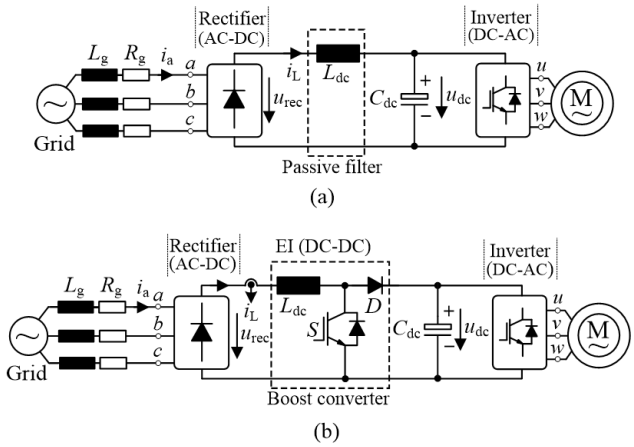


Fig. 1. ASD system architecture: (a) Conventional Drive (CD) with passive filtering at the DC-link, (b) EI technique.

distribution networks [13], [14]. Some of the main issues affecting voltage unbalance in a distribution network are [15]:

- Unequal distribution of single-phase load on three phase power system
- Asymmetrical feeders and transformer winding impedances
- Asymmetrical power generation of grid connected single phase distributed generations such as roof-top solar inverters

During voltage unbalance events, three-phase diode rectifiers are forced to enter in single-phase operation mode which can generate low-order harmonic components (100Hz, 300Hz etc. at 50Hz mains) in DC-link voltage. These low-order voltage harmonics significantly raise the AC-flux densities of DC-choke's core material, which leads to additional core losses and possibly saturates the choke [16]. The DC-link capacitors used in ASD are commonly electrolytic capacitors. These capacitors have rather high Equivalent Series Resistance (ESR), which is function of temperature and frequency. A high ripple current under unbalance conditions can result in high operating temperature and rise in ESR value. Also it is important to note that the capacitor's ESR increases significantly at low frequencies, therefore the capacitors' losses are extremely high at low frequency components [17]. These low frequency harmonic components in DC-link voltage can also distort the PWM output voltage of inverter and cause additional low frequency harmonic current in the motor load. These low

frequency harmonics in motor input current create undesired ripple in motor torque at same frequency as seen in DC-link voltage, which is commonly known as pulsating torque [18].

As unbalanced in distribution network can give serious implications on drives' performance and its life time. Therefore, it is very important to analyze the performance of any new proposed topology under unbalanced grid conditions. Thus, in this paper the performances of the EI analyzed under various unbalanced grid conditions and then compare with CD topology.

The rest of this paper is organized as follows. In Section II, the proposed EI topology is analyzed under unbalanced grid based on the developed analytical method. In Section III, the performance of proposed EI is compared with CD under unbalanced grid conditions is performed. Simulation and experiments are carried out in order to verify the analysis. The obtained results will demonstrate the effectiveness of EI-drive and validates the proposed analytical approach. Finally, conclusion is drawn in Section IV.

II. Electronic Inductor under Unbalanced Grid Conditions

A simple and a cost-effective solution to maintain the performance of a three-phase power electronic system in terms of THD_i and power factor (λ) (where, λ = distortion factor × displacement factor) is to use EI technique (e.g., Fig. 1(b)). Fig. 2(a) shows that the behavior of an EI at the DC-link side of the rectifier can be modeled as a current source which draws a constant current equal to I_L. In this situation, the input current at the grid side (i.e., i_{abc}) will be a square-wave with 120º conduction, and the resultant of $THD_i \approx 30\%$ and $\lambda \approx 0.95$ (Fig. 2(b)).

In order to understand the impact of the grid voltage on EI performance, the circuit diagram depicted in Fig. 2(a) is considered. Due to the nature of a three-phase system (i.e., 120º phase shift between the phases) under balanced grid condition (i.e., symmetrical input waveforms) the most prominent harmonics are the fifth, the seventh, the eleventh, and the thirteenth orders [11]. When the grid voltage is unbalanced, the conduction period of each diode in a three-phase rectifier depends on a type and a level of the unbalanced voltage. Under balanced conditions, the square wave switching function of the three-phase diode rectifier is symmetrical and generates the following current harmonics:

$$I_{ph,h} = \frac{2\sqrt{3}I_L}{h\pi} \tag{1}$$

where $I_{ph,n}$ is the line current magnitude, $ph = a$, b, or c and h = 1, 5, 7, 11, 13, … being the harmonic order.

When the line voltages are not symmetrical, then they affect the conduction times of the diodes; thus the harmonic orders of the line currents are a function of the unbalanced voltage. The type of supply voltage unbalance can be in amplitude or phase angle in distribution grids. In this section, in order to analyze the performance of EI-drive, mathematical models are developed for both types of the voltage unbalances.

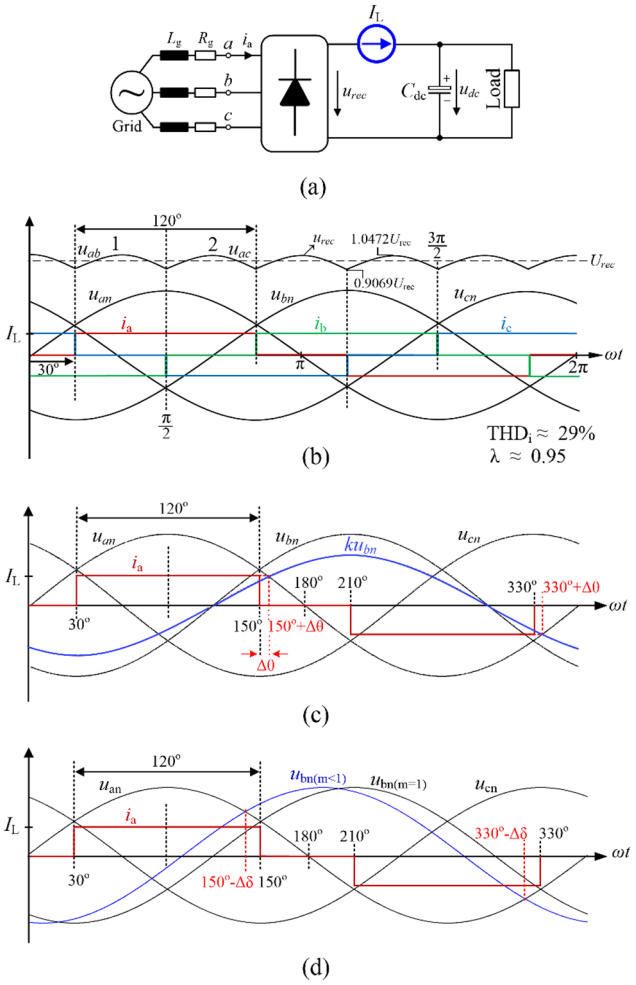


Fig. 2. Circuit diagram of a three-phase diode rectifier with a controlled DC-link current, (a) system schematic, (b) ideal three-phase input current, (c) change in conduction time during voltage amplitude unbalance, and (d) change in conduction time during voltage phase angle unbalance.

A. Voltage amplitude unbalance

In order to develop a mathematical modelling of the current harmonics in terms of voltage amplitude unbalance, it is assumed that one of the phases (e.g., u_b) has different magnitude compared to the other phases, while their phase angle values have 120º difference as shown in Fig. 2(c). Phases "*a*" and "*b*" are based on the symmetrical voltage waveforms and the conduction angles of the diodes are calculated when magnitudes of phases "*a*" and "*b*" are the same. This has been defined as:

$$\begin{cases} u_a = U_m \sin(\omega t) \\ u_b = kU_m \sin(\omega t - 120^o) \\ u_c = U_m \sin(\omega t + 120^o) \end{cases} \tag{2}$$

where k is a factor between 0 to 1. The conduction angle of the line current in phase "*a*" is defined when the amplitude of the phase voltages "*a*" and "*b*" are equal, which are given by the following equations:

$$\overbrace{U_m \sin(\omega t)}^{u_a(t)} = \overbrace{kU_m \sin(\omega t - 120^o)}^{u_b(t)} \quad (3)$$

$$\sin(\omega t) = k\sin(\omega t)\cos(120^o) - k\sin(120^o)\cos(\omega t) \quad (4)$$

$$\sin(\omega t)\left[1+\frac{k}{2}\right] = -k\frac{\sqrt{3}}{2}\cos(\omega t) \quad (5)$$

$$\tan(\omega t) = \frac{-k\sqrt{3}/2}{1+k/2} \quad (6)$$

If $\omega t = \phi$ then equation (6) can be written as:

$$\tan(\phi) = \frac{-k\sqrt{3}/2}{1+k/2} \quad (7)$$

Following Fig. 2(c), the change in diodes' conduction angles ($\Delta\theta$) can be calculated as:

$$|\Delta\theta| = |\phi + 30^o| \quad \text{with} \quad \phi = tan^{-1}\left(-0.5\sqrt{3}k \Big/ \left(1+\frac{k}{2}\right)\right) \quad (8)$$

As the phase voltages of "*a*" and "*b*" are based on the symmetrical voltage waveforms, the conduction angle of the line current starts at π/6. Based on the Fourier series, the harmonic currents can be represented as:

- For phase "*b*" which has a lower amplitude:

$$i_b^h = \frac{2I_L}{\pi}\int_{\frac{\pi}{6}+\Delta\theta}^{\frac{5\pi}{6}-\Delta\theta} \sin(h\omega t)\, d(\omega t) \quad (9)$$

$$i_b^h = \frac{2I_L}{h\pi}\left[\cos\left(h\left(\frac{\pi}{6}+\Delta\theta\right)\right) - \cos\left(h\left(\frac{5\pi}{6}-\Delta\theta\right)\right)\right] \quad (10)$$

- For phase "*a*" and "*c*" which have same amplitude:

$$i_{a,c}^h = \overbrace{\frac{2}{\pi}\int_0^{\pi} I_L \cos(h\omega t)d\omega t}^{a_h} + \overbrace{\frac{2}{\pi}\int_0^{\pi} I_L \sin(h\omega t)d\omega t}^{b_h} \quad (11)$$

where the Fourier coefficients a_h and b_h are defined as:

$$\begin{cases} a_h = \dfrac{2I_L}{h\pi}\left[\sin\left(h\left(\dfrac{5\pi}{6}+\Delta\theta\right)\right) - \sin\left(h\left(\dfrac{\pi}{6}\right)\right)\right] \\ b_h = \dfrac{2I_L}{h\pi}\left[-\cos\left(h\left(\dfrac{5\pi}{6}+\Delta\theta\right)\right) + \cos\left(h\left(\dfrac{\pi}{6}\right)\right)\right] \end{cases} \quad (12)$$

As already mentioned, the presence of voltage unbalance on a three-phase system lead to generation of third harmonic current and its multiples:

$$\begin{cases} \left|i_b^3\right| = \dfrac{4I_L}{3\pi}\sin(3\Delta\theta) \\ \left|i_{a,c}^3\right| = \dfrac{2I_L}{3\pi}\sqrt{2-2\cos(3\Delta\theta)} \end{cases} \quad (13)$$

Equation (8) and (13) show the relationship between the levels of voltage amplitude unbalance and generated third harmonics.

B. Voltage phase angle unbalance

In order to analyze the current harmonics performance under voltage phase angle unbalance, it is assumed that one of the phases (e.g., u_b) has phase angle difference other than 120° as shown in Fig. 2(d). Phases "*a*" and "*b*" are based on the symmetrical voltage waveforms and the conduction angles of the diodes are calculated when magnitudes of phases "*a*" and "*b*" are the same and having 120° phase angle difference. This has been defined as:

$$\begin{cases} u_a = U_m \sin(\omega t) \\ u_b = U_m \sin(\omega t - m.120^o) \\ u_c = U_m \sin(\omega t + 120^o) \end{cases} \quad (14)$$

where *m* is a factor between 0 to 1. The conduction angle of the line current in phase "*a*" is defined when the amplitude of phase voltages "*a*" and "*b*" are equal and having 120° phase angle difference, which are given by the following equations:

$$\overbrace{U_m \sin(\omega t)}^{u_a(t)} = \overbrace{U_m \sin(\omega t - m.120^o)}^{u_b(t)} \quad (15)$$

$$\sin(\omega t) = \sin(\omega t - m.120^o) \quad (16)$$

Using trigonometric identities, (16) can be re-arranged as:

$$2\sin(m.60^o)\cos(\omega t - m.60^o) = 0 \quad (17)$$

where the term $2sin(m.60^o)$ is a constant value and cannot be equal to zero in any condition. Therefore, considering $\omega t = \alpha$ equation (17) can be simplified as:

$$\cos(\alpha - m.60^o) = 0 \quad (18)$$

Thereby, the solution for (18) can be obtained as below:

$$\alpha = m.60^o + 90^o \quad (19)$$

$$\begin{cases} if \quad m = 1 \Rightarrow \alpha = 150^o \\ if \quad 0 \le m \le 1 \Rightarrow \alpha = 150^o - \Delta\delta \end{cases} \quad (20)$$

Following Fig. 2(d), the change in diodes conduction angle ($\Delta\delta$) can be calculated as:

$$|\Delta\delta| = |60^o.(1-m)| \quad (21)$$

Notably, the conduction angles under unbalance voltage phase angle condition are different than the previous case where the voltage amplitude was affected. This can be clearly understood from the victim phase (e.g., phase *b*) which its conduction angle remains 120°. Table I compares the conduction angles under both unbalance situations. Therefore, based on the Fourier series, the harmonic currents under unbalance phase angle can be represented as:

TABLE I. COMPARISON OF DIODE CONDUCTION ANGLES AT EACH PHASE UNDER VOLTAGE UNBALANCE IN PHASE B OF EI-DRIVE

	Amplitude unbalance $U_b = kU_m\angle$-120°	Phase angle unbalance $U_b = U_m\angle -m120°$
Phase	Conduction angle	Conduction angle
a	$120° + \Delta\theta$	$120° - \Delta\delta$
b	$120° - 2\Delta\theta$	120°
c	$120° + \Delta\theta$	$120° + \Delta\delta$

- For phase "*b*" which has deviation in phase angle:

$$i_b^h = a_h + b_h$$

$$\begin{cases} a_h = \dfrac{2I_L}{h\pi}\left[\sin\left(h\left(\dfrac{5\pi}{6}-\Delta\delta\right)\right)-\sin\left(h\left(\dfrac{\pi}{6}-\Delta\delta\right)\right)\right] \\ b_h = -\dfrac{2I_L}{h\pi}\left[\cos\left(h\left(\dfrac{5\pi}{6}-\Delta\delta\right)\right)-\cos\left(h\left(\dfrac{\pi}{6}-\Delta\delta\right)\right)\right] \end{cases} \quad (22)$$

- For phase "*a*" and "*c*" which have no deviation in their phase angle:

$$i_a^h = a_h + b_h$$

$$\begin{cases} a_h = \dfrac{2I_L}{h\pi}\left[\sin\left(h\left(\dfrac{5\pi}{6}-\Delta\delta\right)\right)-\sin\left(h\left(\dfrac{\pi}{6}\right)\right)\right] \\ b_h = -\dfrac{2I_L}{h\pi}\left[\cos\left(h\left(\dfrac{5\pi}{6}-\Delta\delta\right)\right)-\cos\left(h\left(\dfrac{\pi}{6}\right)\right)\right] \end{cases} \quad (23)$$

$$i_c^h = a_h + b_h$$

$$\begin{cases} a_h = \dfrac{2I_L}{h\pi}\left[\sin\left(h\left(\dfrac{5\pi}{6}\right)\right)-\sin\left(h\left(\dfrac{\pi}{6}-\Delta\delta\right)\right)\right] \\ b_h = -\dfrac{2I_L}{h\pi}\left[\cos\left(h\left(\dfrac{5\pi}{6}\right)\right)-\cos\left(h\left(\dfrac{\pi}{6}-\Delta\delta\right)\right)\right] \end{cases} \quad (24)$$

TABLE II. PARAMETERS OF THE SYSTEM (FIG. 1)

	Grid phase voltage and frequency	DC-link Inductor	DC-link capacitor	DC-link output voltage
	U_{abc}, f_g	L_{dc}	C_{dc}	U_{dc}
CD	230 V_{rms}, 50 Hz	2.5 mH	680 µF	≈ 535 V
EI	230 V_{rms}, 50 Hz	2 mH	470 µF	700 V

TABLE III. VOLTAGE UNBALANCE CASES

U_a	U_b	U_c	$U_{unbalanced}$
balanced			
230∠0°	230∠-120°	230∠120°	0
amplitude unbalance (phase a)			
209.7∠0°	230∠-120°	230∠120°	3%
196.7∠0°	230∠-120°	230∠120°	5%
165.5∠0°	230∠-120°	230∠120°	10%
phase angle unbalance (phase c)			
230∠0°	230∠-120°	230∠125.2°	3%
230∠0°	230∠-120°	230∠128.6°	5%
230∠0°	230∠-120°	230∠102.9°	10%

Thereby, following (22) - (24), the third harmonic order can be calculated as:

$$\begin{cases} \left|i_b^3\right| = 0 \\ \left|i_{a,c}^3\right| = \dfrac{2I_L}{3\pi}\sqrt{2-2\cos(3\Delta\delta)} \end{cases} \quad (25)$$

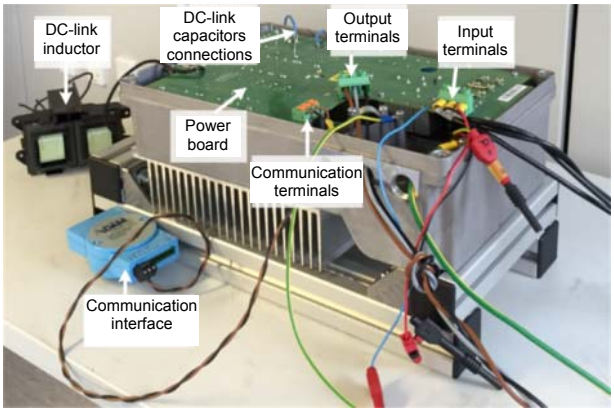
III. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, the performance of the CD and the EI-drive under unbalance supply grid are analyzed through a number of simulations and experiments at three output power levels (1 kW, 3 kW and 5 kW) under unbalanced supply grid conditions (3%, 5% and 10%) using the parameters given in Table II and Table III. Experimental tests have been carried out for a 7.5 kW drive system with an Induction Motor (IM) as a load for both CD and EI systems. Fig. 3 shows the hardware prototypes.

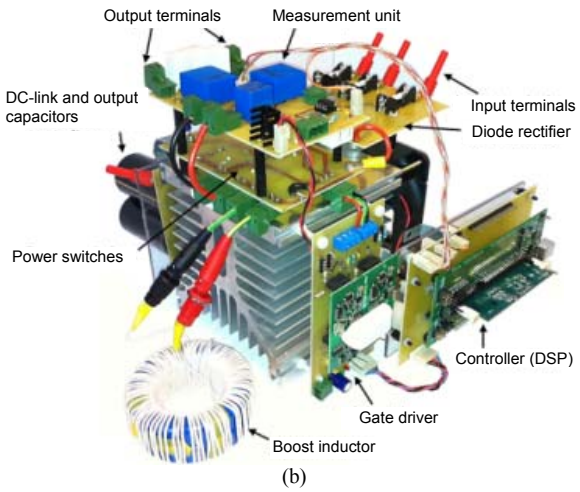
The amount of voltage unbalance is calculated by using the IEC61000-2-2 for three-phase system expressed as:

$$U_{unbalanced}(\%) = \sqrt{\frac{6\times\left(U_{ab}^2+U_{bc}^2+U_{ca}^2\right)}{\left(U_{ab}+U_{bc}+U_{ca}\right)^2}-2} \quad (26)$$

where U_{ab}, U_{bc} and U_{ca} are line-line RMS voltages in three-phase system. Table III shows the considered voltage unbalanced conditions.



(a)



(b)

Fig. 3. Photograph of implemented, (a) conventional three-phase diode rectifier based motor drive, (b) three-phase EI-drive.

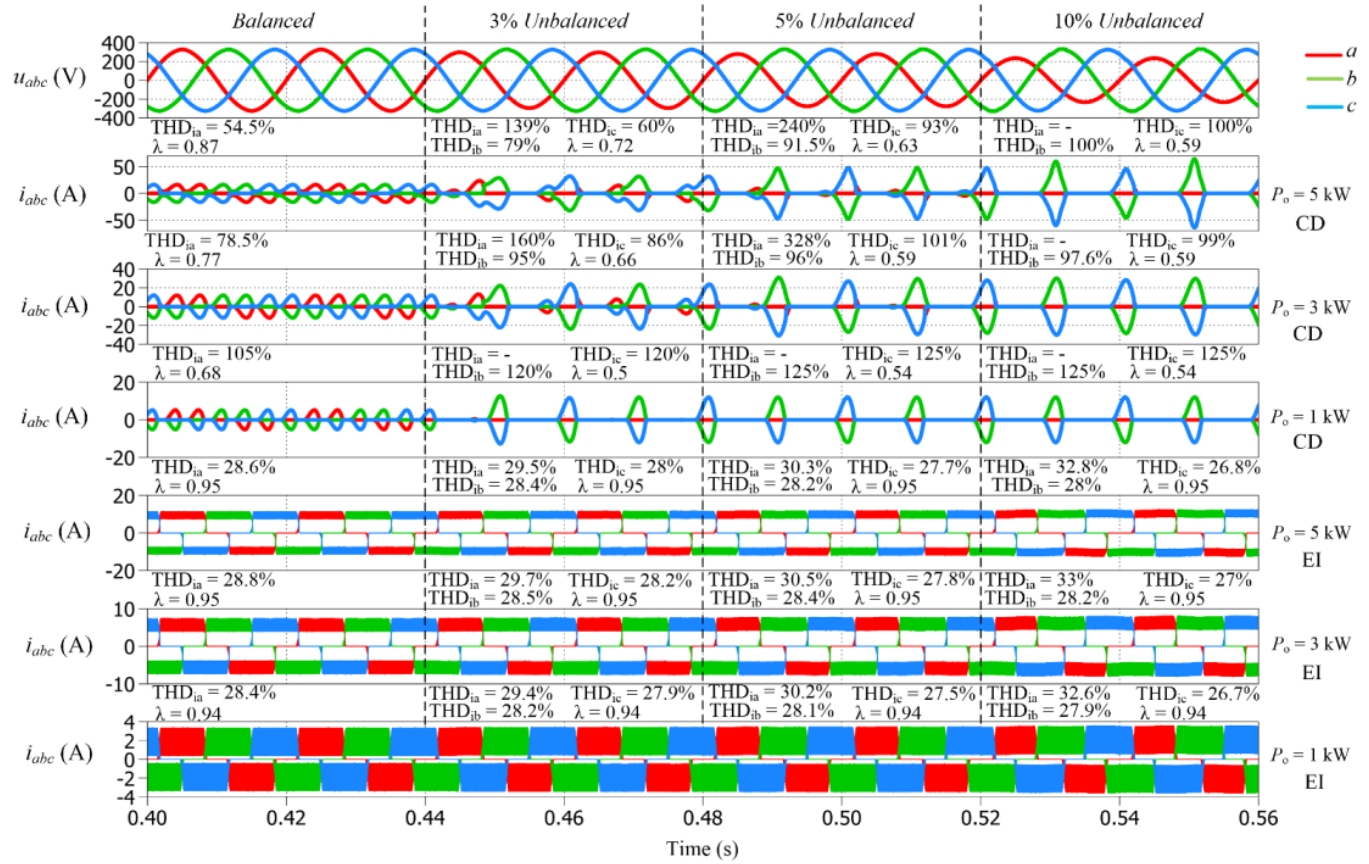


Fig. 4. Simulation waveform of three-phase supply voltage and current for Conventional Drive (CD) and EI at different loading and supply voltage **amplitude** unbalance conditions (Phase *a*).

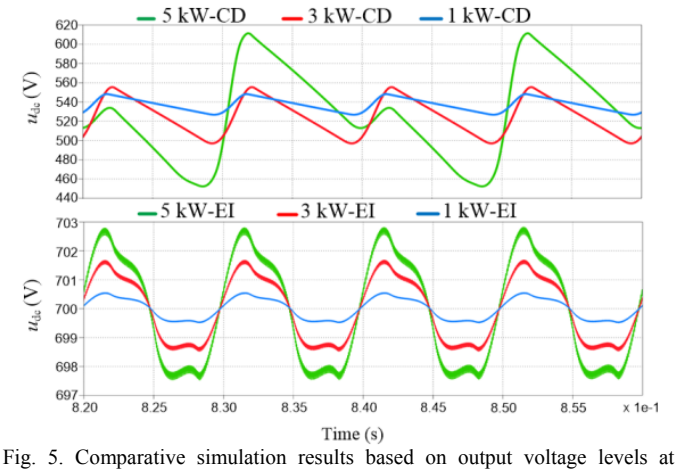


Fig. 5. Comparative simulation results based on output voltage levels at different output power levels under 10% amplitude unbalanced grid.

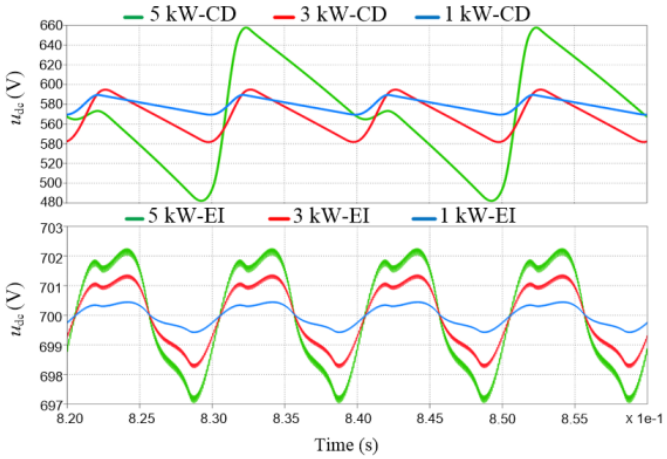


Fig. 6. Comparative simulation results based on output voltage levels at different output power levels under 10% phase angle unbalanced grid.

A. Simulation Results

Fig. 4 shows the obtained simulation results for both EI and CD systems with amplitude unbalance following Fig. 1. As it can be seen, under the balanced condition the input currents of the CD system are in Continuous Conduction Mode (CCM) only when the output power is 5 kW. This is in contrary to the EI system where the input currents are kept in CCM regardless of the output power level. Notably, the EI system operates in CCM even under significant unbalanced condition (i.e., 10 %), where performance of the conventional system is degraded (i.e., THD_i and λ) as it operates in the single-phase mode.

In order to show the effect of unbalance phase angle, aforementioned simulation cases are repeated following Table II and Table III parameters. Notably, the unbalanced condition also affects the DC-link voltage ripple. Figs. 5 and 6 illustrate the DC-link voltage at different output power levels under 10% voltage amplitude and phase angle unbalance. As it can be seen, the voltage ripple in the CD system can be as high as 160 V and

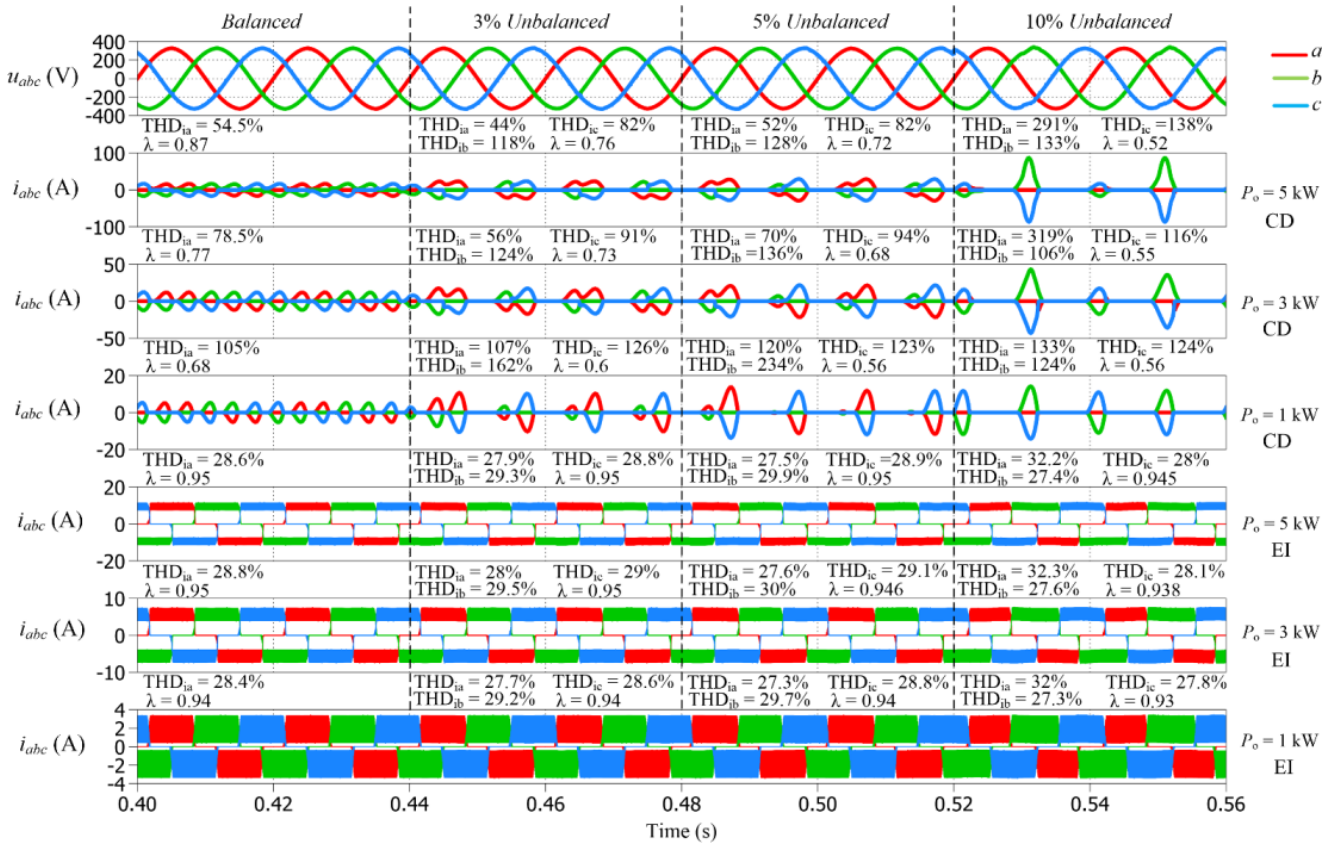


Fig. 7. Simulation waveform of three-phase supply voltage and current for Conventional Drive (CD) and EI at different loading and supply voltage **phase angle** unbalance conditions (Phase *c*).

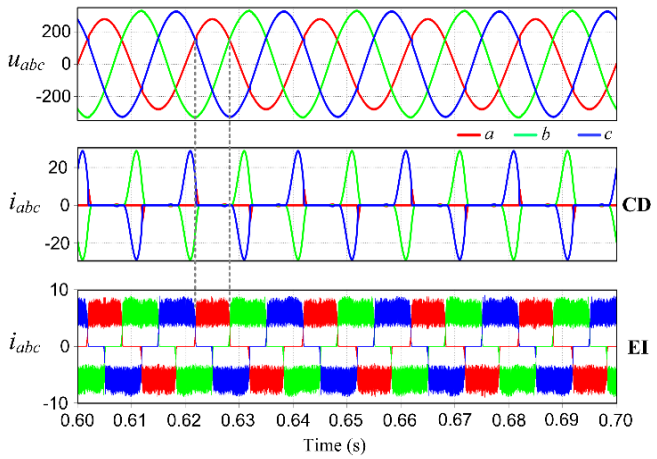


Fig. 8. Experimental waveform of three-phase supply voltage and line current for CD and EI at 3kW output power with 5% voltage **amplitude** unbalance conditions (Phase *a*).

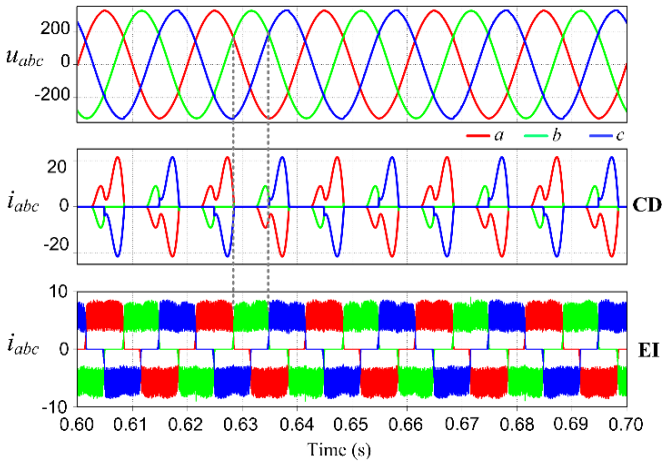


Fig. 9. Experimental waveform of three-phase supply voltage and current for Conventional Drive (CD) and EI at 3kW output power with 5% voltage **phase angle** unbalance conditions (Phase *c*).

180 V under unbalance voltage amplitude and phase angle respectively, while in the case of the EI-drive the maximum oscillation in both cases is 5 V. This is an important information for design engineers in order to decide the protection level. Simulation results clearly verify consistent performance of EI-drive irrespective to the type of unbalance (amplitude or phase angle) and level of unbalanced.

Finally, Fig. 7 illustrates the obtained simulation results under voltage phase angle unbalance condition. Here, it is important to note that in CD with amplitude unbalance, current in victim phase is significantly reduced (phase "*a*" in previous case) due to reduction in diode conduction angle in that phase. However, this phenomenon is different in case of phase angle unbalance, for instance in this study phase angle deviation applied at phase "*c*", but current in phase "*c*" and "*a*" increased but reduced in phase "*b*". This is due to increase in diode conduction angle in phase "*c*", which is opposite in case of amplitude unbalance.

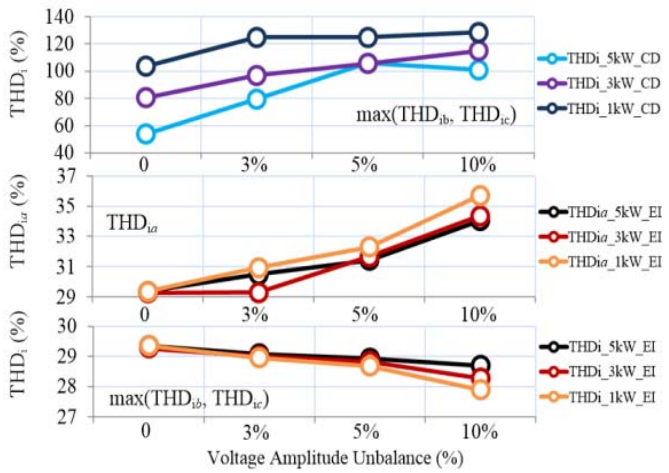


Fig. 10. Measured THD_i for Conventional Drive (CD) and Electronic Inductor (EI) at different output power levels under voltage **amplitude** unbalanced condition.

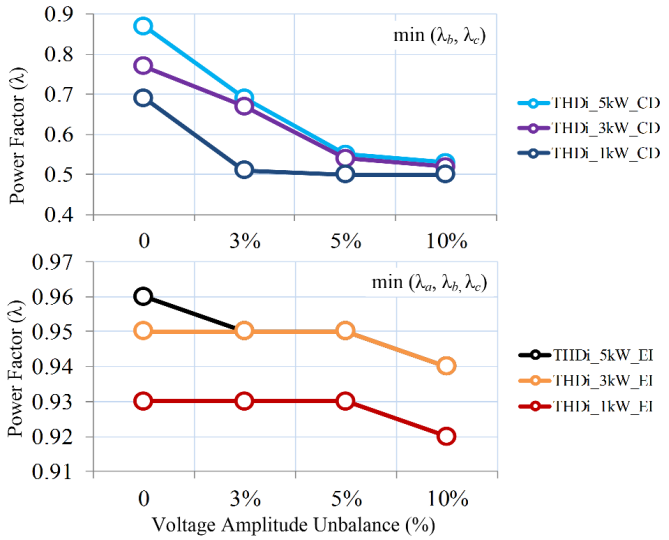


Fig. 11. Measured power factor (λ) for Conventional Drive (CD) and Electronic Inductor (EI) at different output power levels under voltage **amplitude** unbalanced condition.

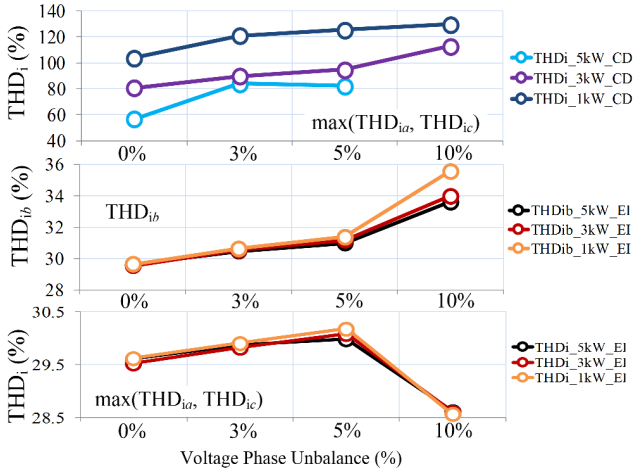


Fig. 12. Measured THD_i for Conventional Drive (CD) and Electronic Inductor (EI) at different output power levels under voltage **phase angle** unbalanced condition.

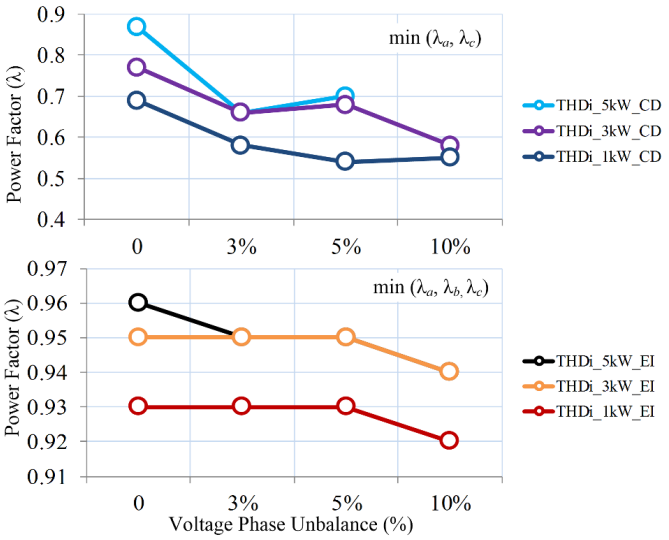


Fig. 13. Measured power factor (λ) for Conventional Drive (CD) and Electronic Inductor (EI) at different output power levels under voltage **phase angle** unbalanced condition.

B. Experimental Results

Experimental tests are performed for both drive topologies at three different power levels (1 kW, 3 kW and 5 kW) and under unbalanced supply voltage conditions summarized in Table III. Fig. 8 shows the experimental waveforms of three-phase supply voltage and current waveforms for CD at 5% voltage amplitude unbalance condition. Notably, during the voltage unbalance (amplitude deviation in phase "*a*" (red color in Fig. 8) in this study), the CD enters into single phase operation and this results to significantly reduction of the current in phase "a" and increased in other two phases due to asymmetric conduction of diodes. The peak of current in these phases increases with increase in voltage unbalance in the system. This excessive current can risk of overloading in these phases, which can trip overload-protection circuits of the drive.

Similarly tests have been performed with voltage phase angle unbalance at different output power levels. Fig. 9 shows the experimental waveforms of three-phase supply voltage and current waveforms for CD and EI at 3 kW output power with 5% phase angle unbalances (phase angle deviation in phase "*c*" (blue color in Fig. 9) in this study). As it can be seen, the measured current waveforms closely follow the obtained simulation results.

In order to further verify the obtained simulation results, Figs. 10 and 11 illustrate the measured THD_i and power factor when unbalance voltage amplitude is applied to phase "*a*". Fig. 10 shows a significant increase in recorded THD_i values in either of phases "*b*" or "*c*" for the CD. This scenario is completely different in EI topology, where both THD_i and λ value remains almost the same despite of unbalance and load power levels. As it is shown in Fig. 4, EI drive never enters in single phase operation at voltage unbalance conditions and also current in all three phase is almost same. Therefore, maximum THD_i and lowest λ values are presented in Figs. 10 and 11 for EI drive topology.

TABLE IV. MEASURED LINE CURRENT HARMONICS FOR CONVENTIONAL DRIVE (CD) AND ELECTRONIC INDUCTOR (EI) UNDER AMPLITUDE AND PHASE UNBALANCED GRID CONDITIONS AT P_o = 3 KW

Harmonic (n)	Balanced		5% Amplitude Unbalance						5% Phase Unbalance					
	CD	EI	CD			EI			CD			EI		
	i_a^h (%)	i_a^h (%)	i_a^h (%)	i_b^h (%)	i_c^h (%)	i_a^h (%)	i_b^h (%)	i_c^h (%)	i_a^h (%)	i_b^h (%)	i_c^h (%)	i_a^h (%)	i_b^h (%)	i_c^h (%)
3	**1.0**	**0.0**	**59.5**	**80.3**	**83.5**	**5.0**	**2.9**	**1.7**	**43.2**	**97.8**	**76.7**	**3.5**	**4.4**	**1.1**
5	65.1	20.8	55.8	51.2	55.6	23.7	19.4	18.8	44.5	79.5	46.5	17.8	23.0	21.3
7	44.9	13.2	58.8	23.7	27.8	10.5	14.2	14.1	32.6	57.9	24.4	14.3	11.0	13.3
9	**0.1**	**0.1**	**53.2**	**7.9**	**11.3**	**5.0**	**2.3**	**2.3**	**3.4**	**35.9**	**14.0**	**3.9**	**4.1**	**0.3**
11	9.6	9.0	57.6	5.7	8.6	10.7	7.5	7.3	8.3	20.1	5.8	6.0	10.4	9.2
13	9.2	7.2	50.9	3.6	6.5	3.8	8.1	8.0	5.2	13.2	4.9	8.1	4.5	7.2

As it can be seen the current harmonics of CD are significantly higher in phases "*b*" and "*c*" which are operating almost in the single-phase conduction mode. These significant harmonic contents in line currents can increase THD_i and degrade power factor (λ) as shown in Figs. 10 and 11 respectively. It is also important to highlight that the single–phase mode operation of the three- phase system due to unbalanced grid voltage can magnify the unbalanced issue of the grid.

Similar to amplitude unbalance, harmonics and power factor performance of CD degrade in case of phase unbalance are depicted in Figs. 12 and 13 (notably, CD enter in protection mode in case of 5 kW output power at 10% phase angle unbalance). However, results show that CD performance is more sensitive with voltage amplitude unbalance compare to equal percentage of phase angle unbalance. On the other hand, EI topology performance remains very consistent in both amplitude and phase angle unbalances.

During voltage unbalance, the input current harmonics are not restricted to the three-phase diode rectifier characteristic harmonics, but uncharacteristic triplen harmonics can also appear such as the third and the ninth harmonics as verified in Table IV. It should be noted that measured current harmonic amplitudes are matched with the developed mathematical models, however the existing difference is due to the effect of grid impedance. The dominance of the third harmonic in all three phases can be clearly observed in CD system.

IV. CONCLUSION

In this paper, the influence of voltage unbalance events on the performance of an EI-based ASD has been investigated, simulated and tested and the results are compared with the conventional diode rectifier based drive system. The obtained practical measurements and simulation results highlight the effectiveness of the EI technique for a wide range of unbalanced grid voltages. The CD performance in terms of harmonics and power factor is more sensitive to the voltage amplitude unbalance, but EI performance is very consistent in both amplitude and phase unbalance conditions.

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