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Comparative Admittance-based Analysis for Different Droop Control Approaches in DC Microgrids

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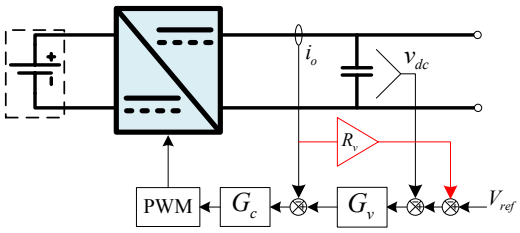
***Abstract*—In DC microgrids, virtual resistance based droop control is broadly used as the fundamental coordination method. As the virtual resistance guarantees load sharing effect in steady states, the output admittance determines the dynamic response of converters in transient states, which is critical in stability analysis and system design. So far, two different approaches of droop control (i.e. *V-I* droop and *I-V* droop) are proposed. Although they can achieve the same steady-state power sharing effect and fully compliable with each other, the output characteristics are not the same due to significant difference in control architecture. In this paper, a comparative admittance-based analysis is carried out between these two approaches. State-space models and more general analytical models are established to derive the output admittance of droop-controlled converter in DC microgrids. Simulations and impedance measurement is carried out using PLECS to validate the analytical results.**

Keywords—DC microgrids; droop control; output impedance; stability; virtual resistance; constant power load

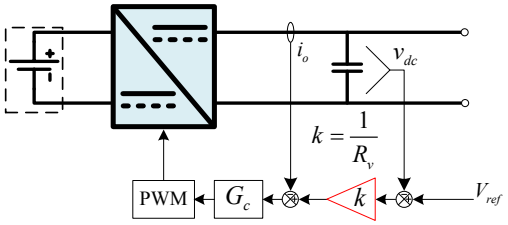
I. INTRODUCTION

With the increasing penetration of renewable energy and the rapid growth of modern electronic loads that inherently consume DC power, the concept of DC microgrids (MGs) is becoming attractive in both mobile and stationary applications, especially in off-grid and islanded cases [1-4]. By packing distributed energy sources and loads together with energy storages, DC MGs can operate as an independent and self-sustainable entity. When compared with its AC counterparts, DC MGs can provide better compliance and efficiency and eliminate several unwanted problems of AC distribution [2].

So far, droop control is broadly used in both AC and DC MGs to share the loads among paralleled power sources properly without introducing communication or additional losses [5], [6]. In DC MGs, virtual resistance based droop approaches are commonly implemented. With virtual resistance equal to the maximum voltage tolerance divided by the maximum output current of the converter, the loads can be shared among paralleled energy sources proportional to their power rating. In addition to that, the presence of virtual resistance effectively avoids circulating current caused by measurement errors, thus maintaining stable operation. So far, two different approaches have been proposed to achieve such a control function, which are the conventional *V-I* droop method presented in [7] and [8], and the emerging *I-V* droop method, as known as reverse-droop method, presented in [9], [10] and [11]. Fig. 1 illustrates the different control architectures of these two approaches. Although these two droop approaches are fully compatible with each other, considerable difference can be seen from transient responses, which means their stability margin are unequal.



(a) Control diagram of *V-I* droop method



(b) Control diagram of *I-V* droop method

Fig. 1. Control architectures of different droop approaches.

The system-level stability is a critical and challenging issue in the field of DC MGs. As DC MGs are power electronic based distribution network, which means majority of the loads will be interfaced by tightly controlled converters with control bandwidth high enough to make the consumed power independent from the bus voltage variations, namely constant power loads (CPLs). When operating in DC systems, CPLs will perform a negative incremental impedance characteristic, which can lead to instability [12]. The study associated with this instability issue can be traced back to 1976, when the interaction between the input filter and power converter was firstly analyzed in [13], in which the Middlebrook stability criterion is proposed. As the criterion is very conservative for designing controllers, several relaxed stability criterions have been proposed in the later studies, as reviewed in [14] and [15]. For all these stability criterions, it is mandatory to derive the accurate output impedance/admittance of the source-side converters to conduct stability analysis. In [16], the output impedance characteristics of common types (Buck, Boost and

Buck-Boost) of DC/DC converters are analyzed in detail. However, the analysis is based on small-signal model that assumes the converter is working around a specific operation point, usually the system's nominal voltage. It is acceptable for voltage mode controlled system, but not for droop controlled cases that have load-dependent bus voltage within a considerable range (e.g. ±10%) of operational points. In [17] and [18], the authors modeled droop controlled source converters as Thévenin equivalents with open-circuit voltages equal to the voltage references and output resistance equal to the virtual resistance, and use such model to evaluate the stability of DC MGs. To the author's opinion, such a modeling method can be sufficiently accurate at the low-frequency range to make steady state analysis. However, due to the limited bandwidth of the voltage and/or current controllers, the output impedance shall vary with frequency, which is more critical to be evaluated in stability analysis.

In this paper, the output characteristics of both *V-I* and *I-V* droop-controlled converters are analyzed. For comparison, two detailed state-space based models are established for a notional DC MG feeding by two droop-controlled buck converters. By deriving the transfer functions from the established models, the output admittance of droop-controlled converters are obtained and compared. In addition, by fairly simplifying current loops as first-order delay with time constant derived by its control bandwidth, generalized analytical models are derived for other cases. From the generalized models, two modified Thévenin equivalents of both *V-I* and *I-V* droop-controlled converters are deduced. To verify the proposed modeling work and analytical results, especially the stability margin, simulations are carried out with both approaches using PLECS and its impedance measurement function.

II. Modeling of Droop-Controlled Converters

In this paper, a notional DC microgrid composed by two parallel connected droop controlled Buck converters as source converters feeding point-of-load converter (as CPL) is selected as the study case, as shown in Fig. 2. The notional microgrid is modeled based on the following assumptions:

1) The inputs of the source converters can be regarded as ideal voltage sources.
2) The distance between source converters and load converters are short, the line impedance is neglectable.

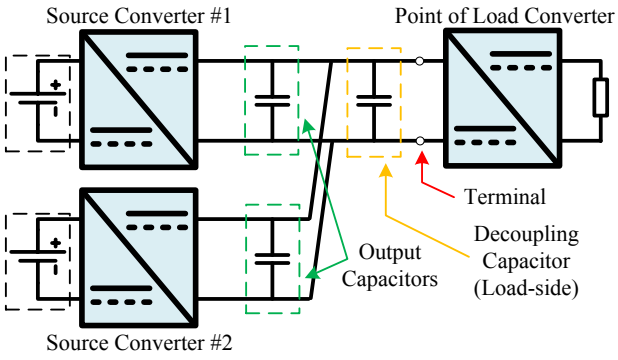


Fig. 2. Control architectures of different droop approaches.

A. State-space Model for V-I Droop Controlled Case

For the *i*-th Buck converters, the increment of the average output current can be described by the differential equations as:

$$\begin{cases} L_i \dfrac{di_{oi}}{dt} = E_i d_i - u - r_i i_{oi} \\ C \dfrac{du}{dt} = \sum i_{oi} - i_{Load} \end{cases} \quad (i \in \{1,2\}) \tag{1}$$

where the subscript i represents the i-th converter, E_i, and d_i are the input voltage and the duty cycle, respectively. L_i, r_i and i_{oi} stands for the inductance, the stray resistance, the average current of the inductor, respectively. C, u, and i_{Load} are the total capacitance connected to the common DC bus, the voltage of common DC bus, and the load current.

When adopting conventional *V-I* droop method, the duty cycle d_i follows the following equations:

$$d_i = K_{pci}\left(i_{refi} - i_{oi}\right) + K_{ici}\int_0^t \left(i_{refi} - i_{oi}\right)dt \tag{2}$$

$$i_{refi} = K_{pvi}\left(V_{ref} - u - R_{vi} i_{oi}\right) + K_{ivi}\int_0^t \left(V_{ref} - u - R_{vi} i_{oi}\right)dt \tag{3}$$

where K_{pci}, K_{pvi} represents the proportional term of current and voltage PI controller, respectively. Similarly, K_{ici} and K_{ivi} are the integral term of current and voltage PI controller. R_{vi} is the virtual resistance of the droop control. V_{ref} is the global no-load voltage reference of the droop control.

Rewrite (2) and (3) as differential equations:

$$\frac{dd_i}{dt} = K_{pci}\frac{di_{refi}}{dt} - K_{pci}\frac{di_{oi}}{dt} + K_{ici} i_{refi} - K_{ici} i_{oi} \tag{4}$$

$$\frac{di_{refi}}{dt} = K_{pvi}\frac{dV_{ref}}{dt} - K_{pvi}\frac{du}{dt} - K_{pvi}R_{vi}\frac{di_{oi}}{dt} + K_{ivi}\left(V_{ref} - u - R_{vi} i_{oi}\right) \tag{5}$$

As V_{ref} is a time-invariant parameter, substitute (1) into (5), the equation will be:

$$\begin{aligned} \frac{di_{refi}}{dt} = {} & K_{ivi}\left(V_{ref} - u - R_{vi} i_{oi}\right) - K_{pvi}\left(\sum \frac{i_{oi}}{C} - \frac{i_{Load}}{C}\right) \\ & - K_{pvi}R_{vi}\left(\frac{E_i}{L_i} d_i - \frac{u}{L_i} - \frac{r_i}{L_i} i_{oi}\right) \end{aligned} \tag{6}$$

Substitute (6) into (4), the equation can be rewritten as:

$$\begin{aligned} \frac{dd_i}{dt} = {} & K_{pci}K_{ivi}\left(V_{ref} - u - R_{vi} i_{oi}\right) - K_{pci}K_{pvi}\left(\sum \frac{i_{oi}}{C} - \frac{i_{Load}}{C}\right) \\ & - \left(K_{pci}K_{pvi}R_{vi} + K_{pci}\right)\left(\frac{E_i}{L_i} d_i - \frac{u}{L_i} - \frac{r_i}{L_i} i_{oi}\right) + K_{ici} i_{refi} - K_{ici} i_{oi} \end{aligned} \tag{7}$$

By combining (1), (6) and (7), a state-space model can be derived as following:

$$\dot{\boldsymbol{X}} = \boldsymbol{AX} + \boldsymbol{BU}, \quad \boldsymbol{Y} = \boldsymbol{CX}, \tag{8}$$

$$\boldsymbol{X} = \left[x_1, x_2, u\right]^T, \boldsymbol{U} = \left[V_{ref}, i_{Load}\right]^T, \boldsymbol{x_i} = \left[i_{oi}, i_{refi}, d_i\right]$$

$$\boldsymbol{A} = \begin{bmatrix} \boldsymbol{J_1} & \boldsymbol{M_1} & \boldsymbol{F_1} \\ \boldsymbol{M_2} & \boldsymbol{J_2} & \boldsymbol{F_2} \\ \boldsymbol{C_1} & \boldsymbol{C_1} & 0 \end{bmatrix}, \boldsymbol{B} = \begin{bmatrix} \boldsymbol{B_1} \\ \boldsymbol{B_2} \\ \boldsymbol{C_2} \end{bmatrix}, \boldsymbol{C} = \boldsymbol{I}_{7\times 7} \tag{9}$$

$$\boldsymbol{J_i} = \begin{bmatrix} -\frac{r_i}{L_i} & 0 & \frac{E_i}{L_i} \\ j_{i1} & 0 & \frac{K_{pvi}R_{vi}E_i}{L_i} \\ j_{i2} & K_{ici} & j_{i3} \end{bmatrix}, \boldsymbol{M_i} = \begin{bmatrix} 0 & 0 & 0 \\ -\frac{K_{pvi}}{C} & 0 & 0 \\ -\frac{K_{pvi}K_{pci}}{C} & 0 & 0 \end{bmatrix}, \tag{10}$$

$$\boldsymbol{F_i} = \begin{bmatrix} -\frac{1}{L_i} \\ f_{i1} \\ f_{i2} \end{bmatrix}, \boldsymbol{C_1} = \left[\frac{1}{C}, 0, 0\right], \boldsymbol{C_2} = \left[0, -\frac{1}{C}\right], \boldsymbol{B_i} = \begin{bmatrix} 0 & 0 \\ K_{ivi} & \frac{K_{pvi}}{C} \\ K_{pci}K_{ivi} & \frac{K_{pci}K_{pvi}}{C} \end{bmatrix}$$

$$\begin{cases} j_{i1} = \dfrac{K_{pvi}R_{vi}r_i}{L_i} - \dfrac{K_{pvi}}{C} - K_{ivi}R_{vi}, \\ j_{i2} = \dfrac{K_{pci}r_i\left(K_{pvi}R_{vi}+1\right)}{L_i} - \dfrac{K_{pci}K_{pvi}}{C} - K_{ici} - K_{pci}K_{ivi}R_{vi}, \\ j_{i3} = -\dfrac{K_{pci}E_i(K_{pvi}R_{vi}+1)}{L_i}, \end{cases} \tag{11}$$

$$\begin{cases} f_{i1} = \dfrac{K_{pvi}R_{vi}}{L_i} - K_{ivi}, \\ f_{i2} = \dfrac{K_{pci}\left(K_{pvi}R_{vi}+1\right)}{L_i} - K_{pci}K_{ivi}, \end{cases}$$

In the state-space model, the study case of this paper is modeled. To make the model scalable, the dynamic response of converters are described as a set of five component matrixes. Among them, the component matrix $\boldsymbol{M_i}$ is describing coupling effect among parallel connected converters, while the others are set to describe the internal control effect of *i*-th converter. When extended to a *n*-converter case, the matrixes $\boldsymbol{A}$, $\boldsymbol{B}$, and $\boldsymbol{C}$ shall be organized as following:

$$\boldsymbol{X} = \left[x_1, \cdots, x_n, u\right]^T, \boldsymbol{U} = \left[V_{ref}, i_{Load}\right]^T, \boldsymbol{x_i} = \left[i_{oi}, i_{refi}, d_i\right]$$

$$\boldsymbol{A} = \begin{bmatrix} \boldsymbol{J_1} & \boldsymbol{M_1} & \cdots & \boldsymbol{M_1} & \boldsymbol{F}_1 \\ \boldsymbol{M_2} & \boldsymbol{J_2} & \cdots & \boldsymbol{M_2} & \boldsymbol{F_2} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \boldsymbol{M_n} & \boldsymbol{M_n} & \cdots & \boldsymbol{J_n} & \boldsymbol{F_n} \\ \boldsymbol{C_1} & \boldsymbol{C_1} & \cdots & \boldsymbol{C_1} & 0 \end{bmatrix}, \boldsymbol{B} = \begin{bmatrix} \boldsymbol{B_1} \\ \vdots \\ \boldsymbol{B_n} \\ \boldsymbol{C_2} \end{bmatrix}, \boldsymbol{C} = \boldsymbol{I}_{(3n+1)\times(3n+1)} \tag{12}$$

B. State-space Model for I-V Droop Controlled Case

When adopting *I-V* droop method, the output current of the *i*-th converters will follow the same equation as shown in (1). However, the current reference i_{refi} and the duty cycle d_i will be calculated by the following equations:

$$i_{refi} = k_i\left(V_{ref} - u\right) \tag{13}$$

$$d_i = K_{pci}\left(k_iV_{ref} - k_iu - i_{oi}\right) + K_{ici}\int_0^t\left(k_iV_{ref} - k_iu - i_{oi}\right)dt \tag{14}$$

$$\begin{cases} \dfrac{di_{refi}}{dt} = -k_i\dfrac{du}{dt} = k_i\dfrac{i_{Load}}{C} - k_i\sum\dfrac{i_{oi}}{C} \\ \dfrac{dd_i}{dt} = K_{ici}\left(k_iV_{ref} - k_iu - i_{oi}\right) + K_{pci}k_i\left(\dfrac{i_{Load}}{C} - \sum\dfrac{i_{oi}}{C}\right) \\ \qquad - K_{pci}\left(\dfrac{E_i}{L_i}d_i - \dfrac{u}{L_i} - \dfrac{r_i}{L_i}i_{oi}\right) \end{cases} \tag{15}$$

where k_i equals to the reciprocal of virtual resistance used in conventional *V-I* droop method, which represents conductance of the virtual resistor in physics.

By combining (1) and (15) a similar state-space model can be derived as following:

$$\dot{\boldsymbol{X}} = \boldsymbol{A'X} + \boldsymbol{B'U}, \quad \boldsymbol{Y} = \boldsymbol{CX}, \tag{16}$$

$$\boldsymbol{X} = \left[x_1, x_2, u\right]^T, \boldsymbol{U} = \left[V_{ref}, i_{Load}\right]^T, \boldsymbol{x_i} = \left[i_{oi}, i_{refi}, d_i\right]$$

$$\boldsymbol{A'} = \begin{bmatrix} \boldsymbol{J_1'} & \boldsymbol{M_1'} & \boldsymbol{F_1'} \\ \boldsymbol{M_2'} & \boldsymbol{J_2'} & \boldsymbol{F_2'} \\ \boldsymbol{C_1} & \boldsymbol{C_1} & 0 \end{bmatrix}, \boldsymbol{B'} = \begin{bmatrix} \boldsymbol{B_1'} \\ \boldsymbol{B_2'} \\ \boldsymbol{C_2} \end{bmatrix}, \boldsymbol{C} = \boldsymbol{I}_{7\times 7} \tag{17}$$

$$\boldsymbol{J_i'} = \begin{bmatrix} -\frac{r_i}{L_i} & 0 & \frac{E_i}{L_i} \\ -\frac{k_i}{C} & 0 & 0 \\ j_i' & 0 & -\frac{K_{pci}E_i}{L_i} \end{bmatrix}, \boldsymbol{M_i'} = \begin{bmatrix} 0 & 0 & 0 \\ -\frac{k_i}{C} & 0 & 0 \\ -\frac{k_iK_{pci}}{C} & 0 & 0 \end{bmatrix},$$

$$\boldsymbol{F_i'} = \begin{bmatrix} -\frac{1}{L_i} \\ 0 \\ \frac{K_{pci}}{L_i} - k_iK_{ici} \end{bmatrix}, \boldsymbol{C_1} = \left[\frac{1}{C}, 0, 0\right], \boldsymbol{C_2} = \left[0, -\frac{1}{C}\right], \boldsymbol{B_i'} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{k_i}{C} \\ k_iK_{ici} & \frac{k_iK_{pci}}{C} \end{bmatrix} \tag{18}$$

$$j_i' = \frac{K_{pci}r_i}{L_i} - \frac{k_iK_{pci}}{C} - K_{ici}$$

The derived state-space model for *I-V* droop controlled case maintains the scalability of the previous model. By organizing the component matrixes as shown in (12), the state-space model can also be extended to a *n*-converter case. In addition to that, the component matrixes shown in (10) and (18) are interchangeable. Thus, the derived framework of state-

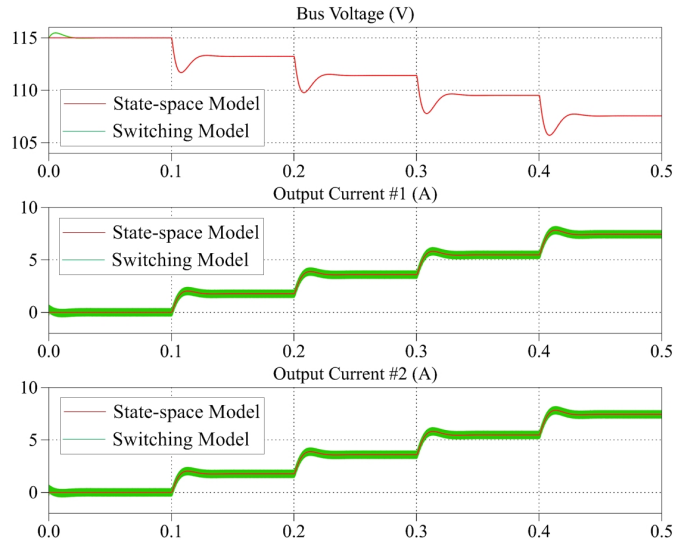


Fig. 3. Simulation results of *V-I* droop controlled case.

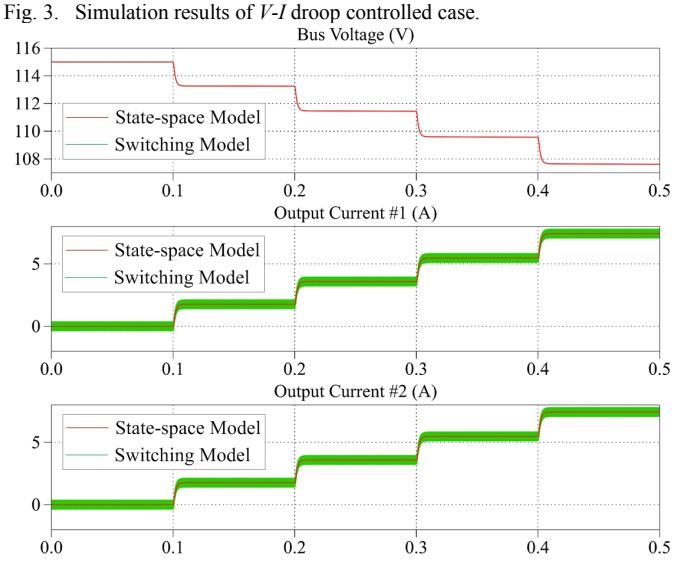


Fig. 4. Simulation results of *V-I* droop controlled case.

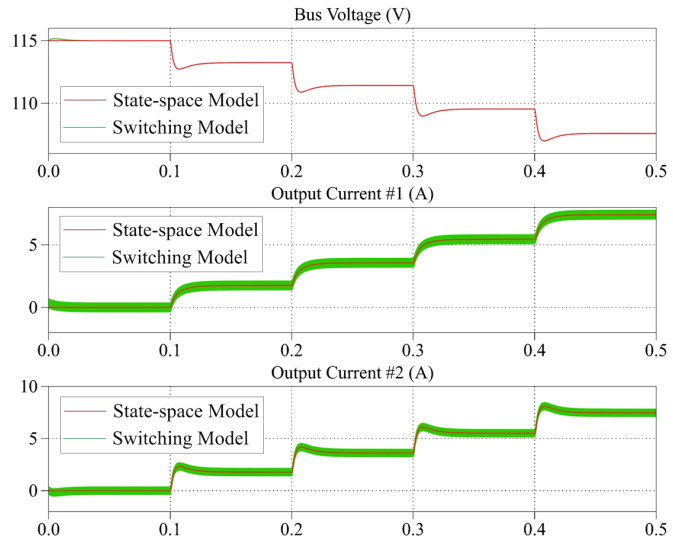


Fig. 5. Simulation results of mixed droop controlled case. Converter #1 is *V-I* droop controlled, converter #2 is *I-V* droop controlled.

space model can also describe the dynamic response of mixed droop-controlled cases of DC microgrids.

C. *Simulation Validation of the Derived Models*

To validate the derived state-space models, simulations of abovementioned study case are carried out using PLECS. The simulation results are as shown in Fig. 3, Fig. 4, and Fig. 5. For this simulation, the parameters of the simulated study case are listed in Table. I.

TABLE I. PARAMETERS OF SIMULATED STUDY CASE

Description of the Parameter	***Symbol***	***Value***
Global No-load Voltage Reference	V_{ref}	115 V
Source Voltage	E_1, E_2	230 V, 230 V
Inductance of Buck Converters	L_1, L_2	8 mH, 8 mH
Stary Resistance of inductors,	r_1, r_2	0.1 Ω, 0.1 Ω
Switching Frequency	f_{sw}	10 kHz
Virtual Resistances for Droop Control	R_{v1}, R_{v2}	1 Ω, 1 Ω
Total Capacitance in DC Bus	C	3.3 mF
Proportion Term of Voltage Controller	K_{pv1}, K_{pv2}	0.5, 0,5
Integral Term of Voltage Controller	K_{iv1}, K_{iv2}	100, 100
Proportion Term of Current Controller	K_{pc1}, K_{pc2}	0.2, 0.2
Integral Term of Current Controller	K_{ic1}, K_{ic2}	1, 1
Load Profile	P_{Load}	0.4 kW/step

As a conclusion, the derived state-space models have sufficient accuracy and can describe the dynamic of source converters properly.

III. OUTPUT ADMITTANCE ANALYSIS OF DROOP-CONTROLLED CONVERTERS

As shown in Fig. 5, even though the virtual resistances and the current controllers are exactly the same value, the dynamics of *V-I* and *I-V* droop controlled converters are different. In this section, the output admittance of *V-I* and *I-V* droop controlled converter is analyzed to address the mechanism.

A. *Deriving Output Admittance from State-space Models*

As droop control is to make the converter act as Thévenin equivalent branch, at least in its steady states, an effective way to describe their dynamic is the same way. According to the Thévenin's theorem, the output admittance of source converters can be calculated by:

$$Y_{eq} = \frac{I}{V_{oc} - u} \tag{19}$$

$$Y_{eq}(s) = \frac{\Delta I(s)}{\Delta\left(V_{ref}(s) - u(s)\right)} = \frac{\Delta I_o(s) - \Delta I_c(s)}{-\Delta u(s)} = \frac{\Delta I_o(s)}{-\Delta u(s)} + sC \tag{20}$$

where $I(s)$, $I_o(s)$, $I_c(s)$ and $u(s)$ are the terminal output current, inductor current, capacitor current and terminal voltage of the converter. V_{oc} is the open-circuit voltage, which equals to the global no-load voltage reference.

From (20) it can be derived that the output admittance of source converters is depending on converter's dynamic and the total capacitance of the common DC bus. As abovementioned, the converter's dynamic can be descripted by derived state-space models properly. Therefore, a small-signal model of the converter's output admittance can be derived by:

$$\boldsymbol{G}=\boldsymbol{C}(s\boldsymbol{I}-\boldsymbol{A})^{-1}\boldsymbol{B}=\begin{bmatrix} G_{i_{o1}ref}(s) & G_{i_{o1}Load}(s) \\ G_{i_{ref\,1}ref}(s) & G_{i_{ref\,1}Load}(s) \\ G_{d_1ref}(s) & G_{d_1Load}(s) \\ G_{i_{o2}ref}(s) & G_{i_{o2}Load}(s) \\ G_{i_{ref\,2}ref}(s) & G_{i_{ref\,2}Load}(s) \\ G_{d_2ref}(s) & G_{d_2Load}(s) \\ G_{uref}(s) & G_{uLoad}(s) \end{bmatrix} \tag{21}$$

$$\begin{aligned}\frac{\Delta I_o(s)}{\Delta u(s)}=&\frac{G_{i_{o1}ref}(s)\Delta V_{ref}(s)+G_{i_{o1}Load}(s)\Delta I_{Load}(s)}{G_{uref}(s)\Delta V_{ref}(s)+G_{uLoad}(s)\Delta I_{Load}(s)}\\&+\frac{G_{i_{o2}ref}(s)\Delta V_{ref}(s)+G_{i_{o2}Load}(s)\Delta I_{Load}(s)}{G_{uref}(s)\Delta V_{ref}(s)+G_{uLoad}(s)\Delta I_{Load}(s)}\end{aligned} \tag{22}$$

As the global voltage reference is constant while talking only about droop control, the equation can be simplified as:

$$\frac{\Delta I_o(s)}{\Delta u(s)}=\frac{G_{i_{o1}Load}(s)+G_{i_{o2}Load}(s)}{G_{uLoad}(s)} \tag{23}$$

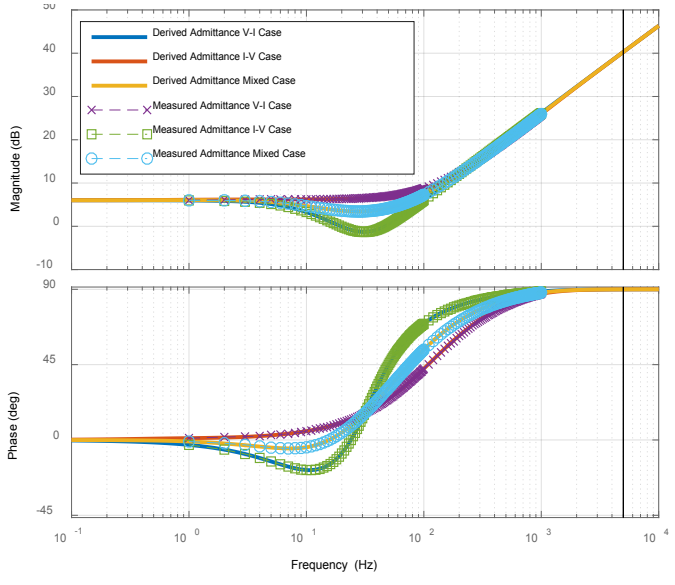


Fig. 6. Frequency Response of State-space Model-Derived and Measured Source-side Output Admittance.

For the study cases discussed in the above sections, their source-side output admittance is derived and illustrated in Fig. 6. At the same time, by using the impedance measurement function of PLECS, the output admittance of simulated study cases can be measured. The results of measured admittance are also shown as the dashed lines with marks in Fig. 6. It can be seen from the results that model-derived output admittance matched measured results very well.

B. *Generalized Analytical Model of Output Admittance*

From the results shown in Fig. 6, the source-side output admittance of *V-I* case and *I-V* case are considerably different, mainly happens in the frequency range of 10Hz to 100Hz. A maximum of 7.8 dB magnitude difference can be found. As the capacitance in DC bus is the same in these simulated cases, the converter's dynamic is the dominant factor of such a difference. To the author's opinion, the different controller configuration of *V-I* and *I-V* droop control is the main reason.

As illustrated in Fig. 1, the *V-I* droop controller is a dual-loop voltage controller with an additional feedback loop for the virtual resistance, while *I-V* droop controller is also a dual-loop controller with finite gain voltage controller. Therefore, their dynamic behavior can be descripted by:

$$I_o^{\,V-I}(s)=\frac{G_v(s)G_{clc}(s)}{1+R_vG_v(s)G_{clc}(s)}\left[V_{ref}(s)-u(s)\right] \tag{24}$$

$$I_o^{\,I-V}(s)=\frac{G_{clc}(s)}{R_v}\left[V_{ref}(s)-u(s)\right] \tag{25}$$

where $G_v(s)$ is the transfer function of voltage controller, $G_{clc}(s)$ is the close-loop transfer function of the whole current loop. The superscripts are to differentiate the droop modes.

By combining (24), (25) and (20), the converter's dynamic can be descripted by intrinsic admittance of converter:

$$Y_{conv}^{\,V-I}(s)=\frac{G_v(s)G_{clc}(s)}{1+R_vG_v(s)G_{clc}(s)} \tag{24}$$

$$Y_{conv}^{\,I-V}(s)=\frac{G_{clc}(s)}{R_v} \tag{25}$$

To analyze the behavior of dual-loop controllers, the inner current loop is commonly simplified as a first order delay. Therefore, the equations above can be presented by:

$$Y_{conv}^{\,V-I}(s)=\frac{G_v(s)G_{clc}(s)}{1+R_vG_v(s)G_{clc}(s)}=\frac{\dfrac{(K_{pvi}s+K_{ivi})}{s}\dfrac{\omega_{clc}}{s+\omega_{clc}}}{1+R_v\dfrac{(K_{pvi}s+K_{ivi})}{s}\dfrac{\omega_{clc}}{s+\omega_{clc}}} \tag{26}$$

$$Y_{conv}^{\,I-V}(s)=\frac{1}{R_v}\frac{\omega_{clc}}{s+\omega_{clc}} \tag{27}$$

where ω_{clc} stands for the bandwidth of current loop.

For Buck Converters, the control bandwidth of a well-designed current loop can be approximately calculated by:

$$\omega_{clc} \approx K_{pci} E_i / L_i \tag{28}$$

In Fig. 7, the converter's intrinsic admittance derived by state-space models and generalized analytical models are both illustrated by their frequency response. The results shows that the established generalized model is sufficient accurate to analyze the droop-controlled converter's intrinsic admittance.

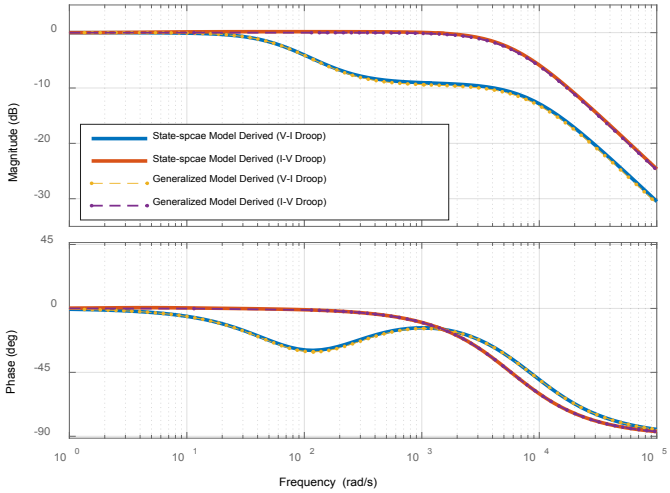


Fig. 7. Frequency Response of Converter's Intrinsic Admittance.

C. *Equivalent Circuit of Droop-controlled Converters*

In [17] and [18], the authors assume that the converter has pure resistive output impedance and established theoretical model based on such an assumption. However, as shown in Fig. 6 and Fig. 7, for both *V-I* and *I-V* droop-controlled converters, the output dynamic show resistive characteristic only in the low-frequency range. Moreover, the feasible range of such modeling method is too narrow to conduct generic stability analysis.

To solve this problem, an alternative solution is to use the converter's intrinsic admittance instead of virtual resistance to establish equivalent model of droop-controlled converters. For *V-I* droop-controlled converters, an equivalent circuit can be derived from (26) as shown in Fig. 8(a). The equivalent circuit of *I-V* droop-controlled converters can be derived from (27), as shown in Fig. 8(b). The inductance and resistance of additional virtual components (marked red in Fig. 8) are as follows:

$$\begin{cases} R_v^{V-I} = R_{vi} \\ L_{v1}^{V-I} = \dfrac{1}{K_{pvi}\omega_{clc}} \\ L_{v2}^{V-I} = \dfrac{\omega_{clc} - K_{ivi}/K_{pvi}}{K_{ivi}\omega_{clc}} \\ R_{Ld}^{V-I} = \dfrac{\omega_{clc} - K_{ivi}/K_{pvi}}{K_{pvi}\omega_{clc}} \end{cases} \qquad \begin{cases} R_v^{I-V} = R_{vi} \\ L_{v1}^{I-V} = \dfrac{R_{vi}}{\omega_{clc}} \end{cases} \tag{29}$$

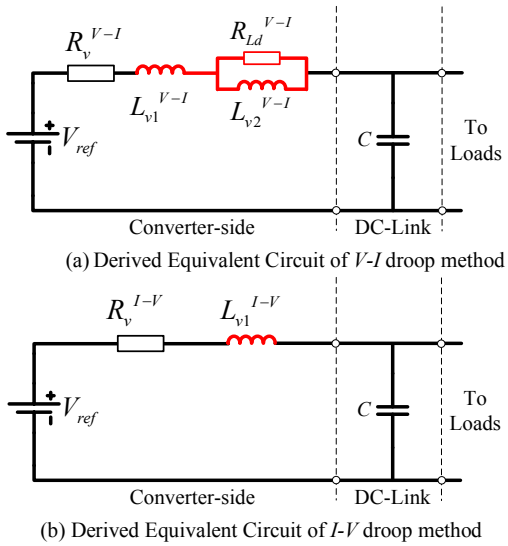


Fig. 8. Derived Equivalent Circuit Model of Droop-controlled Converter.

It is noteworthy that the derived intrinsic admittance and equivalent circuit of *V-I* droop-controlled converter are both also applicable to analyze the behavior of more conventional voltage-controlled converter by simply set virtual resistance to be zero. It can be derived from (26) that *V-I* droop control scheme introduces a virtual resistor that connected in series to the voltage controlled converter's equivalent circuit, while the equivalent circuit itself is not affected by the additional feedback loop. The same conclusion can be also derived from (29) that the additional virtual components are all irrelevant to the virtual resistance.

As for the *I-V* droop method, a significant feature is its finite gain (which take the role of virtual resistance) in voltage control. Also for the same reason, the converter's intrinsic admittance is closely depending on the virtual resistance.

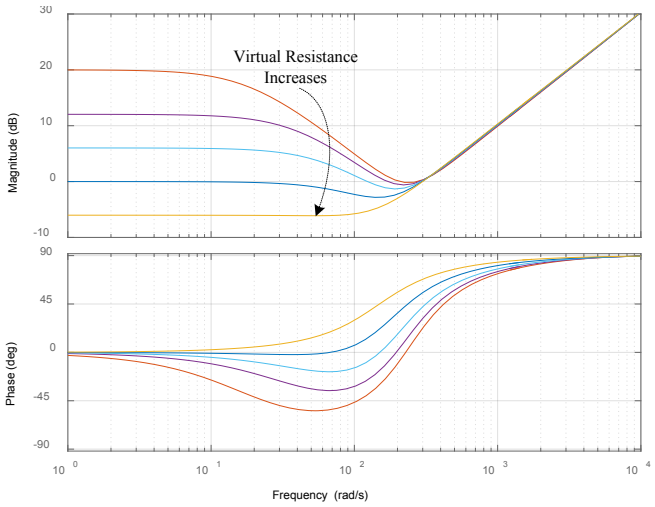


Fig. 9. Frequency Response of Source-side Output Admittance with *V-I* Droop-controlled Converters under Different Virtual Resistance (0.2Ω-4Ω) .

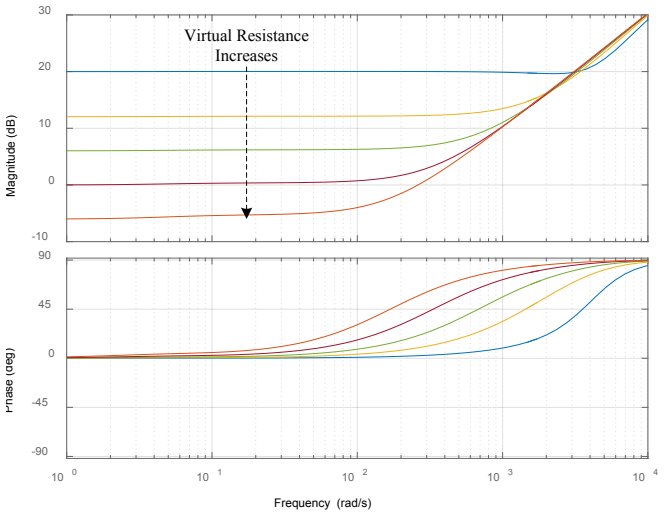


Fig. 10. Frequency Response of Source-side Output Admittance with *I-V* Droop-controlled Converters under Different Virtual Resistance (0.2Ω-4Ω) .

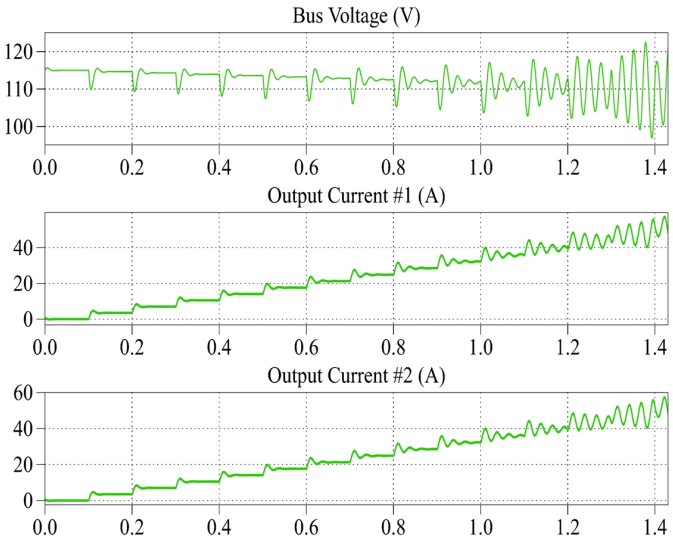


Fig. 11. Simulation results of *V-I* (R_v=0.1Ω) droop-controlled case feeding CPL.

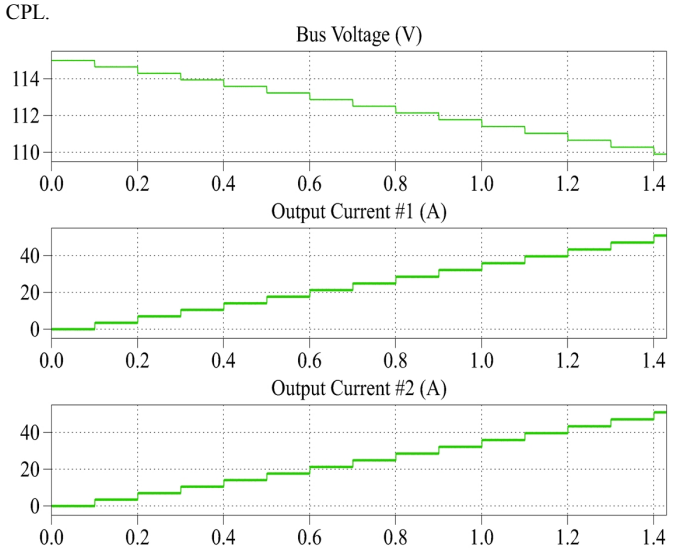


Fig. 12. Simulation results of *I-V* (Rv=0.1Ω) droop-controlled case feeding CPL.

Fig. 9 illustrates the source-side output admittance of *V-I* droop-controlled study case with different virtual resistance (i.e. each virtual resistance increases from 0.2Ω to 4Ω). Fig. 10 illustrates the source-side output admittance of *I-V* droop-controlled study case with the same virtual resistance settings. As a conclusion to the comparison, the *I-V* droop shows better stability margin, especially under small virtual resistances.

In Fig. 11 and Fig. 12, the simulation results of these two approaches feeding CPL is illustrated. The results show that the system damping of *V-I* droop-controlled DC MGs become poorer along with the increase of CPL. The system can be unstable if the CPL is too much. For the same load conditions, *I-V* droop can provide a much larger capability and stability margin when feeding CPL.

IV. Conclusion

In this paper, the output characteristics of both *V-I* and *I-V* droop-controlled converters are analyzed. For comparison, two detailed state-space based models are established for the study case. The proposed framework of state-space model can also be used to analyzed mixed *V-I* and *I-V* droop-controlled DC MG and can be extended to analyze *n*-converters MG. By deriving the transfer functions from the established models, the output admittance of droop controlled converters are obtained and compared. In addition, by fairly simplifying current loops as first-order delay with time constant derived by its control bandwidth, generalized analytical models are derived for other cases. From the generalized models, two modified Thévenin equivalents of both *V-I* and *I-V* droop-controlled converters are deduced. Simulations are carried out using PLECS and its impedance measurement function. The results validate the accuracy of proposed models and analytical results.

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