



## Protection Scheme for Modular Multilevel Converters under Diode Open-Circuit Faults

Deng, Fujin; Zhu, Rongwu; Liu, Dong; Wang, Yanbo; Wang, Huai; Chen, Zhe; Cheng, Ming

*Published in:*

I E E Transactions on Power Electronics

*DOI (link to publication from Publisher):*

[10.1109/TPEL.2017.2702748](https://doi.org/10.1109/TPEL.2017.2702748)

*Publication date:*

2018

*Document Version*

Accepted author manuscript, peer reviewed version

[Link to publication from Aalborg University](#)

*Citation for published version (APA):*

Deng, F., Zhu, R., Liu, D., Wang, Y., Wang, H., Chen, Z., & Cheng, M. (2018). Protection Scheme for Modular Multilevel Converters under Diode Open-Circuit Faults. *I E E Transactions on Power Electronics*, 33(4), 2866 - 2877 . Article 7922575. <https://doi.org/10.1109/TPEL.2017.2702748>

### General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal -

### Take down policy

If you believe that this document breaches copyright please contact us at [vbn@aub.aau.dk](mailto:vbn@aub.aau.dk) providing details, and we will remove access to the work immediately and investigate your claim.

# Protection Scheme for Modular Multilevel Converters Under Diode Open-Circuit Faults

Fujin Deng, *Member, IEEE*, Rongwu Zhu, *Member, IEEE*, Dong Liu, *Student Member, IEEE*, Yanbo Wang, *Member, IEEE*, Huai Wang, *Member, IEEE*, Zhe Chen, *Senior Member, IEEE*, Ming Cheng, *Fellow, IEEE*

**Abstract**--The modular multilevel converter (MMC) is attractive for medium- or high-power applications because of the advantages of its high modularity, availability, and high power quality. Reliability is one of the most important challenges for the MMC consisting of a large number of power electronic devices. The diode open-circuit fault in the submodule (SM) is an important issue for the MMC, which would affect the performance of the MMC and disrupt the operation of the MMC. This paper analyzes the impact of diode open-circuit failures in the SMs on the performance of the MMC and proposes a protection scheme for the MMC under diode open-circuit faults. The proposed protection scheme not only can effectively eliminate the possible caused high voltage due to the diode open-circuit fault but also can quickly detect the faulty SMs, which effectively avoids the destruction and protects the MMC. The proposed protection scheme is verified with a downscale MMC prototype in the laboratory. The results confirm the effectiveness of the proposed protection scheme for the MMC under diode open-circuit faults.

**Index Terms**— Diode faults, modular multilevel converters (MMCs), open-circuit fault, protection.

## I. INTRODUCTION

Modular multilevel converters (MMCs) have become increasingly attractive for high-voltage and high-power applications with the advantages such as the excellent output voltage waveforms, very high efficiency [1-3], etc. A multilevel voltage can be produced with the flexible operation of the MMC while reducing the average switching frequency without compromising the power quality [4]. Recently, due to the easy construction, assembling, and flexibility in converter design, the MMC becomes promising for various applications such as high-voltage direct current transmission [5-7], high power motor drives [8], [9], and electric railway supplies [10].

Reliability is one of the most important challenges for the MMC, where it is desired that MMC can continue operating

without any interruption, even though some of the submodules (SMs) malfunction [11], [12]. The MMC consists of a large number of power electronic devices such as insulated gate bipolar transistor (IGBT), diode, etc., and each device could be a potential failure point [13], [14]. These power electronic device faults may distort the voltage and current, even destroy the MMC and disrupt its operation [14-18]. Therefore, an effective protection scheme is essential for the MMC after the fault occurrences.

To date, a number of studies have been reported for improving reliability of power converters under power electronic device faults such as short-circuit fault and open-circuit fault. The hardware-based methods with the additional sensors are mainly used for short-circuit protection of the switch [19], [20], where the switch is shut down within a short period of time to protect the power converter in case of any short-circuit detection. The software-based methods such as signal processing-based approaches and model-based approaches are widely used for power electronics devices open-circuit fault based on the converter fault characteristics such as distorted voltage and current [19-23]. As to the MMC, a sliding mode observer is presented and investigated to detect the faulty SMs in the MMC under switch open-circuit faults [15]. A Kalman filter is used to detect the faulty phase and a method relying on the SM capacitor voltage is presented to locate the faulty SMs within the faulty phase due to switch open-circuit fault in the MMC [16]. A fault detection method that detects the fault by means of state observers without using any additional sensors is proposed in [12]. A resilient framework is presented for fast SM fault diagnosis and effective restoration in MMCs [17]. A clustering algorithm based method and a calculated capacitance based method are presented for the faulty SMs with open-switch failures in the MMC [18]. The supervisory sensor is presented for the fault detection of the semiconductor switching devices [23]. The above studies are mainly focused on the switch faults in the MMC.

The diode open-circuit fault may occur owing to various reasons, e.g. overcurrent, high temperature fatigue, and mismatch of coefficients of thermal expansion between silicon and aluminum [24-26] would result in bond wire lift-off failure and cause diode open-circuit fault, which is one of the important fault issues for MMCs [14] and may seriously affect the performance of the MMC. In this paper, the fault characteristics of the MMC under diode open-circuit fault are analyzed and an effective protection scheme is proposed. The

---

This work was supported in part by the NSFC under Project 51320105002.

Fujin Deng and Ming Cheng are with the School of Electrical Engineering, Southeast University, Nanjing, 210096, China (dfjqfa@163.com, mcheng@seu.edu.cn)

Rongwu Zhu is with the Chair of Power Electronics, Christian-Albrechts-University of Kiel, 2D-24142, Kiel, Germany (rzh@tf.uni-kiel.de)

Dong Liu, Yanbo Wang, Huai Wang, and Zhe Chen are with the Department of Energy Technology, Aalborg University, Aalborg, 9220 Denmark (dli@et.aau.dk, ywa@et.aau.dk, hwa@et.aau.dk, zch@et.aau.dk).

proposed scheme not only can avoid the possible caused high voltage due to the open-circuit diode but also can quickly detect the faulty SMs, which avoids the destruction and protects the MMC. The effectiveness of the proposed protection scheme is verified based on the experimental test in the laboratory.

This paper is organized as follows. Section II presents the basics of the MMC. Section III and IV analyzes the fault characteristics and proposed the protection scheme for the MMC under diode open-circuit faults, respectively. The system experimental tests are presented in Sections V to show the effectiveness of the proposed protection scheme. Finally, the conclusions are presented in Section VI.

## II. DESCRIPTION OF MMCs

Fig. 1(a) shows a three-phase MMC, which is composed of six arms. Each arm consists of  $n$  identical SMs and an arm inductor  $L_s$ . The upper arm and the lower arm in the same phase comprise a phase unit. Fig. 1(b) shows a SM, which contains a half bridge, a capacitor  $C_{sm}$ , and a bypass switch  $S_w$ . Each half bridge is composed of a top IGBT/Diode ( $T_t/d_t$ ) and a bottom IGBT/Diode ( $T_b/d_b$ ) [27-30]. The  $S_w$  is used to bypass the SM in case of a failure [31].

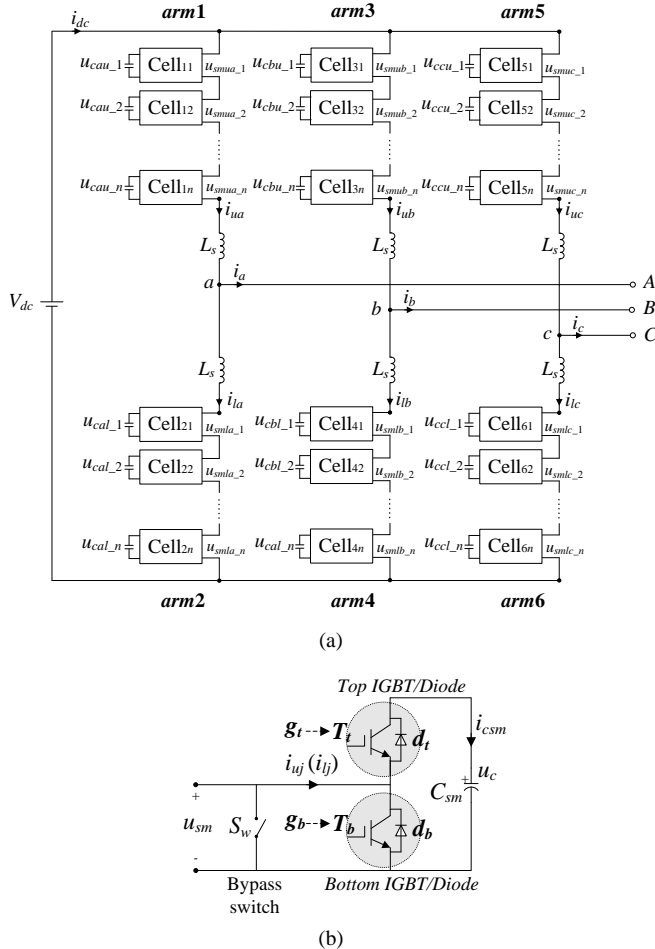


Fig. 1. (a) Block diagram of a three-phase MMC. (b) SM unit.

In normal operation, each SM shown in Fig. 1(b) is controlled with a switching function  $S$ , which is defined as

$$S = \begin{cases} 1, & g_t = 1 \ \& \ g_b = 0 \\ 0, & g_t = 0 \ \& \ g_b = 1 \end{cases} \quad (1)$$

where  $g_t$  and  $g_b$  are gate signals for  $T_t$  and  $T_b$ , respectively. The gate-source voltage of the  $T_t$  ( $T_b$ ) is below the threshold voltage when  $g_t=0$  ( $g_b=0$ ) and above the threshold voltage when  $g_t=1$  ( $g_b=1$ ) [32]. Normally, each SM is operated with four modes depending on the arm current direction and  $S$ , as shown in Table I. Suppose that the arm current  $i_{uj}$  and  $i_{lj}$  ( $j=a, b,$  and  $c$ ) flow direction in Fig. 1 is defined as the positive direction, the SM works in mode 1 when  $i_{uj}$  ( $i_{lj}$ ) is positive and  $S=1$ , where the output voltage  $u_{sm}$  equals  $u_c$  and the capacitor  $C_{sm}$  is charged and  $u_c$  is increased. The SM works in mode 3 when  $i_{uj}$  ( $i_{lj}$ ) is negative and  $S=1$ , where  $u_{sm}$  equals  $u_c$  and  $C_{sm}$  is discharged and  $u_c$  is decreased. In mode 2 and 4 with  $S=0$ ,  $u_{sm}$  equals 0 and  $C_{sm}$  is bypassed and  $u_c$  is unchanged, irrespective of the arm current flow direction [33].

TABLE I  
OPERATION MODES OF THE SM

Mode	current $i_{uj}$ or $i_{lj}$	$S$	$g_t$	$g_b$	$u_{sm}$	Capacitor $C_{sm}$ state	Capacitor voltage $u_c$
1	$\geq 0$	1	1	0	$u_c$	Charge	Increased
2		0	0	1	0	Bypass	Unchanged
3	$< 0$	1	1	0	$u_c$	Discharge	Decreased
4		0	0	1	0	Bypass	Unchanged

In Fig. 1, the arm current  $i_{uj}$  and  $i_{lj}$  can be described as

$$\begin{cases} i_{uj} = \frac{i_j}{2} + i_{diff-j} \\ i_{lj} = -\frac{i_j}{2} + i_{diff-j} \end{cases} \quad (2)$$

where  $i_j$  is the AC current of phase  $j$ .  $i_{diff-j}$  is the inner difference current of phase  $j$ , which contains the dc component  $i_{dc}/3$  and the circulating current  $i_{2f-j}$  in phase  $j$ , as (3) [27].

$$i_{diff-j} = \frac{i_{uj} + i_{lj}}{2} = \frac{i_{dc}}{3} + i_{2f-j} \quad (3)$$

According to [34], the voltage relationship in the MMC is

$$V_{dc} = \sum_{i=1}^n u_{smuj-i} + \sum_{i=1}^n u_{smlj-i} + u_{ulj} + u_{llj} \quad (4)$$

with

$$\begin{cases} u_{ulj} = L_s \frac{di_{uj}}{dt} \\ u_{llj} = L_s \frac{di_{lj}}{dt} \end{cases} \quad (5)$$

where  $V_{dc}$  is the dc bus voltage.  $u_{smuj-i}$  and  $u_{smlj-i}$  are the  $i$ -th SM output voltage in the upper and lower arms of phase  $j$ , respectively, as shown in Fig. 1.  $u_{ulj}$  and  $u_{llj}$  are the upper and lower arm inductor voltage of phase  $j$ , respectively.

## III. ANALYSIS OF MMCs UNDER DIODE FAULTS

Fig. 2 shows two types of possible diode open-circuit faults in the  $k$ -th SM of upper arm of phase A.

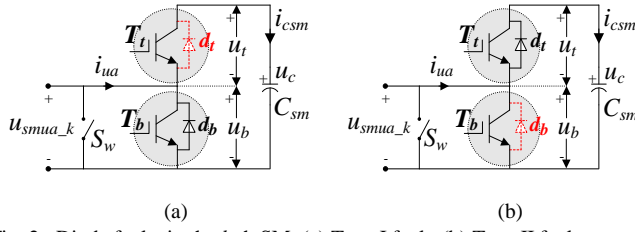


Fig. 2. Diode faults in the  $k$ -th SM. (a) Type I fault. (b) Type II fault.

### A. Type I Fault Situation

Fig. 2(a) shows the Type I fault, where open-circuit fault occurs in the top diode  $d_t$ . Tables II and III show the four modes of the SM under Type I fault. The SM works as normal in modes 2~4. In mode 2 ( $i_{ua} \geq 0$  and  $S=0$ ),  $i_{ua}$  circulates through  $T_b$  with  $u_t = u_c$ ,  $u_b = 0$ ; in mode 3 ( $i_{ua} < 0$  and  $S=1$ ),  $i_{ua}$  circulates through  $C_{sm}$  and  $T_t$  with  $u_t = 0$ ,  $u_b = u_c$ ; in mode 4 ( $i_{ua} < 0$  and  $S=0$ ),  $i_{ua}$  flows through  $d_b$  with  $u_t = u_c$ ,  $u_b = 0$ . However, in mode 1,  $i_{ua}$  can not flow through the faulty  $d_t$  when  $S$  is changed to 1 ( $g_t=1$  and  $g_b=0$ ) under  $i_{ua} \geq 0$ .

TABLE II  
SM CHARACTERISTICS UNDER FAULT SITUATIONS

Mode	$i_{ua}$	$S$	$i_{ua}$ flows through		
			Normal operation	Type I fault	Type II fault
1	$\geq 0$	1	$d_t$ & $C_{sm}$	High $-u_t$ and $u_b$ ( $u_b >  u_t $ )	$d_t$ & $C_{sm}$
2		0	$T_b$	$T_b$	$T_b$
3		1	$C_{sm}$ & $T_t$	$C_{sm}$ & $T_t$	$C_{sm}$ & $T_t$
4	$< 0$	0	$d_b$	$d_b$	High $u_t$ and $-u_b$ ( $u_t >  u_b $ )

TABLE III  
SM VOLTAGES UNDER FAULT SITUATIONS

Mode	$i_{ua}$	$S$	Normal operation		Type I fault		Type II fault	
			$u_t$	$u_b$	$u_t$	$u_b$	$u_t$	$u_b$
1	$\geq 0$	1	0	$u_c$	$< 0$	$> u_c$	0	$u_c$
2		0	$u_c$	0	$u_c$	0	$u_c$	0
3		1	0	$u_c$	0	$u_c$	0	$u_c$
4	$< 0$	0	$u_c$	0	$u_c$	0	$> u_c$	$< 0$

According to (4), in mode 1, the voltage in phase A can be described as (6) at the initial time  $t_{01}$  when  $S$  is changed to 1.

$$V_{dc} = \sum_{i=1}^n u_{smua\_i}(t_{01}) + \sum_{i=1}^n u_{smla\_i}(t_{01}) + u_{ula}(t_{01}) + u_{lla}(t_{01}) \quad (6)$$

Suppose that the  $i_{ua}$  can be blocked by switching off  $T_b$  in the  $k$ -th SM when  $S$  is changed to 1 into mode 1, and normally the turn-off time  $\Delta t$  of the IGBT is around  $1 \mu s$  [32], a high voltage  $u_{ula}$  would be caused on the upper arm inductor of phase A, as

$$u_{ula}(t_{\Delta t1}) = -L_s \frac{i_{ua}(t_{01})}{\Delta t} \quad (7)$$

where  $i_{ua}(t_{01})$  is the upper arm current at the time  $t_{01}$ . According to KVL [35], the voltage  $u_{smua\_k}$  imposed on the  $k$ -th SM in phase A can be obtained as:

$$u_{smua\_k}(t_{\Delta t1}) = V_{dc} - \sum_{i=1}^{k-1} u_{smua\_i}(t_{\Delta t1}) - \sum_{i=k+1}^n u_{smua\_i}(t_{\Delta t1})$$

$$- \sum_{i=1}^n u_{smla\_i}(t_{\Delta t1}) - u_{ula}(t_{\Delta t1}) - u_{lla}(t_{\Delta t1}) \quad (8)$$

Except for the  $k$ -th SM output voltage  $u_{smua\_k}$ , assuming that the other SM output voltages and the lower arm inductor voltage  $u_{lla}$  in phase A are not changed during the very short time  $\Delta t$ , substituting (6) and (7) into (8), there is

$$u_{smua\_k}(t_{\Delta t1}) = L_s \frac{i_{ua}(t_{01})}{\Delta t} + u_{smua\_k}(t_{01}) + u_{ula}(t_{01}) \quad (9)$$

Normally, the arm inductance  $L_s$  is selected around the order of mH [4-8], [27-30]. According to (9) and neglecting  $u_{smua\_k}(t_{01})$  and  $u_{ula}(t_{01})$ , a high voltage  $u_{smua\_k}$  would be caused under various  $L_s$  and  $i_{ua}(t_{01})$ , as shown in Fig. 3. It can be observed that  $u_{smua\_k}$  may reach a very high voltage if the arm current can be blocked by the IGBT under faults. Actually, the voltage  $u_{smua\_k}$  could not reach a very high value under faults because the faulty SM is already destroyed before  $u_{smua\_k}$  increases to such a high value. Consequently, in mode 1, the high voltage  $u_t$  and  $u_b$ , shown in Fig. 2(a), may be quickly caused in faulty SMs with the relationship of

$$\begin{cases} u_t = u_c - u_{smua\_k} \\ u_b = u_{smua\_k} \end{cases} \quad (10)$$

where  $u_b > |u_t|$  and  $u_t < 0$ , as listed in Table III. From (9) and (10), it can be seen that a high reverse voltage  $-u_t$  and a high voltage  $u_b$  would be quickly caused in the faulty SM in mode 1 and may destroy the MMC.

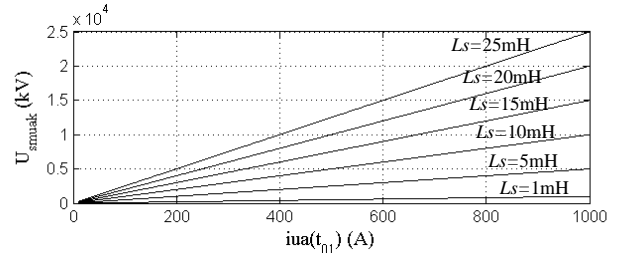


Fig. 3. Voltage  $u_{smua\_k}$  under various  $L_s$  and  $i_{ua}(t_{01})$ .

### B. Type II Fault Situation

Fig. 2(b) shows the Type II fault situation, where the open-circuit fault occurs in the bottom diode  $d_b$ . Tables II and III shows the four modes of the SM under the Type II fault. The SM works as normal in modes 1~3. In mode 1 ( $i_{ua} \geq 0$  and  $S=1$ ),  $i_{ua}$  circulates through  $d_t$  and  $C_{sm}$  with  $u_t = 0$ ,  $u_b = u_c$ ; in mode 2 ( $i_{ua} \geq 0$  and  $S=0$ ),  $i_{ua}$  circulates through  $T_b$  with  $u_t = u_c$ ,  $u_b = 0$ ; in mode 3 ( $i_{ua} < 0$  and  $S=1$ ),  $i_{ua}$  circulates through  $C_{sm}$  and  $T_t$  with  $u_t = 0$ ,  $u_b = u_c$ . However, in mode 4,  $i_{ua}$  can not flow through the faulty  $d_b$  when  $S$  is changed to 0 under  $i_{ua} < 0$ .

In mode 4, the voltage in phase A can be described as (11) at the initial time  $t_{02}$  when  $S$  is changed to 0.

$$V_{dc} = \sum_{i=1}^n u_{smua\_i}(t_{02}) + \sum_{i=1}^n u_{smla\_i}(t_{02}) + u_{ula}(t_{02}) + u_{lla}(t_{02}) \quad (11)$$

Suppose that  $i_{ua}$  can be blocked by switching off  $T_t$  in the  $k$ -th SM when  $S$  is changed to 0 into mode 4, a high voltage  $u_{ula}$  would be caused on the upper arm inductor of phase A after the IGBT turn-off time  $\Delta t$ , as

$$u_{ula}(t_{\Delta t 2}) = L_s \frac{i_{ua}(t_{02})}{\Delta t} \quad (12)$$

where  $i_{ua}(t_{02})$  is the upper arm current at the time  $t_{02}$ . According to KVL [35], the voltage  $u_{smua\_k}$  imposed on the  $k$ -th SM is

$$u_{smua\_k}(t_{\Delta t 2}) = V_{dc} - \sum_{i=1}^{k-1} u_{smua\_i}(t_{\Delta t 2}) - \sum_{i=k+1}^n u_{smua\_i}(t_{\Delta t 2}) - \sum_{i=1}^n u_{smla\_i}(t_{\Delta t 2}) - u_{ula}(t_{\Delta t 2}) - u_{lla}(t_{\Delta t 2}) \quad (13)$$

Except for the  $k$ -th SM output voltage  $u_{smua\_k}$ , assuming that the other SM output voltages and the lower arm inductor voltage  $u_{lla}$  in phase A are not changed during the very short time  $\Delta t$ , substituting (11) and (12) into (13), there is

$$u_{smua\_k}(t_{\Delta t 2}) = -L_s \frac{i_{ua}(t_{02})}{\Delta t} + u_{smua\_k}(t_{02}) + u_{ula}(t_{02}) \quad (14)$$

According to (14) and neglecting  $u_{smua\_k}(t_{02})$  and  $u_{ula}(t_{02})$ , Fig. 4 shows the caused high voltage  $u_{smua\_k}$  under various  $L_s$  and  $i_{ua}(t_{02})$ . It can be observed that  $u_{smua\_k}$  may reach a very high reverse voltage if the arm current can be blocked by the IGBT under faults. Actually, the voltage  $u_{smua\_k}$  could not reach a very high value under faults because the faulty SM is already destroyed before  $u_{smua\_k}$  increases to such a high value. Consequently, in mode 4, the high voltage  $u_t$  and  $u_b$  may be caused in the faulty SM with the voltage relationship shown in (10), where  $u_t > |u_b|$  and  $u_b < 0$ , as listed in Table III. From (10) and (14), it can be seen that a high voltage  $u_t$  and a high reverse voltage  $-u_b$  would be caused in the faulty SM in mode 4 and may destroy the MMC.

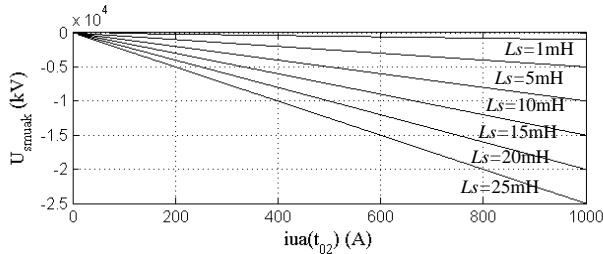


Fig. 4. Voltage  $u_{smua\_k}$  under various  $L_s$  and  $i_{ua}(t_{02})$ .

#### IV. PROPOSED PROTECTION SCHEME FOR MMCs UNDER DIODE OPEN-CIRCUIT FAULTS

In order to protect the MMC under diode open-circuit faults, two identical varistors ( $VR_t$  and  $VR_b$ ) are used to be equipped in parallel with  $T_t$  and  $T_b$  in each SM, respectively, as shown in Fig. 5. At low voltage the varistor has a very high resistance; at high voltage the varistor has a very low resistance [36]. The threshold voltage of the varistor is decided based on the parameters of the devices (e.g. switches, diodes, and capacitors) and the required tolerance level, which can be selected based on the rated capacitor voltage in the SM with a proper margin. If the SM works at normal situation, where the voltage  $u_t$  or  $u_b$  shown in Fig. 5 is not over the threshold voltage of the varistor, the varistor will be highly resistant. If  $u_t$  or  $u_b$  is above the threshold value of the varistor under faults, the varistor would be highly conductive to limit the voltage

and protect the MMC.

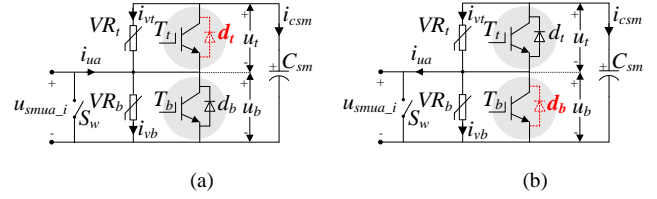


Fig. 5. Proposed protection. (a) Type I fault situation. (b) Type II fault situation.

##### A. Protection Scheme for Type I Fault Situation

Fig. 5(a) shows the Type I fault situation, where the Type I fault mainly affects the mode 1. A protection scheme, as shown in Fig. 6(a), is proposed for the Type I fault as follows.

1) Step 1 shown in Fig. 7(a): In mode 1 ( $i_{ua} \geq 0$  and  $S=1$ ), the arm current  $i_{ua}$  can not flow through the open-circuit  $d_t$  and  $C_{sm}$ , which would cause the high voltage  $u_b$  ( $u_b > |u_t|$ ) and the reverse voltage  $u_t$  ( $u_t < 0$ ). However, with the help of the varistor, when  $u_b$  is over the threshold voltage of the  $VR_b$ ,  $VR_b$  would be conducted to limit  $u_b$ , which makes  $i_{ua}$  flow through  $VR_b$ . Normally, the threshold voltage of the  $VR_b$  is selected higher than the capacitor voltage  $u_c$ , which results in negative  $u_t$  as

$$\begin{cases} u_t < 0 \\ u_b > u_c \end{cases} \quad (15)$$

Combining (15) and Table III, the fault can be detected when  $u_t$  is less than 0, where the  $u_t$  is monitored [37] and compared with the reference value 0.

2) Step 2 shown in Fig. 7(b): After the fault is detected,  $T_t$  and  $T_b$  start to be switched off and on, respectively. When  $T_b$  is switched on,  $i_{ua}$  flows through  $T_b$  and the SM voltage is

$$\begin{cases} u_t = u_c \\ u_b = 0 \end{cases} \quad (16)$$

Here, the  $VR_b$  will stop working because  $u_b=0$  is less than its threshold voltage.

The varistor's capacity is determined by its action time and conduction current, as listed in Table IV. As shown in Fig. 7, the  $VR_b$  only works during the fault detection time of Step 1 and the  $T_b$  switching on time of Step 2, which is normally very short and around the order of  $\mu s$ . The maximum conduction current of the  $VR_b$  is the peak value of the arm current  $i_{ua}$ . The selection of the varistor  $VR_b$  is discussed in the Appendix.

TABLE IV  
PARAMETERS FOR SELECTION OF VARISTOR'S CAPACITY

Fault	Action varistor	Action time of the varistor		Maximum conduction current
		Step 1	Step 2	
Type I	$VR_b$	Fault detecting time	Switching on time of $T_b$	Peak value of the arm current
Type II	$VR_t$	Fault detecting time	Switching on time of $T_t$	

3) Step 3 shown in Fig. 7(c): After  $T_b$  is switched on, the  $S_w$  starts to be closed to bypass the faulty SM.

4) Step 4 shown in Fig. 7(d): After the  $S_w$  is closed,  $T_b$  starts to be switched off.

In the proposed protection scheme, if the varistor is

neglected,  $u_t$  may be increased to a very high value in less than  $1 \mu s$  in Step 1. However, the  $T_b$  is not fast enough to be switched on in such a short time to limit the  $u_t$  in Step 2. Therefore, the varistor is used here, which can limit the voltage with the fast response time around the order of  $ns$  [36] in Step 1. In addition, the varistor is very cheap, as shown in the Appendix.

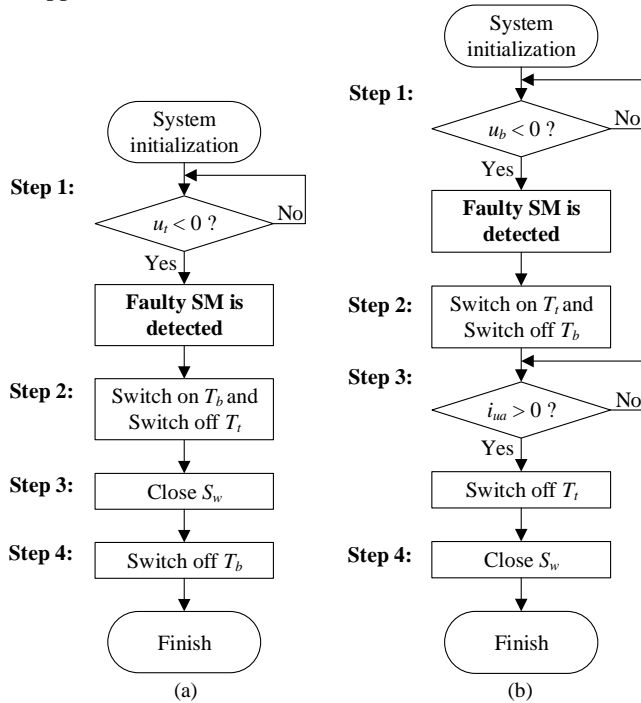


Fig. 6. Proposed protection scheme for (a) Type I fault situation. (b) Type II fault situation.

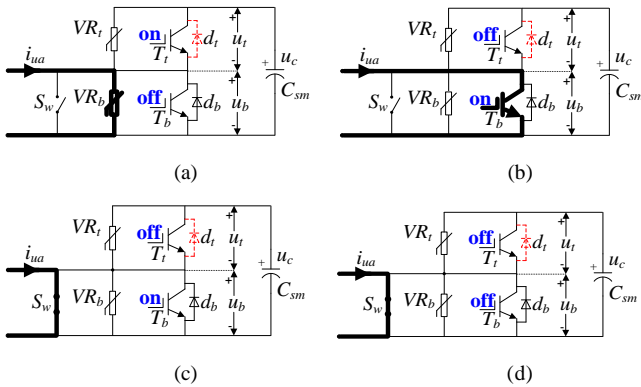


Fig. 7. Protection scheme for Type I fault. (a) Step 1. (b) Step 2. (c) Step 3. (d) Step 4.

### B. Protection Scheme for Type II Fault Situation

Fig. 5(b) shows the Type II fault situation, where the Type II fault mainly affects the mode 4. A protection scheme, as shown in Fig. 6(b), is proposed for the Type II fault as follows.

1) Step 1 shown in Fig. 8(a): In mode 4 ( $i_{ua} < 0$  and  $S=0$ ),  $i_{ua}$  can not flow through the open-circuit  $d_b$ , which would cause the high voltage  $u_t$  ( $u_t > |u_b|$ ) and the reverse voltage  $u_b$  ( $u_b < 0$ ). However, with the help of the  $VR_t$ , when  $u_t$  is over the threshold voltage of the  $VR_t$ ,  $VR_t$  would be conducted to limit  $u_t$ , which makes  $i_{ua}$  flow through  $C_{sm}$  and  $VR_t$ . Normally, the threshold voltage of the  $VR_t$  is selected higher than the capacitor voltage  $u_c$ , which results in negative  $u_b$  as

$$\begin{cases} u_t > u_c \\ u_b < 0 \end{cases} \quad (17)$$

Combining (17) and Table III, the fault can be detected when  $u_b$  is less than 0.

2) Step 2 shown in Fig. 8(b): After the faulty SM is detected,  $T_t$  and  $T_b$  start to be switched on and off, respectively. When  $T_t$  is switched on,  $i_{ua}$  flows through  $C_{sm}$  and  $T_t$  and the SM voltage is

$$\begin{cases} u_t = 0 \\ u_b = u_c \end{cases} \quad (18)$$

Here, the  $VR_t$  will stop working because  $u_t=0$  is less than its threshold voltage. As shown in Fig. 8, the  $VR_t$  only works during the fault detection time of Step 1 and the  $T_t$  switching on time of Step 2, as shown in Table IV, which is very short around the order of  $\mu s$ . The selection of the varistor  $VR_t$  can refer to that of  $VR_b$ , which is not repeated here.

3) Step 3 shown in Fig. 8(c): After  $T_t$  is switched on, the bypass switch  $S_w$  can not be closed immediately. Otherwise, it would result in short circuit, where  $C_{sm}$  discharges through  $T_t$  and  $S_w$ . Therefore,  $T_t$  would be switched off until  $i_{ua}$  becomes positive. In this situation,  $i_{ua}$  will flow through  $d_t$  and  $C_{sm}$ .

4) Step 4 shown in Fig. 8(d): After  $T_t$  is switched off, the  $S_w$  starts to be closed to bypass the faulty SM.

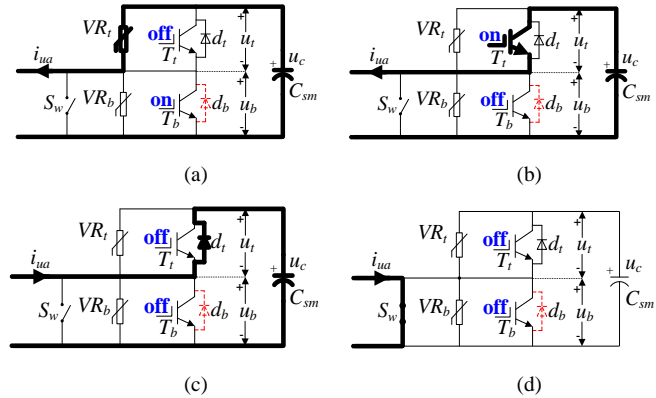


Fig. 8. Protection scheme for Type II fault. (a) Step 1. (b) Step 2. (c) Step 3. (d) Step 4.

## V. EXPERIMENTAL STUDIES

A three-phase MMC prototype with four SMs per arm, as shown in Fig. 1, connected with three-phase RL load is built in the laboratory to confirm the proposed scheme. Fig. 9 shows the photo of the experimental setup. A DC power supply (SM 600-10) is used to support the DC-link voltage. Except for Cell21, the IXFK48N60P with intrinsic diode is used as the switch/diode in each cell. In order to produce the diode open-circuit fault, the IGBT IGW50N60H3 without intrinsic diode and the fast recovery Diode STTH3006 are used to construct the switch/diode in the Cell21, where the diode open-circuit fault is produced by the disconnection of the diode with the circuit. In addition, two IXFK48N60Ps are connected in series with opposite direction to simulate a controllable bypass switch. The system control algorithm is implemented in dSPACE and the pulse signals from the dSPACE are

transferred to the driving panel of each SM by optical fiber. The system parameters are shown in the Table V. The capacitor voltage-balancing method [27] and the circulating current elimination method [30] are used.

TABLE V  
EXPERIMENTAL SYSTEM PARAMETERS

Parameters	Value
DC-link voltage $V_{dc}$ in the case without protective varistor (V)	80
DC-link voltage $V_{dc}$ in the case with protective varistor (V)	280
Rated frequency (Hz)	50
Inductance $L_s$ (mH)	3
DC capacitor $C_{sm}$ (mF)	2.2
Load inductance $L$ (mH)	3.6
Load resistance $R$ in the case without protection ( $\Omega$ )	5.3
Load resistance $R$ in the case with protection ( $\Omega$ )	10
Switching frequency (kHz)	4
Varistor	S14K35

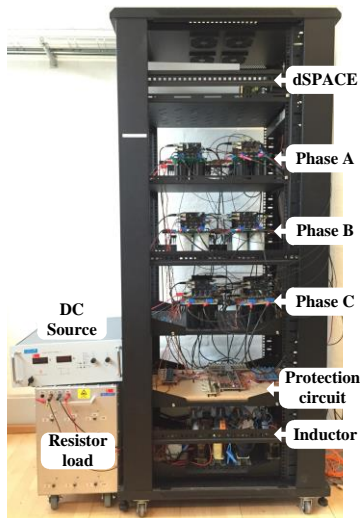


Fig. 9. Photo of the experimental setup.

### A. Without Proposed Protection Scheme

#### 1) Type I fault in Cell21

Fig. 10(a) shows the performance of the MMC without the proposed protection scheme, where the Type I fault occurred in Cell21. Fig. 10(a) shows the lower arm current  $i_{la}$ , capacitor voltage  $u_{cal\_1}$ , top IGBT voltage  $u_{t1}$ , and bottom IGBT voltage  $u_{b1}$  in Cell21. Owing to the Type I fault, a high reverse voltage  $u_{t1}$  is caused when  $i_{la} \geq 0$ , whose maximum value is about 10.5 times higher than the nominal capacitor voltage  $u_{cal\_1}$ ; a high voltage  $u_{b1}$  is also caused when  $i_{la} \geq 0$ , whose maximum value is about 11.5 times higher than the nominal capacitor voltage  $u_{cal\_1}$ . The caused high voltage would be harmful to the MMC.

Fig. 10(b) shows the dotted line area in Fig. 10(a). Owing to the Type I fault, a high reverse voltage  $u_{t1}$  is caused and imposed on the top IGBT, which is the same to the theoretical analysis. Once the caused reverse voltage  $u_{t1}$  is high enough and beyond the reverse blocking capability of the IGBT, it will result in reverse conduction of the top IGBT [32]. Consequently, the arm current  $i_{la}$  is not interrupted under faults.

#### 2) Type II fault in Cell21

Fig. 11(a) shows the performance of the MMC without the proposed protection scheme, where the Type II fault occurred in Cell21. Fig. 11(a) shows the arm current  $i_{la}$ , capacitor

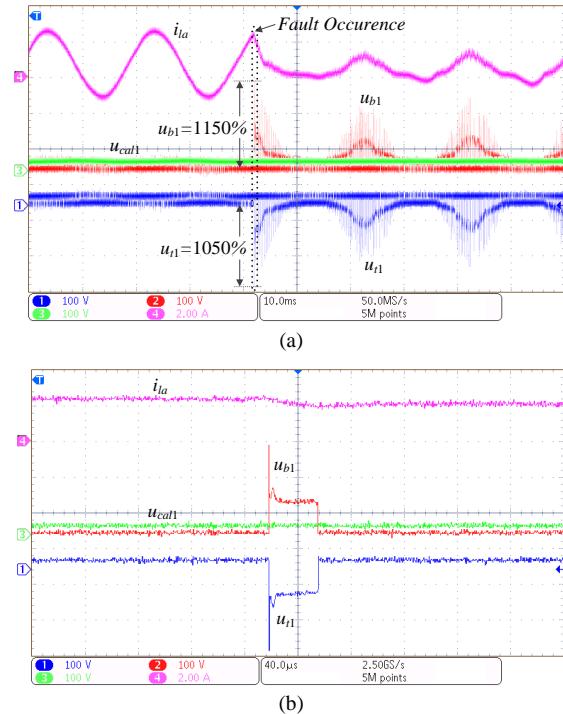


Fig. 10. Experiment waveforms including arm current  $i_{la}$  (2 A/div), top IGBT voltage  $u_{t1}$  (100 V/div), bottom IGBT voltage  $u_{b1}$  (100 V/div), and capacitor voltage  $u_{cal\_1}$  (100 V/div). (a) Type I fault. Time base is 10 ms/div. (b) Type I fault in small time scale. Time base is 40  $\mu$ s/div.

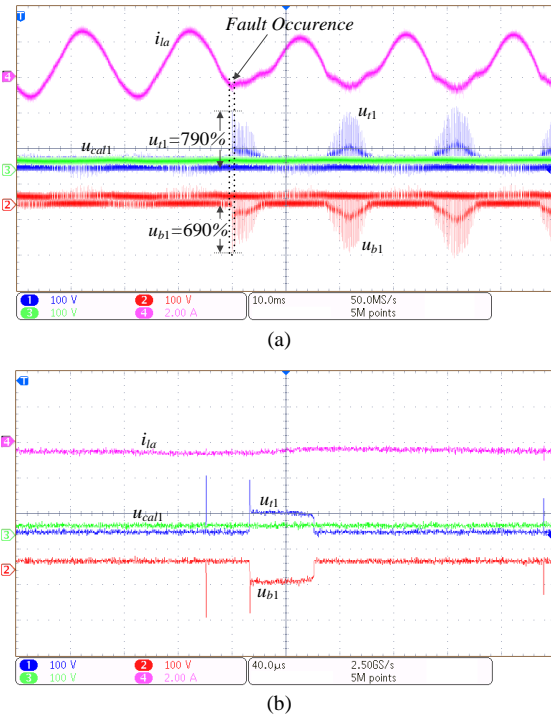


Fig. 11. Experiment waveforms including arm current  $i_{la}$  (2 A/div), top IGBT voltage  $u_{t1}$  (100 V/div), bottom IGBT voltage  $u_{b1}$  (100 V/div), and capacitor voltage  $u_{cal\_1}$  (100 V/div). (a) Type II fault. Time base is 10 ms/div. (b) Type II fault in small time scale. Time base is 40  $\mu$ s/div.

voltage  $u_{cal\_1}$ , top IGBT voltage  $u_{t1}$ , and bottom IGBT voltage  $u_{b1}$  in Cell21. Owing to the Type II fault, a high reverse voltage  $u_{b1}$  is caused when  $i_{la} < 0$ , whose maximum value is about 6.9 times higher than the nominal capacitor voltage  $u_{cal\_1}$ ;

a high voltage  $u_{t1}$  is also caused when  $i_{la} \geq 0$ , whose maximum value is about 7.9 times higher than the nominal capacitor voltage  $u_{cal\_1}$ . The caused high voltage is harmful to the MMC.

Fig. 11(b) shows the dotted line area in Fig. 11(a). Owing to the Type II fault, a high reverse voltage  $u_{b1}$  is caused and imposed on the bottom IGBT. Once the caused reverse voltage  $u_{b1}$  is high enough and beyond the reverse blocking capability of the IGBT, it will result in reverse conduction of the bottom IGBT [32]. Consequently, the arm current  $i_{la}$  is not interrupted under faults.

### B. Without Varistors

#### 1) Type I fault in Cell21

Fig. 12 shows the performance of the MMC with the proposed protection scheme shown in Fig. 6(a), where the Type I fault occurred in Cell21. However, the protective varistors are not used in Fig. 12. Fig. 12(a) shows the lower arm current  $i_{la}$ , capacitor voltage  $u_{cal\_1}$ , top IGBT voltage  $u_{t1}$ , and bottom IGBT voltage  $u_{b1}$  in Cell21. Fig. 12(b) shows the dotted line area in Fig. 12(a). Although the bottom IGBT  $T_b$  starts to be switched on once the fault is detected, the  $T_b$  is not fast enough to avoid the high voltage, which is the same to the theoretical analysis. Consequently, a high reverse voltage  $u_{t1}$  is caused when  $i_{la} \geq 0$ , whose maximum value is about 10.5 times higher than the nominal capacitor voltage  $u_{cal\_1}$ ; a high voltage  $u_{b1}$  is also caused when  $i_{la} \geq 0$ , whose maximum value is about 11.5 times higher than the nominal capacitor voltage  $u_{cal\_1}$ . The caused high voltage is harmful to the MMC.

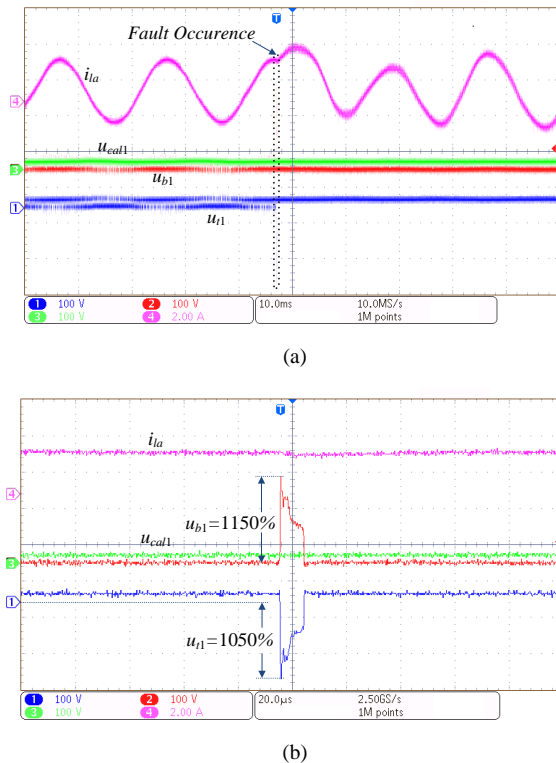


Fig. 12. Experiment waveforms including arm current  $i_{la}$  (2 A/div), top IGBT voltage  $u_{t1}$  (100 V/div), bottom IGBT voltage  $u_{b1}$  (100 V/div), and capacitor voltage  $u_{cal\_1}$  (100 V/div). (a) Type I fault. Time base is 10 ms/div. (b) Type I fault in small time scale. Time base is 20  $\mu$ s/div.

#### 2) Type II fault in Cell21

Fig. 13 shows the performance of the MMC with the proposed protection scheme shown in Fig. 6(b), where the Type II fault occurred in Cell21. However, the protective varistors are not used in Fig. 13. Fig. 13(a) shows the lower arm current  $i_{la}$ , capacitor voltage  $u_{cal\_1}$ , top IGBT voltage  $u_{t1}$ , and bottom IGBT voltage  $u_{b1}$  in Cell21. Fig. 13(b) shows the dotted line area in Fig. 13(a). Although the top IGBT  $T_t$  starts to be switched on once the fault is detected, the  $T_t$  is not fast enough to avoid the high voltage, which is the same to the theoretical analysis. Consequently, a high reverse voltage  $u_{b1}$  is caused when  $i_{la} < 0$ , whose maximum value is about 7.7 times higher than the nominal capacitor voltage  $u_{cal\_1}$ ; a high voltage  $u_{t1}$  is also caused when  $i_{la} < 0$ , whose maximum value is about 8.7 times higher than the nominal capacitor voltage  $u_{cal\_1}$ . The caused high voltage is harmful to the MMC.

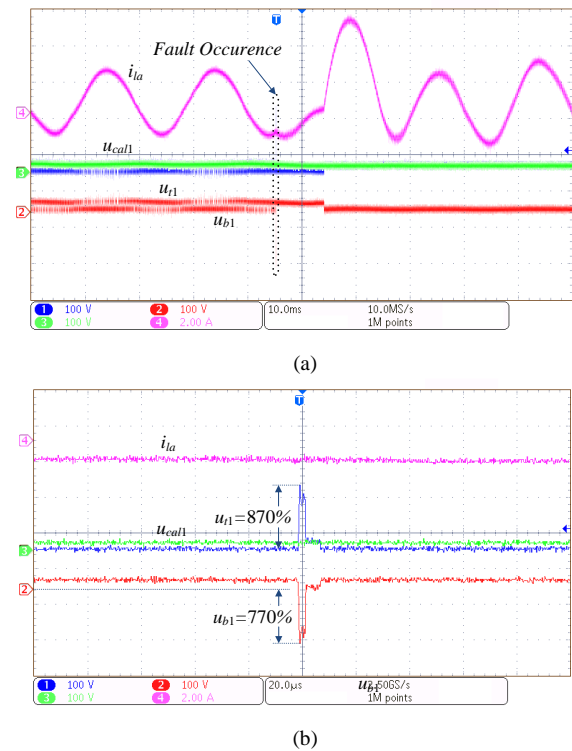


Fig. 13. Experiment waveforms including arm current  $i_{la}$  (2 A/div), top IGBT voltage  $u_{t1}$  (100 V/div), bottom IGBT voltage  $u_{b1}$  (100 V/div), and capacitor voltage  $u_{cal\_1}$  (100 V/div). (a) Type II fault. Time base is 10 ms/div. (b) Type II fault in small time scale. Time base is 20  $\mu$ s/div.

### C. With Proposed Protection Scheme

#### 1) Type I fault in Cell21

Fig. 14 shows the performance of the MMC with the proposed protection scheme, where the Type I fault occurred in Cell21. Fig. 14(a) shows the arm current  $i_{la}$ , capacitor voltage  $u_{cal\_1}$ , top IGBT voltage  $u_{t1}$  and bottom IGBT voltage  $u_{b1}$  in Cell21. Fig. 14(b) shows the dotted line area in Fig. 14(a). The fault can be detected when the top IGBT voltage  $u_{t1}$  drops below zero. With the help of the varistor, the  $u_{b1}$  is effectively limited and only increased a little by 20%. After the fault is detected, the top IGBT  $T_t$  and bottom IGBT  $T_b$  starts to be switched off and on, respectively. And then, the bypass switch is switched on to bypass the faulty SM. Consequently,

the  $u_{t1}$  is the capacitor voltage  $u_{cal\_1}$  and  $u_{b1}$  is 0 after faults.

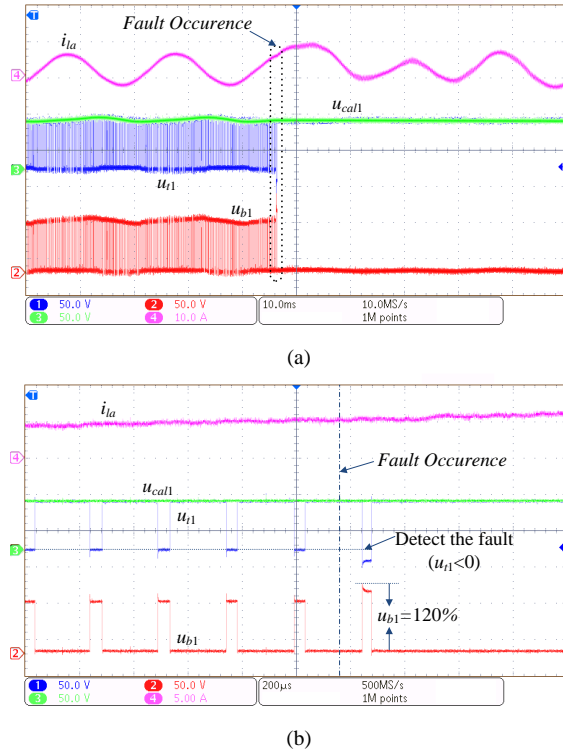


Fig. 14. Experiment waveforms including arm current  $i_{la}$  (10 A/div), top IGBT voltage  $u_{t1}$  (50 V/div), bottom IGBT voltage  $u_{b1}$  (50 V/div), and capacitor voltage  $u_{cal\_1}$  (50 V/div). (a) Type I fault. Time base is 10 ms/div. (b) Type I fault in small time scale. Time base is 200  $\mu$ s/div.

Fig. 15 shows the Cell21 performance with the proposed scheme including the top IGBT voltage  $u_{t1}$ , bottom IGBT voltage  $u_{b1}$ , top varistor  $VR_t$  current  $i_{vt1}$ , and bottom varistor  $VR_b$  current  $i_{vb1}$ . After the Type I fault occurrence, the bottom IGBT voltage  $u_{b1}$  is effectively limited by the bottom varistor, when  $u_{b1}$  is over the threshold value of the varistor. The varistor only works with a very short time about 39  $\mu$ s.

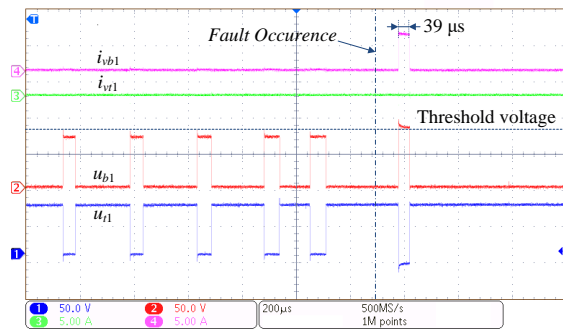


Fig. 15. Experiment waveforms including top IGBT voltage  $u_{t1}$  (50 V/div), bottom IGBT voltage  $u_{b1}$  (50 V/div), top varistor current  $i_{vt1}$  (5 A/div) and bottom varistor current  $i_{vb1}$  (5 A/div). Time base is 200 $\mu$ s/div.

Fig. 16 shows the Cell21 performance with the proposed scheme including the top IGBT drive signal  $g_{t1}$ , bottom IGBT drive signal  $g_{b1}$ , bottom varistor  $VR_b$  current  $i_{vb1}$ , and the action of the bypass switch  $S_w$ . After the Type I fault occurrence, the  $VR_b$  works in a short time to limit the voltage;  $g_{t1}$  and  $g_{b1}$  start to turn off and on the top and bottom IGBTs, respectively. Afterwards, the bypass switch  $S_w$  starts to bypass the faulty SM and the bottom IGBT is blocked with  $g_{b1}$  off.

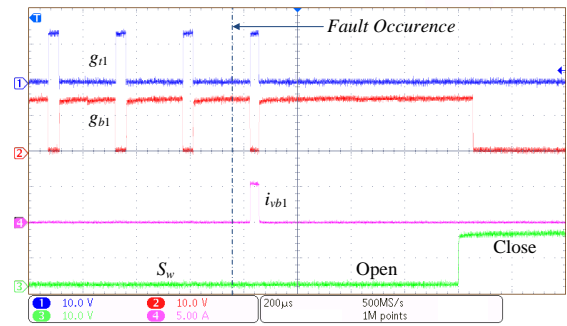


Fig. 16. Experiment waveforms including top IGBT drive signal  $g_{t1}$  (10 V/div), bottom IGBT drive signal  $g_{b1}$  (10 V/div), bottom varistor current  $i_{vb1}$  (5 A/div), and bypass switch action. Time base is 200  $\mu$ s/div.

## 2) Type II fault in Cell21

Fig. 17 shows the performance of the MMC with the proposed protection scheme, where the Type II fault occurred in Cell21. Fig. 17(a) shows the arm current  $i_{la}$ , capacitor voltage  $u_{cal\_1}$ , top IGBT voltage  $u_{t1}$  and bottom IGBT voltage  $u_{b1}$  in Cell21. Fig. 17(b) shows the dotted line area in Fig. 17(a). The fault can be detected when the bottom IGBT voltage  $u_{b1}$  drops below zero. The  $u_{t1}$  is effectively limited by the varistor and only increased a little by 20%. After the fault is detected, the top IGBT  $T_t$  and bottom IGBT  $T_b$  starts to be switched on and off, respectively, which results in that  $u_{t1}$  is 0 and  $u_{b1}$  is the capacitor voltage  $u_{cal\_1}$ . Afterwards, the top IGBT  $T_t$  starts to be opened when  $i_{la}$  becomes positive; the bypass switch is switched on to bypass the faulty SM, which results in that  $u_{t1}$  equals the capacitor voltage  $u_{cal\_1}$  and  $u_{b1}$  equals 0.

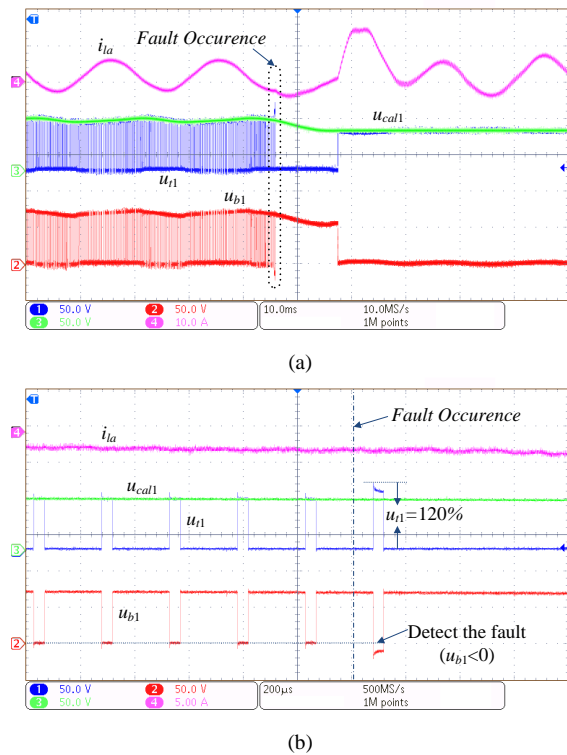


Fig. 17. Experiment waveforms including arm current  $i_{la}$  (10 A/div), top IGBT voltage  $u_{t1}$  (50 V/div), bottom IGBT voltage  $u_{b1}$  (50 V/div), and capacitor voltage  $u_{cal\_1}$  (50 V/div). (a) Type I fault. Time base is 10 ms/div. (b) Type I fault in small time scale. Time base is 200  $\mu$ s/div.

Fig. 18 shows the Cell21 performance with the proposed scheme including the top IGBT voltage  $u_{t1}$ , bottom IGBT voltage  $u_{b1}$ , top varistor current  $i_{vt1}$ , and bottom varistor current  $i_{vb1}$ . After the Type II fault occurrence, the top IGBT voltage  $u_{t1}$  is effectively limited by the varistor, when  $u_{t1}$  is over the threshold value of the varistor. The varistor only works with a very short time about 37  $\mu$ s.

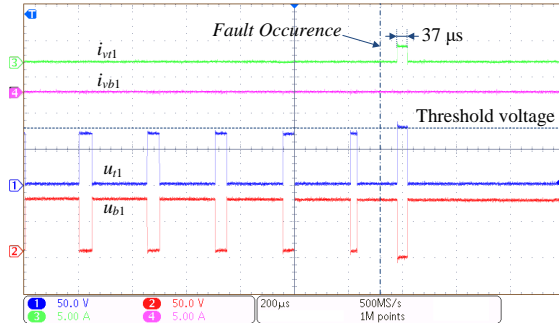


Fig. 18. Experiment waveforms including top IGBT voltage  $u_{t1}$  (50 V/div), bottom IGBT voltage  $u_{b1}$  (50 V/div), top varistor current  $i_{vt1}$  (5 A/div), and bottom varistor current  $i_{vb1}$  (5 A/div). Time base is 200  $\mu$ s/div.

Fig. 19 shows the Cell21 performance with the proposed scheme including the top IGBT drive signal  $g_{t1}$ , bottom IGBT drive signal  $g_{b1}$ , arm current  $i_{la}$ , and the action of the bypass switch  $S_w$ . After the Type II fault occurrence,  $g_{t1}$  and  $g_{b1}$  start to turn on and off the top and bottom IGBT, respectively. Afterwards,  $g_{t1}$  start to turn off the top IGBT when  $i_{la}$  becomes positive. And then,  $S_w$  is switched on to bypass the faulty SM.

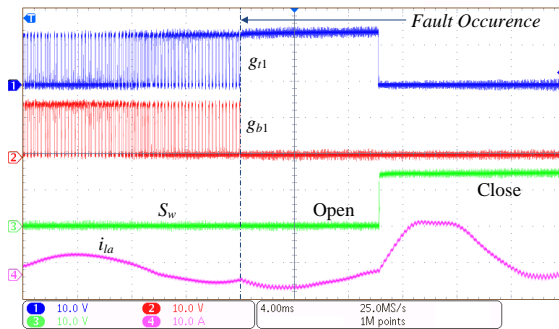


Fig. 19. Experiment waveforms including top IGBT drive signal  $g_{t1}$  (10 V/div), bottom IGBT drive signal  $g_{b1}$  (10 V/div), bottom varistor current  $i_{vb1}$  (5 A/div), and bypass switch action. Time base is 4 ms/div.

## VI. CONCLUSIONS

Reliability is one of the primary concerns for the modular multilevel converter. This paper proposed a protection scheme for the MMC under diode open-circuit faults. The impact of diode open-circuit failures of the SMs on the operation of the MMC is analyzed to reveal that the diode open-circuit fault would cause the high voltage in the faulty SM, which would destroy the MMC and disrupt the operation of the MMC. A protection scheme based on the varistor is proposed for the MMC under diode open-circuit faults, which can effectively limit the voltage, detect the fault, and protect the MMC. A downscale prototype is tested in the laboratory to validate the proposed protection scheme, and the results show the effectiveness of the proposed protection scheme.

## VII. APPENDIX

The MMC system [38], as shown in Table VI, is considered as an example for the selection of the protective varistor. The varistor VDRS14T510 [39] can be selected for the MMC system, whose threshold voltage is 820 V, which is 1.24 times of the peak value of capacitor voltage in the SM. The maximum conduction current of the varistor is the peak value of the arm current, as 192 A. According to the pulse rating curve of the varistor VDRS14T510, as shown in Fig. 20, the VDRS14T510 is able to withstand the conduction current 192 A for more than 400  $\mu$ s, which fully meets the capacity's requirement of the varistor, because the varistor only works for a very short time and around the order of tens of  $\mu$ s, as shown in Figs. 15 and 18 in Section V. As to the MMC system, the Infineon IGBT FF300R12KT4 can be used, whose price is 113.49  $\text{\textsterling}$  [40], while the price of the varistor VDRS14T510 is 0.971  $\text{\textsterling}$  and less than 0.9% of the IGBT [41]. The cost increase because of the varistor is therefore negligible in this application, while the varistor can effectively avoid the destruction and protect the MMC under the diode open-circuit fault.

TABLE VI  
MMC SYSTEM PARAMETERS [38]

Parameters	Value
Active power $P$ (MW)	1
Reactive power $Q$ (MVar)	0.16
DC bus voltage $V_{dc}$ (kV)	6
Output line-to-line voltage (kV)	3
Number of SMs per arm $n$	10
Rated capacitor voltage $u_c$ (V)	600
Peak value of capacitor voltage (V)	660
Peak value of arm current (A)	192
DC capacitor $C_{sm}$ (mF)	3.75
Inductance $L_s$ (mH)	10
IGBT	FF300R12KT4
Price of per FF300R12KT4 ( $\text{\textsterling}$ )	113.49

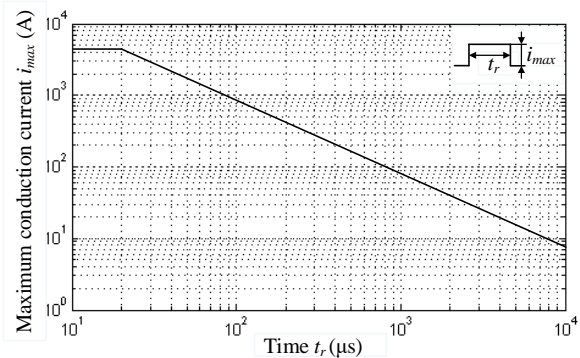


Fig. 20. Pulse rating curve of the varistor.

## REFERENCES

- [1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.
- [2] S. Debnath, J. Qin, B. Bahrani, M. Saedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: a review," *IEEE Trans. Power Electron.*, vol.30, no. 1, pp. 37-53, Jan. 2015.
- [3] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular

- multilevel converters," *IEEE Trans. Power. Electron.*, vol. 30, no. 1, pp. 4-17, Jan. 2015.
- [4] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Cárca, and L. Zajac, "Modular multilevel converter with different submodule concepts-Part I: Capacitor voltage balancing method," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4525-4535, October 2013
- [5] M. Guan and Z. Xu, "Modeling and control of a modular multilevel converter-based HVDC system under unbalanced grid conditions," *IEEE Trans. Power Electron.*, vol. 27, no. 12, pp. 4858-4867, Dec. 2012.
- [6] E. Solas, G. Abad, J. Barrena, S. Aurtenetxea, A. Cárca, and L. Zajac, "Modular multilevel converter with different submodule concepts-Part II: Experimental validation and comparison for HVDC application," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4536-4545, Oct. 2013.
- [7] G. Bergna, E. Berne, P. Egrot, P. Lefranc, A. Arzandé J. Vannier, and M. Molinas, "An energy-based controller for HVDC modular multilevel converter in decoupled double synchronous reference frame for voltage oscillation reduction," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2360-2371, Jun. 2013.
- [8] S. Du, B. Wu, N. Zargari, and Z. Cheng, "A flying-capacitor modular multilevel converter for medium-voltage motor drive," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2081-2089, Mar. 2017.
- [9] Y. Okazaki, W. Kawamura, M. Hagiwara, H. Akagi, T. Ishida, M. Tsukakoshi, and R. Nakamura, "Experimental comparisons between modular multilevel DSCC inverters and TSBC converters for medium-voltage motor drives," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1805-1817, Mar. 2017.
- [10] Q. Xu, F. Ma, Z. He, Y. Chen, J. Guerrero, A. Luo, Y. Li, and Y. Yue, "Analysis and comparison of modular railway power conditioner for high-speed railway traction system," *IEEE Trans. Power Electron.*, accepted, 2016.
- [11] B. Gemell, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel VSC technologies for power transmission," in *Proc. IEEE PES T&D Conf. and Exp.*, 2008, pp. 1-16.
- [12] B. Li, S. Shi, B. Wang, G. Wang, W. Wang, and D. Xu, "Fault diagnosis and tolerant control of single IGBT open-circuit failure in modular multilevel converters," *IEEE Trans. Power Electron.*, Accepted, 2015.
- [13] F. Richardeau and T. Pham, "Reliability calculation of multilevel converters: theory and applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4225-4233, Oct. 2013.
- [14] H. Liu, P. C. Loh, and F. Blaabjerg, "Review of fault diagnosis and fault-tolerant control for modular multilevel converter of HVDC," in *Proc. IECON*, 2013, pp. 1242-1247.
- [15] S. Shao, P. Wheeler, J. Clare, and A. Watson, "Fault detection for modular multilevel converters based on sliding mode observer," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4867-4872, Nov. 2013.
- [16] F. Deng, Z. Chen, M. K. Rezwani, and R. Zhu, "Fault detection and localization method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2721-2732, May, 2015.
- [17] A. Ghazanfari and Y. A-R I. Mohamed, "A resilient framework for fault-tolerant operation of modular multilevel converters," *IEEE Trans. Ind. Electron.*, accepted, 2015.
- [18] Q. Yang, J. Qin, and M. Saadifard, "Analysis, detection, and location of open-switch submodule failures in a modular multilevel converter," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 155-164, Feb. 2016.
- [19] U.-M. Choi, F. Blaabjerg, and K.-B. Lee, "Study and handling methods of power IGBT module failures in power electronic converter systems," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2517-2533, May 2015
- [20] H. Oh, B. Han, P. McCluskey, C. Han, and B. Youn, "Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2413-2426, May 2015.
- [21] B. Mirafzal, "Survey of fault-tolerance techniques for three-phase voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5192-5202, Oct. 2014.
- [22] N. Freire, J. Estima, and A. Marques Cardoso, "Open-circuit fault diagnosis in PMSG drives for wind turbine applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3957-3967, Sep. 2013.
- [23] R. Picas, J. Zaragoza, J. Pou, and S. Ceballos, "Reliable modular multilevel converter fault detection with redundant voltage sensor," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 39-51, Jan. 2017.
- [24] R. Wu, F. Blaabjerg, H. Wang, and M. Liserre, "Overview of catastrophic failures of freewheeling diodes in power electronic circuits," *Microelectron. Reliab.*, vol. 53, no. 9-11, 2013, pp. 1788-1792.
- [25] T. Basler, M. Pfaffenlehner, H. Felsl, F. Niedernostheide, F. Pfirsch, H. Schulze, R. Baburske, and J. Lutz, "Switching ruggedness and surge-current capability of diodes using the self-adjusting p emitter efficiency diode concept," *IET Circuits, Devices Syst.*, vol. 8, no. 3, pp. 205-212, Jun. 2014.
- [26] B. Heinze, J. Lutz, M. Neumeister, "Surge current ruggedness of silicon carbide schottky- and merged-pin-schottky diodes," in *Proc. ISPS*, 2008, pp. 245-248.
- [27] F. Deng and Z. Chen, "A control method for voltage balancing in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 66-76, Jan. 2014.
- [28] W. Li, L. Grégoire, and J. Bédanger, "A modular multilevel converter pulse generation and capacitor voltage balance method optimized for FPGA implementation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2859-2867, May 2015.
- [29] J. Pou, S. Ceballos, G. Konstantinou, V. G. Agelidis, R. Picas, and J. Zaragoza, "Circulating current injection methods based on instantaneous information for the modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 777-788, Feb. 2015.
- [30] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009-2017, Jul. 2011.
- [31] G. P. Adam, I. Abdelsalam, J. Fletcher, G. M. Burt, D. Holliday, and S. J. Finney, "New efficient submodule for a modular multilevel converter in multiterminal HVDC Networks," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4258-4278, Jun. 2017.
- [32] N. Mohan, T. M. Undeland, and W. P. P Robbins, *Power Electronics Converters, Applications, And Design*, Third Edition, New York: John Wiley & Sons, 2002, pp. 27.
- [33] K. Ilves, S. Norrga, L. Harnefors, and H. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Trans. Power. Electron.*, vol. 29, no. 1, pp. 77-88, Jan. 2014.
- [34] Z. Li, F. Gao, F. Xu, X. Ma, Z. Chu, P. Wang, R. Gou, and Y. Li, "Power modular capacitor voltage balancing method for a  $\pm 350$ -kV/1000-MW modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 3977-3984, Jun. 2016.
- [35] W. K. Chen, *The Electrical Engineering Handbook*, USA: Elsevier Academic Press, 2005, pp.6.
- [36] R. B. Standler, *Protection of Electronic Circuits From Overvoltages*, New York: John Wiley & Sons, 2002, pp. 134.
- [37] Y. Wang, P. P. Palmer, A. T. Bryant, S. J. Finney, M. S. Abu-Khaizaran, and G. Li, "An analysis of high-power IGBT switching under cascade active voltage control," *IEEE Trans. Ind. Appl.*, vol. 45, no. 2, pp. 861-870, Mar./Apr. 2009.
- [38] F. Deng and Z. Chen, "Voltage-balancing method for modular multilevel converters under phase-shifted carrier-based pulsewidth modulation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4158-4169, Jul. 2014.
- [39] VDRS Series, VISHAY, 2015. [Online]. Available: <http://www.mouser.com/ds/2/427/vdrs-101657.pdf>V\_Leaded\_StandarD.pdf
- [40] Mouser, 2017. [Online]. Available: <http://eu.mouser.com/ProductDetail/Infineon/FF300R12KT4/?qs=%2fha2pyFadugpDt5WSE0x3Jd2Cc5FQBIOZeMnWckc7VRy8sTOi477fg%3d%3d>
- [41] Mouser, 2017. [Online]. Available: <http://eu.mouser.com/ProductDetail/Vishay/VDRS14T510BSE/?qs=%2fha2pyFaduho8Fzj3MUUt%252b8KALtutsrSoWd%2fhuD%252bQ8U%3d>



**Fujin Deng** (S'10, M'13) received the B.Eng. degree in electrical engineering from China University of Mining and Technology, Jiangsu, China, in 2005, the M.Sc. Degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2008, and the Ph.D. degree in energy technology from the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2012.

He joined the Southeast University in 2017 and is currently a Professor in the School of Electrical Engineering, Southeast

University, Nanjing, China. From 2013 to 2015 and from 2015 to 2017, he was a Postdoctoral Researcher and an Assistant Professor, respectively, in the Department of Energy Technology, Aalborg University, Aalborg, Denmark. His main research interests include wind power generation, multilevel converters, high-voltage direct-current (HVDC) technology, DC grid, and offshore wind farm-power systems dynamics.



**Rongwu Zhu** (S'13) received the B.Eng. in Electrical Engineering from Nanjing Normal University, Nanjing, China, in 2007 and the Ph.D. degree in the Department of Energy Technology from Aalborg University, Aalborg, Denmark in 2015. From 2011-2012, he is a guest researcher with Aalborg University.

He is currently a Postdoctoral Researcher with Chair of Power Electronics, at Christian-Albrechts-University of Kiel (Germany). His research interests include high-power multilevel converters, nonlinear control, DC-grid and wind-farm power systems, smart-transformer-fed distribution generation system.



**Dong Liu** (S'15) received the B.Eng. degree and M.Sc. degree in electrical engineering from South China University of Technology, Guangdong, China, in 2008 and 2011 respectively. He is currently working toward the Ph.D. degree in the Department of Energy Technology, Aalborg University, Denmark.

From 2011 to 2014, he was a R&D Engineer in Emerson Network Power Co., Ltd., Shenzhen, China. His main research interests include renewable energy technology, multilevel converters, and DC/DC converters.



**Yanbo Wang** (S'15-M'17) received the M.S. degrees in electrical engineering in the Electrical Engineering School, Southwest Jiaotong University, Chengdu, China, in 2011. He is currently working toward the Ph.D degree in the department of Energy Technology, Aalborg University, Denmark.

His research interests include harmonic analysis and mitigation in power electronic-fed power system, distributed power generation system, microgrid, power system state estimation and stability analysis.



**Huai Wang** (M'12) received the B.E. degree in electrical engineering and its automation, from Huazhong University of Science and Technology, Wuhan, China, in 2007 and the Ph.D. degree in power electronics, from the City University of Hong Kong, Hong Kong, in 2012. He is currently an Associate Professor and a Research Thrust Leader in the Center of Reliable Power Electronics (CORPE), Aalborg University, Aalborg, Denmark. He was a Visiting Scientist with the ETH Zurich, Switzerland,

from Aug. to Sep. 2014, and with the Massachusetts Institute of Technology (MIT), USA, from Sep. to Nov. 2013. He was with the ABB Corporate Research Center, Switzerland, in 2009. His research addresses the fundamental challenges in modelling and validation of power electronic component failure mechanisms, and application issues in system-level predictability, condition monitoring, circuit architecture, and robustness design. He has contributed a few concept papers in the area of power electronics reliability, filed four patents on capacitive DC-link inventions, and co-edited a book.

Dr. Wang received the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society in 2016, and the Green Talents Award from the German Federal Ministry of Education and Research in 2014. He is currently the Award Chair of the Technical Committee of the High Performance and Emerging Technologies, IEEE Power Electronics Society. He serves as an Associate Editor of IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS and IEEE TRANSACTIONS ON POWER ELECTRONICS.



**Zhe Chen** (M'95-SM'98) received the B.Eng. and M.Sc. degrees all in Electrical Engineering from Northeast China Institute of Electric Power Engineering, Jilin City, China, MPhil in Power Electronic, from Staffordshire University, England and the Ph.D. degree in Power and Control, from University of Durham, England.

Dr Chen is a full Professor with the Department of Energy Technology, Aalborg University, Denmark. He is the leader of Wind Power System Research program at the Department of Energy Technology, Aalborg University and the Danish Principle Investigator for Wind Energy of Sino-Danish Centre for Education and Research.

His research areas are power systems, power electronics and electric machines; and his main current research interests are wind energy and modern power systems. He has led many research projects and has more than 400 technical publications with more than 10000 citations and h-index of 44 (Google Scholar).

Dr Chen is an Associate Editor of the IEEE Transactions on Power Electronics, a Fellow of the Institution of Engineering and Technology (London, U.K.), and a Chartered Engineer in the U.K.



**Ming Cheng** (M'01-SM'02-F'15) received the B.Sc. and M.Sc. degrees from the Department of Electrical Engineering, Southeast University, Nanjing, China, in 1982 and 1987, respectively, and the Ph.D. degree from the Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong, in 2001.

Since 1987, he has been with Southeast University, where he is currently a Distinguished Professor in the School of Electrical Engineering and the Director of the Research Center for Wind Power Generation. His teaching and research interests include electrical machines, motor drives for electric vehicles, and renewable energy generation. He has authored or coauthored over 300 technical papers and four books and is the holder of 55 patents in these areas.

Prof. Cheng is a fellow of the Institution of Engineering and Technology. He has served as chair and organizing committee member for many international conferences. He is a Distinguished Lecturer of the IEEE Industry Applications Society (IAS) in 2015/2016.