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A Fast Electro-Thermal Co-Simulation Modeling Approach for SiC Power MOSFETs

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***Abstract*— The purpose of this work is to propose a novel electro-thermal co-simulation approach for the new generation of SiC MOSFETs, by development of a PSpice-based compact and physical SiC MOSFET model including temperature dependency of several parameters and a Simulink-based thermal network. The PSpice electrical model is capable to estimate the switching behavior and the energy losses of the device accurately under a wide range of operational conditions, including high temperature operations, within a relatively fast simulation time (few seconds). The the thermal network elements are extracted from the FEM simulation of the DUT's structure, performed in ANSYS Icepack. A MATLAB script is used to process the simulation data and feed the needed settings and parameters back into the simulation. The parameters for a CREE 1.2 kV/30 A SiC MOSFET have been identified and the electro-thermal model has been validated through experimental and manufacturer's data.**

Keywords*— *Electro-thermal modeling, PSpice modeling, SiC-MOSFETs, Wide bandgap devices

NOMECLATURE

A	Device chip area (cm^2).
I_d	Drain current (A).
K_p	Saturation region transconductance (A/V^2).
K_{p0} , K_{p1}	K_p temperature scaling coefficients.
$L\sigma$	Stray inductance of the loop (H).
N_b	Doping density of the base (cm^{-3}).
P_{sw}	Switching power loss (W).
P_{cond}	Conduction power loss (W).
R_b	Resistance of epitaxial layer (Ω).
R_s	Drain substrate resistance (Ω).
T_j	Device junction temperature (K).
T_c	Device case temperature (K).
T_a	Ambient temperature (K).
T_{hs}	Heat-sink temperature (K).
T_0	Reference termperature (K).
V_{bd}	Device breakdown voltage (V).
V_{ds}	Drain-to-source MOSFET voltage (V).
V_{gs}	Gate-to-source MOSFET voltage (V).
V_t	MOSFET threshold voltage (V).
V_{t0} ,V_{t1}	V_t temperature scaling coefficients (V/K).
V_{th}	High current channel threshold voltage (V).
W_b	Width of the drift region (cm).
W_{dsj}	Drain-body depletion width (cm).

I. INTRODUCTION

Wide bandgap (WBG) semiconductor devices are capable of switching mode operation beyond the temperature limitations of traditional Silicon devices, offering reliable operation in a harsh environment [1]. So far Silicon Carbide (SiC) MOSFETs are among the most promising and developed WBG devices, showing outstanding switching speed and efficiency as well as attractive thermal properties. Discrete devices and power modules up to 1.7 kV breakdown voltage and 300 A rated current are already off-the-shelf with on-state resistances around 100 mΩ or less, which is quite unachievable with traditional silicon technology. Although the manufacturing technology of SiC MOSFETS is quickly approaching its maturity, the circuit modelling, especially referring to reliability of high-voltage devices has not been studied in the past research works. Several electrical and electro-thermal models have been developed and implemented so far, based on simple behaviorally-based [2] or physically-based equations [3], [4]. A survey of the available models' features and their implementations is reported in [5]. A co-simulation modeling approach for IGBT power modules was proposed in [6] and [7], aimed to reliability evaluation. An interesting electro-thermal modeling technique for WBG devices is presented in [8], though, to the best of authors' knowledge, nobody has applied a fast co-simulation modeling procedure (including temperature feedback) for the SiC MOSFETs so far. Former works have been using datasheet-driven losses profiles and not complete electro-thermal models capable of accurately estimating the device status under different operating conditions. Thus, an integrated modeling platform is proposed, which can exploit both the velocity and accuracy of electrically-oriented modeling software like PSpice and the flexibility of the MATLAB/Simulink environment, together with a detailed Finite Element Method (FEM) analysis of the thermal structure of the device. In the section II of the paper the structure of the

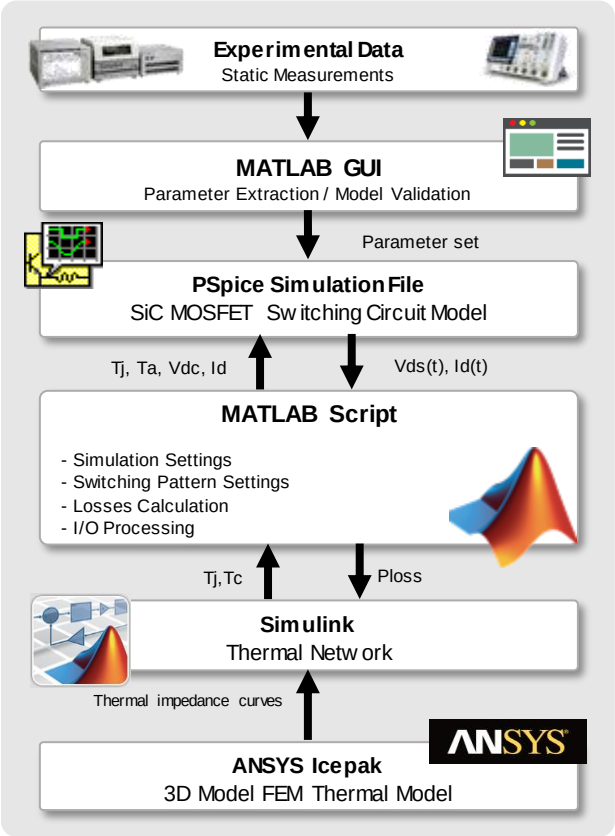

Fig. 1. Flowchart of the proposed co-simulation approach.

electro-thermal co-simulation procedure will be described in detail, including the overview of the PSpice SiC MOSFET model and the ANSYS Icepak simulation. Section III will be dedicated to a description of the static and switching measurements setup and section IV is dedicated to the validation of the model with experimental data from the performed measurements. Section V is dedicated to simulation results and shows the estimation of the junction and case temperature for simple switching mission profiles in a half-bridge inverter topology. Therefore, some conclusions and possible future improvements are stated.

II. Electro-thermal Co-Simulation Structure

A cross-section of the proposed co-simulation approach is depicted in Fig. 1. A SiC power MOSFET electro-thermal model, available in the literature [3], has been implemented in PSpice [9]. The PSpice simulation is launched from a MATLAB script with assigned circuit parameters (DC bus voltage, load current, ambient and junction temperature values) and is set to last for a single switching period. The parasitic elements of the switching circuit have been evaluated and included in the model. The simulation is rather fast (few seconds) and returns to MATLAB the current and voltage waveforms ($v_{DS}(t)$, $i_D(t)$). At this point, the algorithm calculates the conduction losses based on the on-state voltage and load current for a certain duty-cycle (Eq. 1), while the switching losses are extracted by averaging the energy loss on a switching period *Tsw* and subtracting the conduction losses as in Eq. 2.

$$P_{cond} = DV_{ON}I_{ON} \quad (1)$$

$$P_{sw} = \frac{1}{T_{sw}}\int_0^{T_{sw}} v_{DS}(t)\cdot i_D(t)\mathrm{d}t - P_{cond} \quad (2)$$

The two amounts are summed up and fed into a Simulink model, which includes the one-dimensional lumped thermal network, whose parameters have been previously obtained by FEM simulation. The parameters are variable for different losses amounts, and their impact is considered into behavioral equations, since the time needed for a FEM simulation would have been considerably slowing down the whole process. The thermal network simulation is launched for a given number of switching periods before returning the estimated temperature values for junction, case and heat sink. It has been observed that, depending on the switching frequency, the power loss of the device does not significantly variate in a few switching periods, and the temperature rise is almost negligible, thus we can assume it constant. A more frequent update of the temperature values means in fact a larger number of iterations and thus a longer time needed to simulate a certain switching pattern, but also increased accuracy in the estimation.

A. SiC Power MOSFET Model

The model presented in [3] by McNutt and others is a temperature-dependent SiC MOSFET physical model. It is well established among the available compact models and includes some quite interesting features, including a detailed physical characterization of the MOS channel current in linear and saturation regions [5]. The on-state behavior of the device is obtained as the series connection of the variable bulk (epitaxial layer) resistance *Rb* (visible in Fig. 2) with the MOSFET channel area and a constant drift substrate layer resistance *Rs*.

$$R_{on} = R_s + R_b \quad (3)$$

$$R_b = \frac{W_b - W_{dsj}}{qAN_b\mu_n} \quad (4)$$

The switching behavior of the MOSFET is determined by three variable capacitors (gate-to-source, gate-to-drain and source-to-drain) as shown in Fig. 2. Among the critical temperature-dependent parameters of the model there are the gate threshold voltage, the large signal transconductance and the carrier

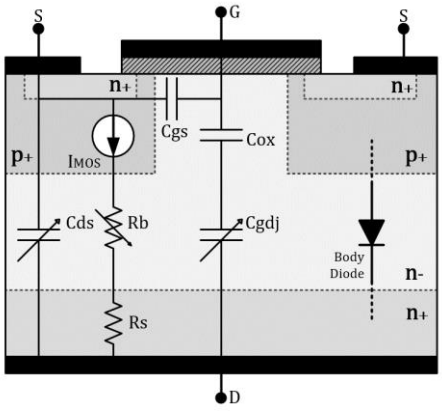

Fig. 2: SiC MOSFET model structure [2].

mobility (Eq. 5-7), which define the current capability of the device cell for a given temperature, as well as the variation of the on-state resistance.

$$V_T(T_j) = V_{T0} - V_{T1}(T_j - T_0) \quad (5)$$

$$K_p(T_j) = K_{p0}\left(\frac{T_j}{T_0}\right)^{K_{p1}} \quad (6)$$

$$\mu_n(T_j) = \frac{947}{1 + \left(\frac{N_b}{1.94 \times 10^{17}}\right)^{0.61}}\left(\frac{T_j}{T_0}\right)^{-2.15} \quad (7)$$

Some novel features were included in the model, which is now capable to calculate the power loss during the simulation, accounting for self-heating. The model is thus complete with the estimation of both switching and conduction losses. The power loss due to leakage current has been assumed negligible in this work, so there is no current flowing during the off-state in the model. During the experimental characterization of the device, in fact, the leakage current has been observed to be small enough (around few µA) to be neglected. The model has been implemented in PSpice simulation environment in the form of a *.cir* simulation profile code, which is capable of rather fast convergence time (always below one minute) in the range of few microseconds. The parameters for this model have been identified by a dedicated parameter extraction tool, developed in MATLAB through a GUI [9]. The procedure basically consists in an analysis of I-V static characteristics, capacitance measurements of the DUT and rearrangements of the model's equations. The tool is general purpose for SiC MOSFETs and completely open-source and can be found at [10].

B. FEM-based Lumped Thermal Network

In order to introduce a temperature-dependent model, a physically-based model of the SiC power MOSFET is built in ANSYS Icepack (Fig. 3-4). The method to characterize thermal behavior is based on a boundary-dependent lumped thermal network which varies with respect to the power losses, cooling system performance and ambient temperature. In order to extract lumped thermal parameters, i.e. thermal resistance and thermal capacitance, a trial analysis is implemented by giving a volumetric step power loss to the chip junction area and extraction of temperature responses in the junction and case monitoring points. A temperature distribution is shown in Fig. 4, where two devices (operating in a half-bridge configuration) are clamped on a heatsink, as will be explained later in the

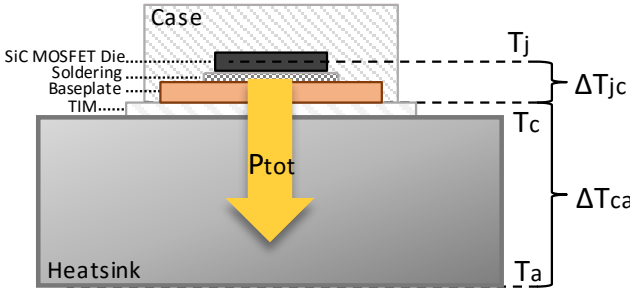

Fig. 3. Physical structure of the modeled system (device + heatsink).

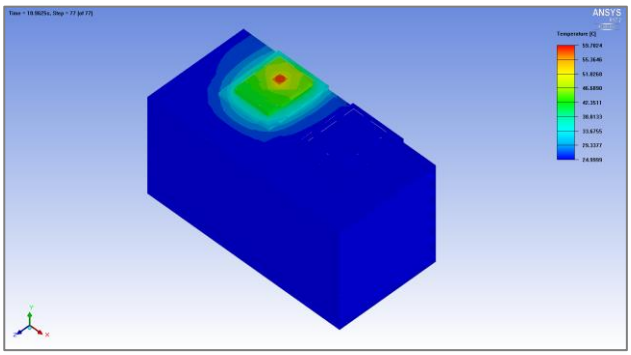

Fig. 4. 3D FEM thermal model developed in ANSYS Icepack.

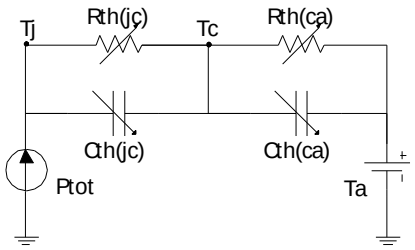

Fig. 5. Equivalent electrical circuit of the lumped thermal network.

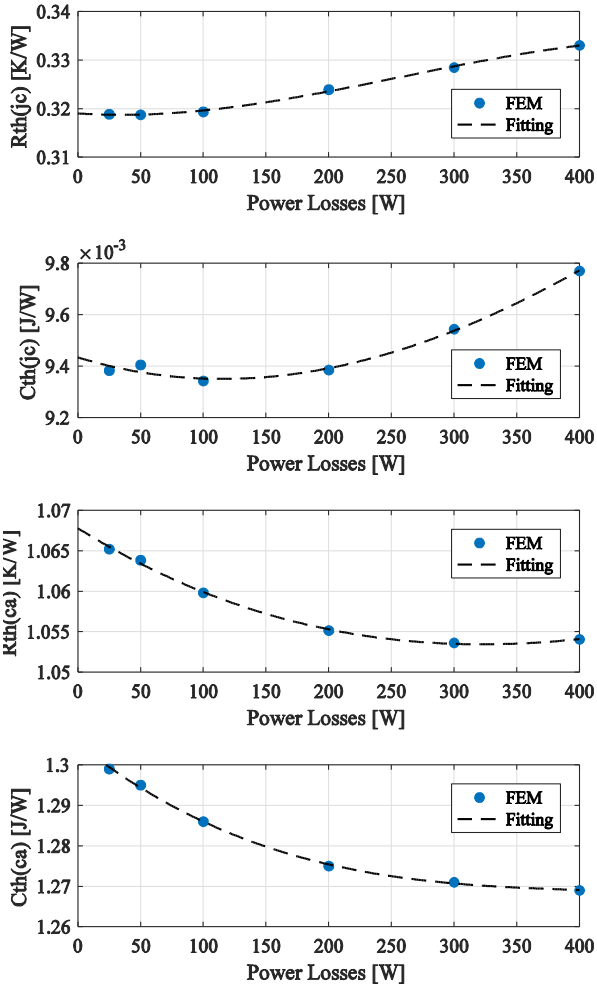

Fig. 6. Fitting of the lumped thermal network impedance curves

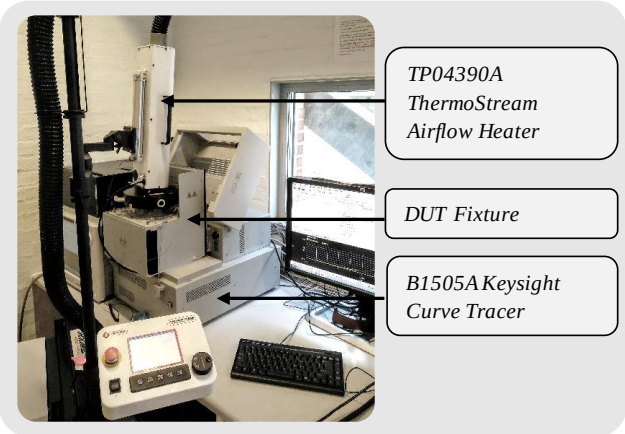

Fig 7. Laboratory setup for static measurements.

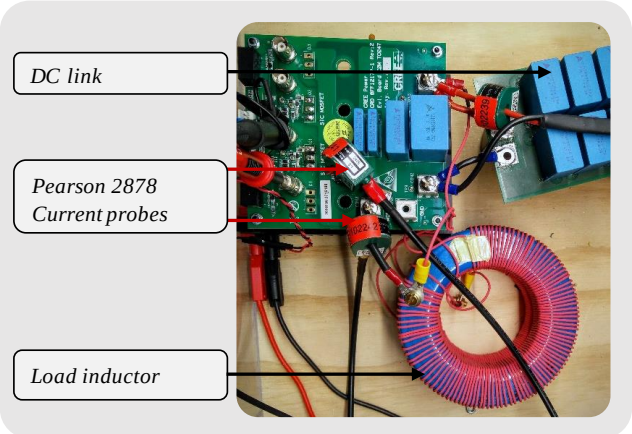

Fig. 8. Laboratory setup for DPT.

experimental setup description. The distance between the device and their alternate switching mode can lead to the assumption of neglecting the thermal coupling between them in the thermal network and considering them as acting independently. According to the method presented in [11], [12] the transient thermal impedance curves and consequently the lumped parameters are identified. It has been proven in [12] that with high accuracy single-element lumped networks can be used as shown in Fig. 5, representing the equivalent electric circuit used in the Simulink model to estimate junction and case temperature. Knowing the lumped elements for a few sample points in the range of boundary conditions variation and extrapolation of the fitted curve (Fig. 6), the following fitting equations are obtained:

$$R_{th(jc)} = -4 \cdot 10^{-10}P^3 + 3 \cdot 10^{-7}P^2 - 2 \cdot 10^{-10}P + 0.3$$

$$C_{th(jc)} = -3 \cdot 10^{-12}P^3 + 7 \cdot 10^{-9}P^2 - 1 \cdot 10^{-6}P + 0.01$$

$$R_{th(ca)} = -7 \cdot 10^{-11}P^3 + 2 \cdot 10^{-7}P^2 - 1 \cdot 10^{-4}P + 1.07$$

$$C_{th(ca)} = -5 \cdot 10^{-10}P^3 + 6 \cdot 10^{-7}P^2 - 2 \cdot 10^{-4}P + 1.3$$

III. Measurement Setup

The whole experimental work has been carried out in the laboratory facilities at Aalborg University, Denmark. The static behavior measurements (Fig. 7) necessary to identify the model parameters for the device have been performed with a B1505A Keysight curve tracer/device analyzer. A fixture was connected in order to execute measurements at different temperatures. A TP04390A ThermoStream airflow heater has been used to heat the fixture up to the desired set-point for the time necessary for the junction to be at the same temperature as the outer environment. The DC transfer and output characteristics were measured for five different temperature values from room temperature up to 150°C (the maximum allowed for the fixture). A Double-Pulse test (DPT) setup (Fig. 8) has been developed to observe the switching behavior of the MOSFET for different current values up to the rated drain current and up to 600V DC bus voltage [13]. A CREE evaluation PCB optimized for SiC MOSFET switching tests has been connected to a DC bus by a 47 µF DC-link capacitor bank and to a 1 mH, 100A load inductor in the topology shown in Fig. 9. Two gate drive circuits are embedded in the PCB with 10 Ω gate resistance, and have been controlled by the signals from an Arduino DUE microcontroller board. The upper MOSFET, in parallel with the load inductor, has been used as freewheeling path for the load current during off-state through its body diode. Both the MOSFETs have been screwed on an aluminum heatsink which has been heated by a resistive heating element controlled by a PID temperature regulator, whose feedback

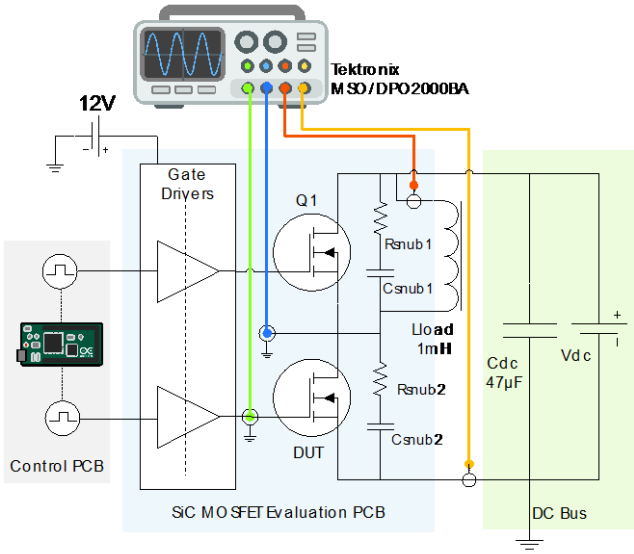

Fig. 9. Schematic of the DPT laboratory setup.

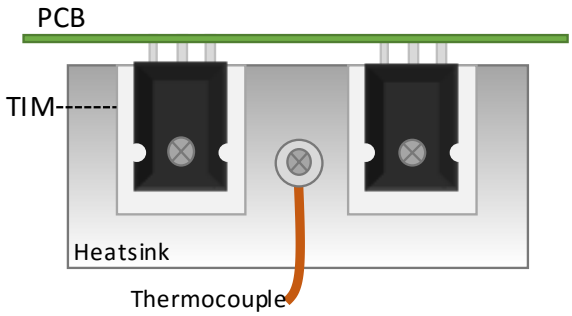

Fig. 10. Physical layout of the half-bridge configuration with the heatsink.

comes from a thermocouple placed on the heatsink, as sketched in Fig. 10. This solution has been chosen in order to guarantee a homogeneous temperature distribution among the two devices, without the bulk and inaccuracy problems due to the use of a larger hot plate. A *Pearson 2878* coil was used to measure the drain current for the DUT on the lower switch's source terminal, while a second one was detecting the load current. The difference between the two amounts yields the current in the body diode of the upper MOSFET. A Tektronix MSO/DPO2000BA digital oscilloscope was used for the waveforms capture. 100x high voltage probe measured the DUT's drain-source voltage and a low voltage probe was connected between its gate and source contacts. BNC ports were already available on the evaluation board. The board also includes a snubber parallel branch for each device (100 pF capacitor and 10 Ω resistor) which must be included in the simulations to correctly estimate the switching behavior.

IV. Experimental Results and Model Validation

A 1.2 kV discrete SiC power MOSFET C2M0080120D from CREE has been chosen for the experimental validation of the model and used as a case study for the electro-thermal simulations. Some of the rated parameters for the device are reported in Tab. 1.

TABLE 1. DUT RATED PARAMETERS

Part Name	C2M0080120D
Package	TO-247-3
Rated Breakdown Voltage	1200 V
Rated Drain Current	31.6 A (25°C)
Gate Source Voltage	-5 / +20 V
Operating Junction Temp.	-55°C to +150°C
On-state Resistance	80 mΩ (25°C)
Internal Gate Resistance	4.6 Ω
Die Thickness	180 µm
Die Size	3.10 × 3.36 mm

A. Static Curves Validation

The curves in Fig. 11 to Fig. 13 show respectively the DC transfer characteristics (in the saturation region, with 20 V drain bias) of the MOSFET for different junction temperature values, the on-state curves for increasing drain bias (and 20 V constant gate bias) and different temperatures and the MOSFET capacitances for a drain bias sweep (while gate is kept to 0 V). It can be observed in Fig. 11, that the current capability of the device decreases with increasing temperatures for high gate voltages due to the higher drift resistance, which is dominant in this region (labeled as PTC: positive temperature coefficient). For lower gate voltages, as the temperature increases, the channel resistance becomes smaller, thus causing the current to increase (NPT: negative temperature coefficient). The parameters for the PSpice model have been identified by means of these experimental static characteristics and the validation of the model (including sensitivity to temperature) has been performed. The simulated curves are overlapped to the experimental ones in the figures showing a rather good matching, with a relative error always below 5%. Therefore, it has been possible to properly estimate and simulate the on-state

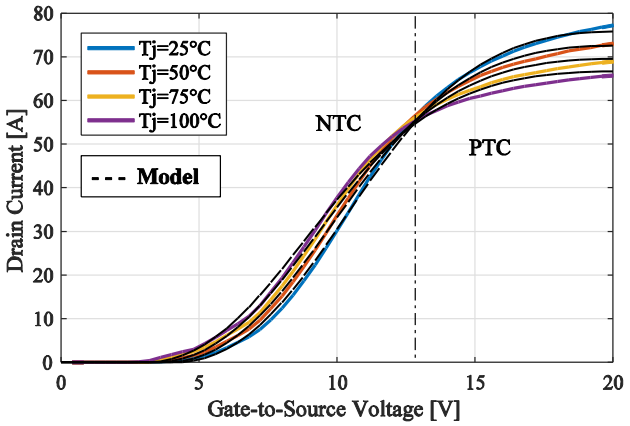

Fig. 11. Validation of static DC transfer curves for different temperatures.

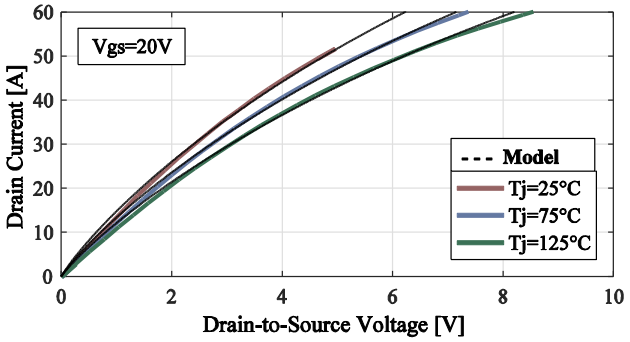

Fig. 12. Validation of static DC output curves for different temperatures.

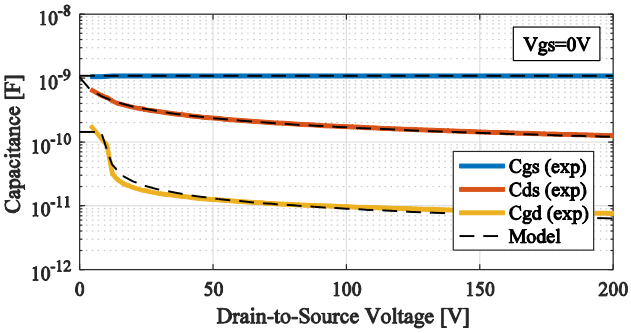

Fig. 13. Validation of the MOSFET capacitances for increasing drain-to-source voltage and zero gate bias.

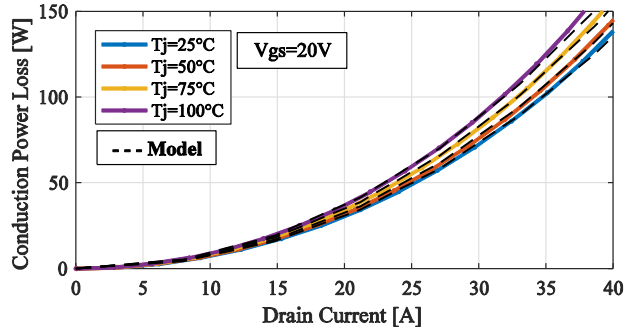

Fig. 14. Validation of the on-state power loss estimation for multiple temperatures for increasing drain current values.

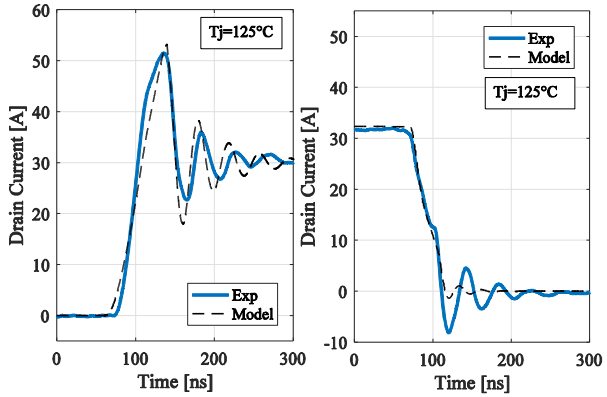

Fig. 15. Validation of Id(t) switching turn-on (left) and turn-off (right)

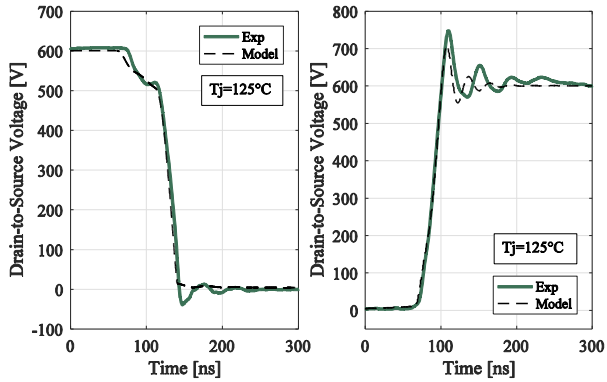

Fig. 16. Validation of Vds(t) switching turn-on (left) and turn-off (right)

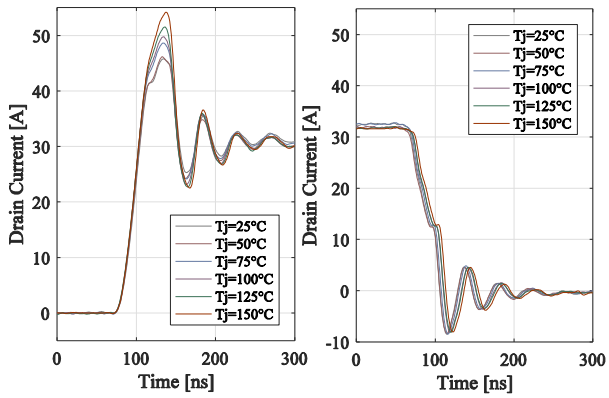

Fig. 17. Switching Id(t) waveforms for increasing Tj

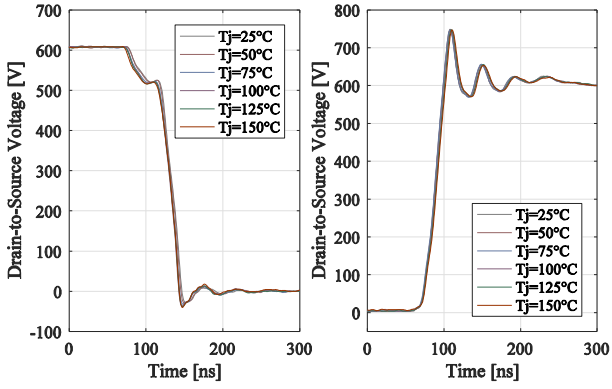

Fig. 18. Switching Vds(t) waveforms for different junction temperatures.

TABLE II. DPT RESULTS

Parameter	Unit	Value
Tj	°C	150
V_{DC}	V	600
Id	A	30
Lσ	nH	17
Rg	Ω	10
$V_{OS\%}$	-%	24.5 (18)
$I_{OS\%}$	-%	75.6 (77.1)
Eon	mJ	0.98 (0.82)
Eoff	mJ	0.19 (0.14)
Etot	mJ	1.17 (0.96)

power loss for different *Tj* values and for increasing drain current, as displayed in Fig. 14.

B. Switching Waveforms Validation

The DPT has been carried out on the DUT with a DC bus voltage of 600 V, increasing the drain current up to the rated value and heating up the device to the maximum rated working temperature. The aim of the test is the validation of the model for the dynamic behavior and the investigation of the temperature effects on the switching losses. The former goal is achieved with good accuracy in the waveforms reported in Fig. 15 and Fig. 16, where turn-on and turn-off experimental waveforms for *Id* and *Vds* are compared to simulations. The oscillations which can be observed in the waveforms are mainly due to the resonance between the loop stray inductance and the load parallel parasitic capacitance. It has been possible to extrapolate the values of the two elements from the oscillation

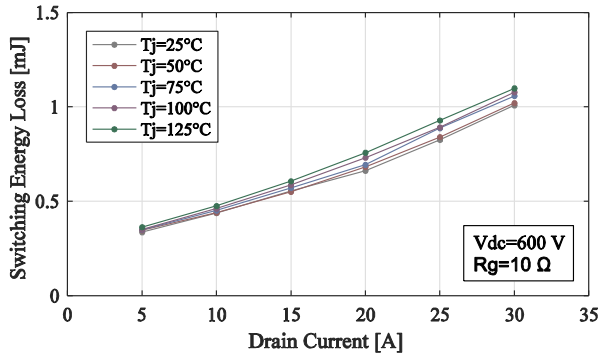

Fig. 19. Total switching energy loss vs. Id for increasing Tj.

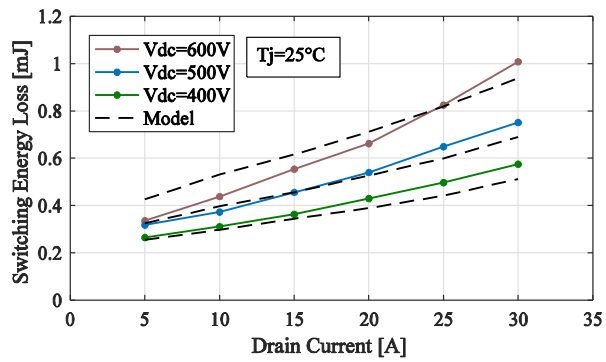

Fig. 20. Switching losses validation for increasing Id and Vdc at room temperature.

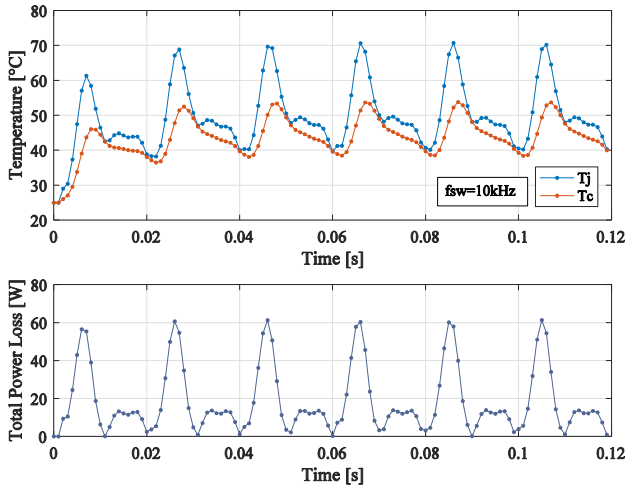

Fig. 21. Switching profile simulation results: temperatures (upper) and total power loss (lower) for fsw=10 kHz and Ipk=30 A.

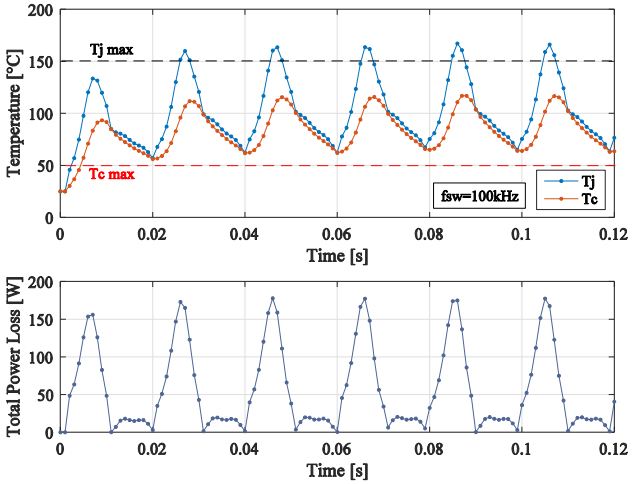

Fig. 22. Switching profile simulation results: temperatures (upper) and total power loss (lower) for fsw=100 kHz and Ipk=30 A.

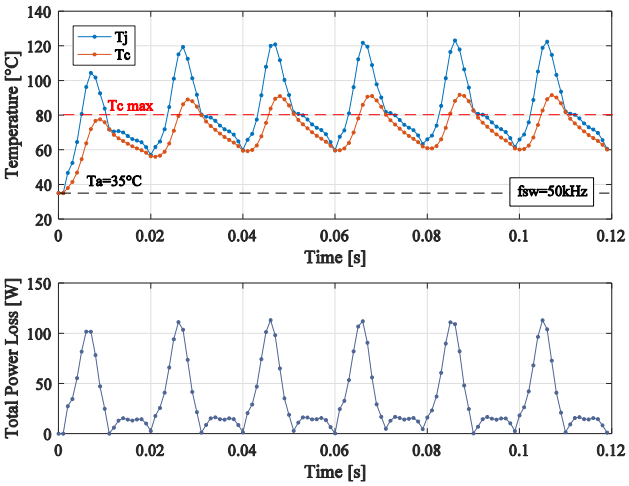

Fig. 23. Switching profile simulation results: temperatures (upper) and total power loss (lower) for fsw=50 kHz, Ipk=30 A and Ta=35°C

frequency and the turn-on drop in *Vds*, and fit them in the circuit model to emulate the real behavior. Table II reports the result of the switching test carried out at the limit rated current and temperature conditions, and the comparison with the model estimations (in brackets).

It can be observed in Fig. 17 and Fig. 18, how the switching waveforms are actually almost unchanged for increasing junction temperature. In fact, the entity of the device's capacitances, which determine the dynamic behavior, is quite unaffected by high temperature. The slight changes in the waveforms can be due to the drift of the gate voltage threshold or the variation of the internal gate resistance, resulting in a minor increase of the rise and fall time for the drain current. This is also visible in Fig. 19 where the switching energy loss are calculated for increasing current values and a number of junction temperatures. Nevertheless, the model is capable to estimate the switching energy at different voltage and current levels (Fig. 20), which is in fact a most critical feature for the co-simulation.

V. Co-Simulation Results

A half-bridge inverter topology has been chosen for the simulation of a switching mission profile. The two devices on the inverter leg are controlled by a 2L-SPWM switching pattern. This means that, in order to obtain a 50 Hz sinusoidal current flowing through the load, each of the devices has to operate during half of the sine period. Due to the inductive nature of the load, the freewheeling current will be flowing through the body diode of the opposite device during the rest of the period. The body diode conduction losses have been taken into account in the model considering the current flow through the body resistance of the device (which is also temperature dependent). The same thermal network has been used to model the diode operation. The current flows through the same die, and is located at the cell's border. By the way, considering the high number of cells in parallel in the die, the power loss distribution can be considered homogeneous. This would have been different in case of a module with an external paralleled diode chip. In this case, in fact, two different thermal networks and the thermal coupling between the dies should have been taken into account [8].

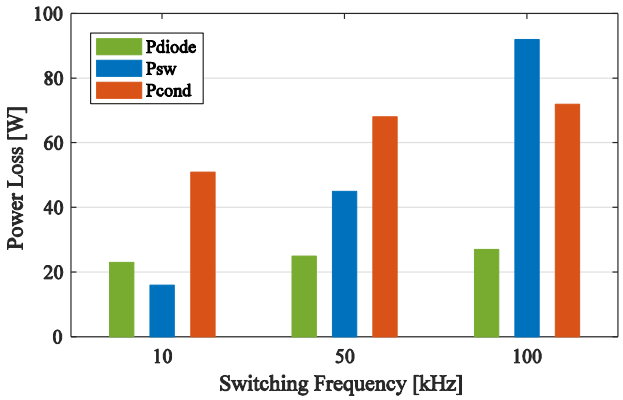

Fig. 24. Losses distribution chart for increasing switching frequency.

A number of switching frequencies and current peak values were set to test the estimation capability of the algorithm and verify the performance of the device.

A 0.1 ns maximum step-size has been used in the PSpice simulation in order to get a precise estimation of the switching waveforms (which usually takes less than 10 s to converge). The update rate for the temperature feedback has been set depending on the chosen switching frequency, aiming to have a trade-off between simulation time and accuracy. It turned out that a 1 ms step for the Simulink model of the thermal network is enough to obtain fairly good results in a quite small simulation time. The algorithm can estimate a switching mission profile for long enough to reach the steady-state conditions in less than 10 minutes. Fig. 21 to Fig. 23 show the results of the simulation of a switching profile for different switching frequencies (10, 100 and 50 kHz) and 30 A peak current. In the plots dedicated to the total power loss, it can be clearly noticed how the power increases following the current value in the first half of the period, while the body diode's conduction losses are visible in the second half. It can be observed, in Fig. 22, how the temperature (both *Tj* and *Tc*) reach values beyond the rated working limits for *fsw*=100 kHz. Moreover, in Fig. 23 the ambient temperature was raised to 35°C with a consequent increase of the junction and case temperatures. The distribution of the power losses (body diode, switching and MOSFET conduction) for the three cases (at peak current) is reported in the chart in Fig. 24.

VI. CONCLUSIONS

A novel electro-thermal modeling approach for SiC Power MOSFETs based on co-simulation has been developed and tested. It is capable to estimate the power losses, junction and case temperatures of the device in a wide range of operating conditions and for an assigned switching mission profile. The PSpice model is capable to accurately estimate the switching and on-state losses, while the lumped thermal network is based on detailed FEM analysis. The simulation time for a given mission profile is short enough to guarantee a fast insight on the device's thermal performances (including case and heatsink) and can be used to build up derating curves and safe operating area charts. This can be a powerful aid to the design of converter topologies in many applications. The procedure has been validated and tested on a discrete low-power device, but it can easily be adapted to high-power modules by modifying the PSpice model and generate a proper thermal network. The approach is potentially suitable for the simulation of long term mission profiles. Nevertheless, the model estimation capability for abnormal conditions should be evaluated aiming to the reliability assessment of power devices. The developed tool will soon be available at [10].

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