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Published in:
Proceedings of 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)

DOI (link to publication from Publisher):
10.23919/EPE17ECCEEurope.2017.8099329

Publication date:
2017

Document Version
Accepted author manuscript, peer reviewed version

Feedforward Control Strategy for the state-decoupling Stand-alone UPS with LC output filter

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Keywords

<<Cascaded Control>>, <<UPS system>>,<<Feedforward control>>,<<Disturbance rejection>>

Abstract

In this paper, the disturbance rejection performance of the cascaded control strategy for UPS system is investigated. The comparison of closed loop system performance between conventional cascaded control (CCC) strategy and state-decoupling cascaded control (SDCC) strategy are further explored. In order to further increase the load current disturbance rejection capability of the state-decoupling in UPS system, a feedforward control strategy is proposed. In addition, the design principle for the current and voltage regulators are discussed. Simulation and experimental results are provided to verify the theoretical analysis.

I. Introduction

The voltage source inverter (VSI) has been playing an important role in energy conversion[1]. Normally, voltage and current controllers are cascaded in designing VSI-based UPS system[2], where a wide bandwidth current loop is nested inside an out narrower bandwidth voltage loop. This approach has several advantages, including the ability to directly control and limit the inductor's current during transient as a protection feature, as well as the ability to regulate the inductor's current following the reference current. Finally, the design of the voltage regulator is less critical and more robust than that in the single loop voltage control scheme.

Research on the voltage and current regulator design for grid-connecting inverter[3, 4], motor drive system and stand-alone VSI[5] has been widely investigated. For stand-alone VSI UPS system, the main task of the controller is to regulate the output voltage to track the reference voltage and reject the disturbance caused by the load current. In [5], an SDCC method is proposed by decoupling capacitor's voltage in the

inner current loop, where the system transient performance is increased. However, the SDCC method actually decreases the disturbance rejection ability due to the system decoupling, which has not been discussed in previous literature.

In this paper, first, the system model is established to investigate the disturbance rejection ability for CCC strategy and SDCC strategy. Furthermore, in order to increase the disturbance rejection ability of SDCC, a direct feedforward control strategy is proposed to mitigate the influence of the load disturbance. For practical implementation, a lead filter is embedded in the feedforward control strategy to reduce the delay by the PWM module. In addition, the design of current and voltage regulators are discussed from a practical view. Finally, the case study is investigated both in simulation and experiment to verify the theoretical analysis.

II. Modeling of stand-alone UPS System

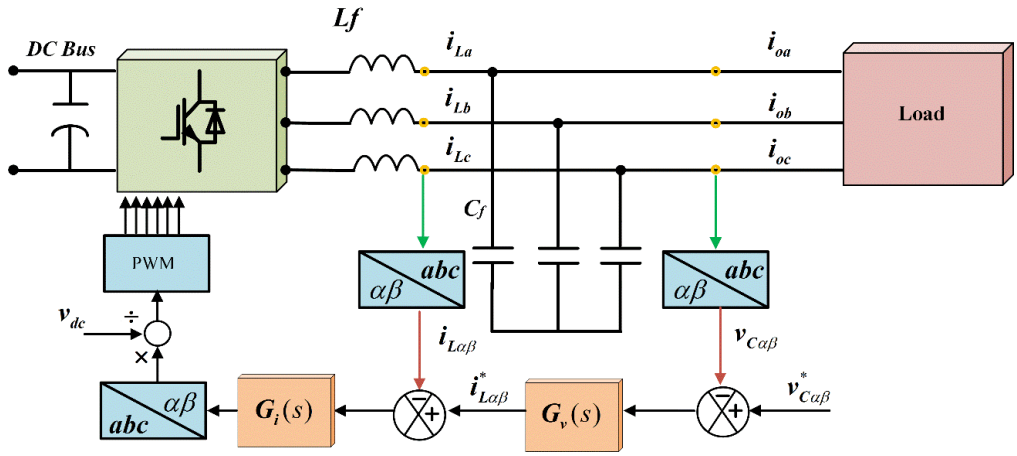


Fig.1. Block diagram of a three-phase VSI with voltage and current regulators.

Fig.1 shows the schematic of a stand-alone UPS system, where the VSI is connected to the load through an *LC* filter and is operated in voltage-controlled mode (VCM) by regulating capacitor's voltage and inductor's current. Normally, voltage and current controllers are cascaded to regulate the output capacitor's voltage and inductor's current for tracking the reference signals.

The control diagram of the closed loop system for CCC is shown in Fig.2, where the $v^*_{C\alpha\beta}$ and $i^*_{L\alpha\beta}$ are the reference of capacitor voltage and inductor current.$i_{o\alpha\beta}$ is the output current which is considered as the disturbance. $G_v(s)$ and $G_i(s)$ are the voltage and current controller.$G_{PWM}(s)$ represented the transfer function including the computation and PWM delay.

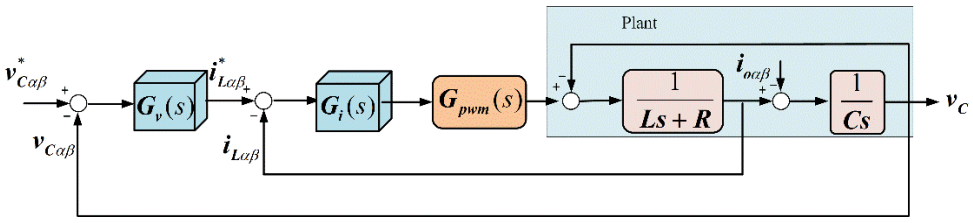


Fig.2 Control Block of CCC strategy

The $G_{PWM}(s)$ is expressed as $G_{PWM}(s) = \frac{1-\frac{T_d}{2}s}{1+\frac{T_d}{2}s}$, $T_d = \frac{1.5}{f_s}$, where f_s is the switching frequency to achieve an accurate description of PWM delay effect, the closed loop transfer function is shown as:

$$v_{C\alpha\beta}(s) = \underbrace{\frac{G_v(s)G_i(s)G_{PWM}(s)}{LCs^2+RCs+(Cs+G_v(s))G_i(s)G_{PWM}(s)+1}}_{first\ term} v^*_{C\alpha\beta}(s) - \underbrace{\frac{Ls+R+G_i(s)G_{PWM}(s)}{LCs^2+RCs+(Cs+G_v(s))G_i(s)G_{PWM}(s)+1}}_{second\ term} i_{o\alpha\beta}(s) \quad (1)$$

When the state decoupling strategy [5] is employed to the stand alone VSI system, as is shown in Fig.3 The closed loop transfer function is shown as:

$$v_{C\alpha\beta_d}(s) = \underbrace{\frac{G_v(s)G_i(s)G_{PWM}(s)}{LCs^2+RCs+(Cs+G_v(s))G_i(s)G_{PWM}(s)-G_{PWM}(s)+1}}_{first\ term} v^*_{C\alpha\beta}(s) - \underbrace{\frac{Ls+R+G_i(s)G_{PWM}(s)}{LCs^2+RCs+(Cs+G_v(s))G_i(s)G_{PWM}(s)-G_{PWM}(s)+1}}_{second\ term} i_{o\alpha\beta}(s) \quad (2)$$

Where the first term is the closed loop gain for the reference voltage and should be unity at the fundamental frequency, meanwhile, the second term is output impedance that should be designed to be low enough for the disturbance rejection

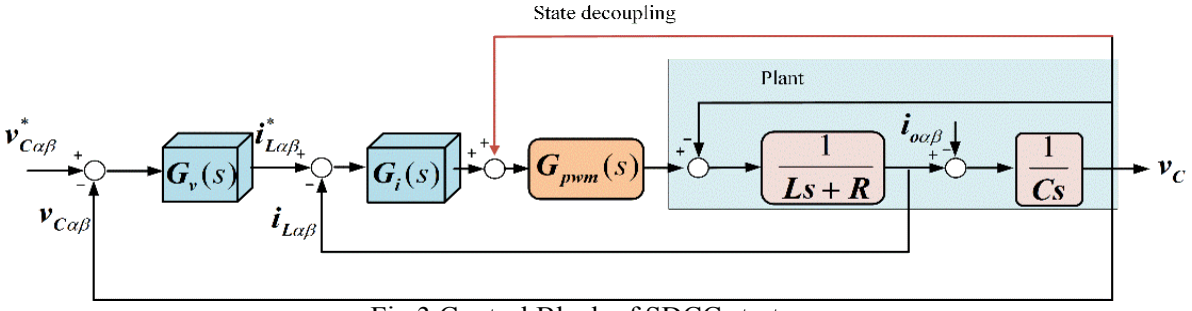
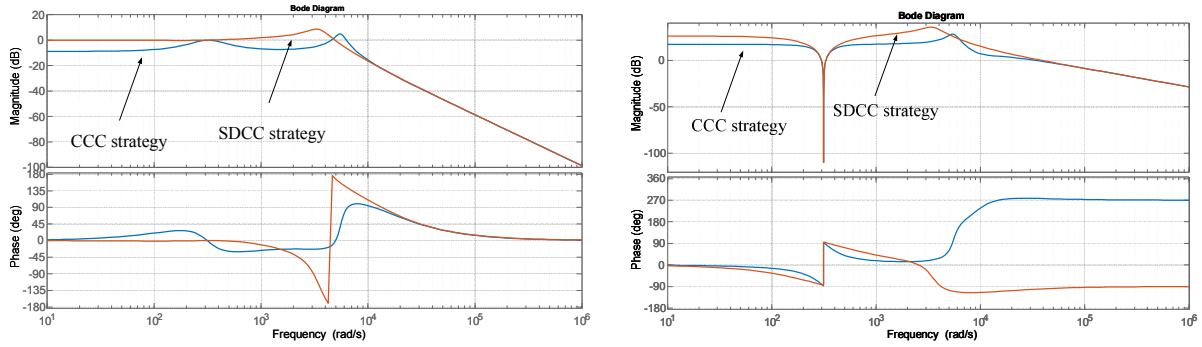


Fig.3 Control Block of SDCC strategy

III. Proposed Control strategy and frequency domain analysis

In this section, the closed loop Bode plots will be implemented to investigate the reference tracking and disturbance rejection ability for CCC and SDCC strategies. The parameters selected for the Bode plots are shown in Table I. By plotting the first term of (1) and (2), it is observed from Fig.4(a) that with the CCC strategy the system shows a low gain at a broad frequency range, only at fundamental frequency the command reference is properly tracked. On the contrary, with SDCC strategy output voltage is able to track the reference at a broad frequency range without steady state error. However, as is shown in Fig.4(b), although these two strategies both have good performance in rejecting the fundamental frequency disturbance, the other frequency disturbance rejection ability with SDCC strategy is less than that of the

CCC strategy, as the higher gain with SDCC strategy indicates more disturbance signals exist in the output voltage. When the step load change occurs, the stepped current contains a broad frequency disturbance signals that would influence the output voltage, with the SDCC strategy the output voltage will suffer from larger disturbance.



(a) Reference tracking (b) Disturbance rejection

Fig.4 Bode plot of closed loop system for the voltage loop for reference tracking and disturbance rejection

In order to further increase the disturbance rejection ability for the SDCC based UPS system, the feedforward control strategy is added to the system, as is shown in Fig. 5.

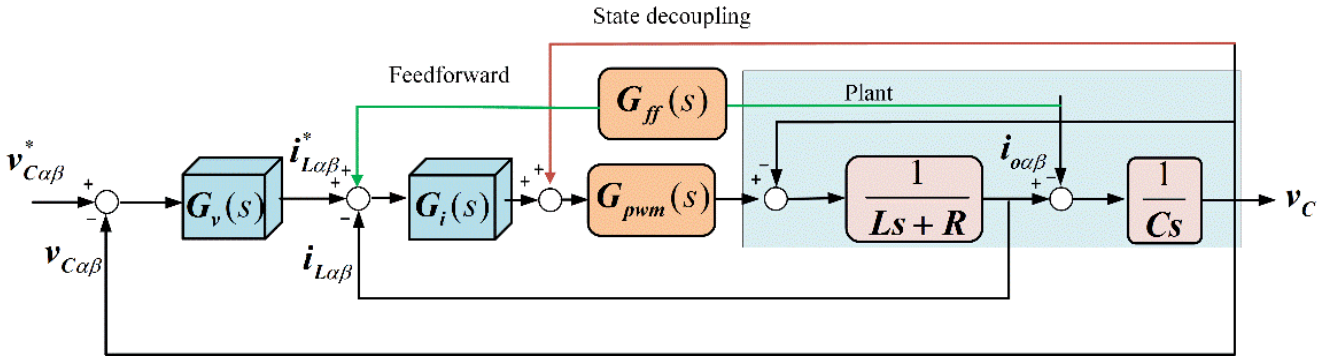


Fig.5 Control Block of UPS system with feedforward strategy

When the $G_{ff}(s) = 1$, from Fig.5, the closed loop transfer function is expressed as:

$$v_{C\alpha\beta_d}(s) = \underbrace{\frac{G_v(s)G_i(s)G_{PWM}(s)}{LCs^2+RCs+(Cs+G_v(s))G_i(s)G_{PWM}(s)-G_{PWM}(s)+1}}_{first\ term} v^*_{C\alpha\beta}(s) - \underbrace{\frac{Ls+R+G_i(s)G_{PWM}(s)}{LCs^2+RCs+(Cs+G_v(s))G_i(s)G_{PWM}(s)-G_{PWM}(s)+1}\left(1-\frac{G_i(s)G_{PWM}(s)}{Ls+R+G_i(s)G_{PWM}(s)}\right)}_{second\ term} i_{o\alpha\beta}(s) \quad (3)$$

The Bode plot for disturbance rejection is shown in Fig.6 (orange curve), where it is observed the disturbance rejection ability is remarkably increased compared to the other two methods, especially for the frequency range from 0 *rad/s* to $10^3\ rad/s$.

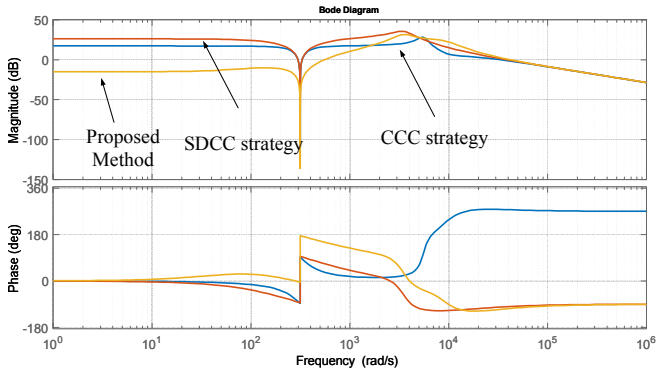


Fig.6 Comparison of Bode plot for disturbance rejection

IV. Current and Voltage Controllers Design

For the inner current loop, due to the state-decoupling, only the proportional controller can satisfy the current tracking requirement and dynamic performance for the current regulation, the parameter for K_{PI} is selected as

$$K_{PI} = \alpha_c L_f \tag{5}$$

Where $\alpha_c \leq \frac{w_s}{10}$, w_s is the angular sampling frequency. For the voltage regulator, a proportional resonant controller with compensation angle is implemented and expressed as:

$$G_v(s) = K_{PV} + \sum_{h=1,5,7} \frac{K_{iV}(scos\varphi_h - h\omega_1 sin\varphi_h)}{s^2+(h\omega_1)^2} \tag{6}$$

Where h is the harmonic order that needs to be compensated. The proportional gain K_{PV} determines the bandwidth of the voltage regulator. Finally, for the discrete-time realization on the digital controller, the resonant frequency should not be shifted due to the discretization. Therefore, the Tustin method with pre-warping [6]should be implemented, which is referred to:

$$s \rightarrow \frac{h\omega_1}{\tan(\frac{h\omega_1 T_s}{2})} \frac{z-1}{z+1} \tag{7}$$

Table. I System Parameters

Physical Parameter	
Nominal Inductance L_N	1.8mH
ESR of Inductor	0.02ohm
Capacitance	27uF
Sampling frequency	10kHz
Load 1	470ohm
Load 2	50 ohm
Voltage controller Parameter	
K_{PV}	0.05
K_{IV}	500
Current controller parameter	
K_{PI}	11.8

V. Case Study

In order to validate the theoretical analysis, the comparison of these methods is illustrated with Matlab/Simulink and experiment. The system configuration is the same as Fig. 1, where system parameter is illustrated in Table.I. two resistive loads are connected in parallel, at the 0.3s, the load 2 is switched off from the UPS system. therefore, the load current

drops from 4.8A to 0.5A, the influence of the load current to the output voltage for these three methods are shown in Figs.7- 9, where output voltage has an overshoot of 120V with SDCC strategy (Fig.7) while output voltage overshoot is around 100V with CCC strategy (Fig.8). In contrast, when the proposed method is applied to the control strategy, the disturbance rejection ability is highly increased with no overshoot when the load2 is switched off (Fig.9).

The proposed control strategy is also verified in an experimental testbed. The platform consists of Danfoss three phase converter with LC filter. System parameters are the same as Table I. Comparison between the SDCC and proposed method are illustrated in Figs. 10 and.11, where in Fig.10 it is observed that the current abrupt change has a significant influence on the output voltage while the output voltage almost does not change when the proposed method is applied.

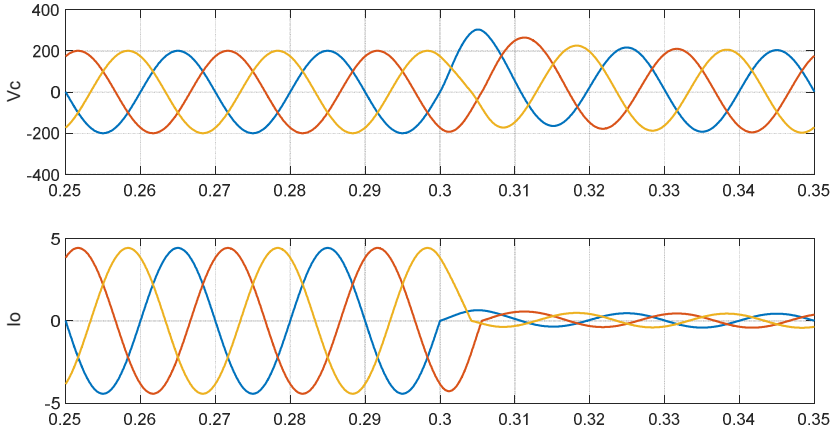


Fig.7 Disturbance rejection performance with SDCC strategy

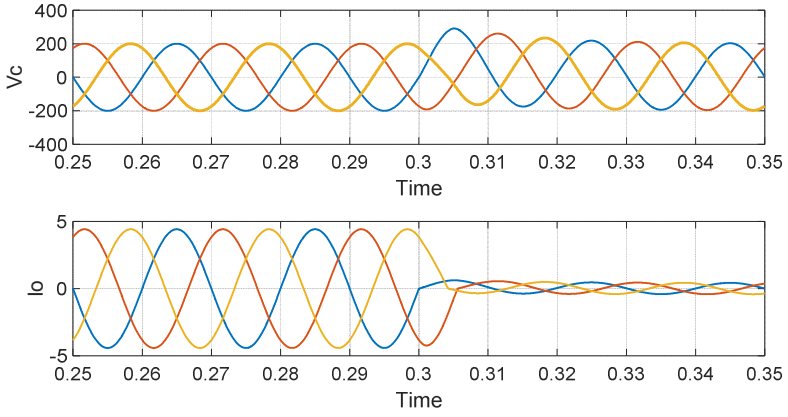


Fig.8 Disturbance rejection performance with CCC strategy

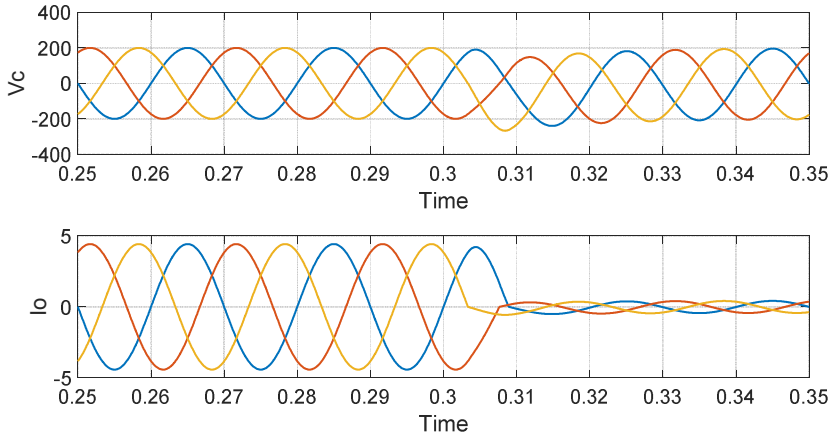


Fig.9 Disturbance rejection performance with SDCC strategy

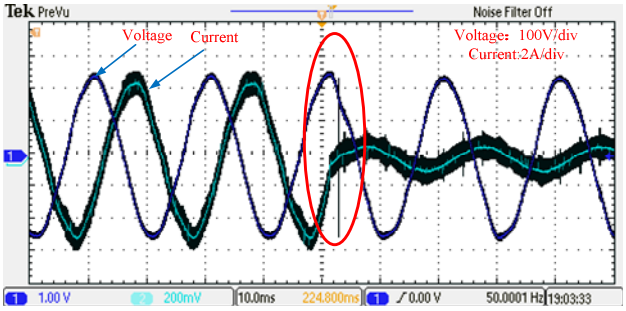


Fig.10 Experimental result with SDCC strategy

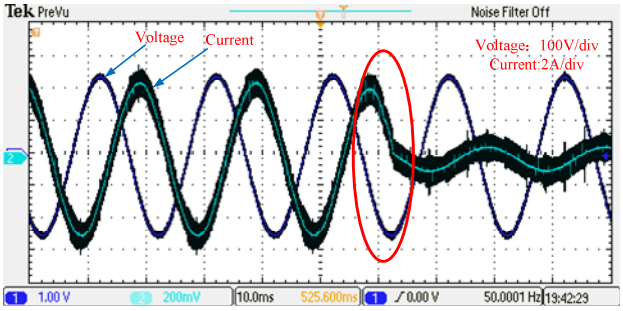


Fig.11 Disturbance rejection performance with proposed strategy

VI. CONCLUSIONS

This paper proposed a feedforward control strategy for the state-decoupled stand-alone UPS system, Bode plots shows the disturbance rejection ability is highly increased compared with SDCC and CCC methods. Simulation and experimental results show the effectiveness of the proposed method.

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