SSTL I/O Standard Based Environment Friendly Energy Efficient ROM Design on FPGA

Bansal, Neha; Bansal, Meenakshi; Saini, Rishita; Pandey, Bishwajeet; Kalra, Lakshay; Hussain, Dil Muhammad Akbar

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LVCMOS I/O Standard Based Environment Friendly Energy Efficient ALU Design on FPGA

Neha Bansal, Meenakshi Bansal, Rishita Saini, Bishwajeet Pandey, Lakshay Kalra
School of Electronics and Electrical Engineering,
Chitkara University, Punjab, India
gyancity@gyancity.com, rishita0025@gmail.com,
meenakshibansal94@gmail.com, nehabansal075@gmail.com

D. M. Akbar Hussain
Department of Energy Technology,
Aalborg University, Denmark
akh@et.aau.dk

Abstract— **in this work, we are making energy efficient 32-bit ALU by using different classes of LVCMOS IO standard. Here, we are operating our design with operating speed of 4th generation i7 processor in order to test the compatibility of our design with the latest state of the art technology based processor. When there is no demand of peak performance, then we can save 75.2% Clock power, 75% Logic power, 75.36% Signal power, 81.82% I/O power by operating our device with 1GHz frequency in place of maximum 4GHz. LVCMOS25 having 69.65%, 53.48%, 38.77% more power consumption with respect to LVCMOS12, LVCMOS15, LVCMOS 18 at 2.9GHz respectively. In this we used, VERILOG hardware description language, XILINX ISE simulator, and Virtex-6 FPGA and XPower analyzer.**

Keywords—I/O standard; LVCMOS; Power Optimized Design; I/Os Power.

I. INTRODUCTION

This LVCMOS (Low Voltage Complementary Metal Oxide Semiconductor) Input/output (I/O) standard based energy efficient ALU design is implemented on Virtex-6 FPGA. In order to make energy efficient ALU, now we are going to use different LVCMOS I/O Standard 12, LVCMOS I/O 15, LVCMOS I/O 18, and LVMOS I/O 25. In this work, we mainly study the analysis of reduction of I/Os power at different frequency [1]. Multiplier is used to enhance the speed of ALU in reference [2]. In order to make ALU energy efficient, reference [3] are using adders and multipliers. Bidirectional adder based asynchronous low power Arithmetic logic unit design is discussed in [4]. In this whole process of [5], they have designed floating point ALU which helps in providing the high performance. Reference [5] also give a methodology to optimize an arithmetic logic unit for area and power. There are other work in energy efficient ALU design using capacitance scaling [6], clock gating [7] and LVCDCI I/O Standard [8]. Design of Arithmetic logic unit exclusively for image processing operations is part of application specific processor design projects [9]. In this work, we are extending our work from LVDCI [8] I/O standard to LVCMOS I/O standard in order to achieve energy efficiency. Here, we are operating our design with the highest speed supported by the 4th generation i7 processor i.e. 4 GHz (4790K) to the lowest speed 2.9 GHz (4610Y). Earlier LVCMOS was used in energy efficient ALU but for 8-bit ALU architecture on 90nm FPGA, 64-bit ALU on 28nm FPGA [10], 8-bit ALU architecture on 28nm FPGA [12] and 8-bit ALU architecture on 40nm FPGA[13]. There was no work on energy efficient 32-bit ALU architecture using LVCMOS I/O standard. Here, 40nm FPGA is used, we will use 90nm, 65nm and 28nm FPGA in future for 32-bit project on FPGA. There are similar 16-functions in this ALU as in other ALU [10, 12-13] design by our other research group. ALU is indispensable components of CPU that can be part of a programmable reversible computing device such as a quantum computer [14].

Table 1: The Latest i7 Processor [9-10]

i7 Processor	Frequency (GHz)	#f Cores
4610Y	2.9	4
4600U	3.3	2
4600M	3.6	2
4960HQ	3.8	2
4790K	4.0	4

In section 2-3, we are analyzing dynamic Power dissipation with different LVCMOS along with different frequencies. In section 4, we discuss the conclusion of this project. In section 5, we discuss the future scope of this projects. Clock power, Logic power, Signal power and IO power are major contributor in dynamic power dissipation.

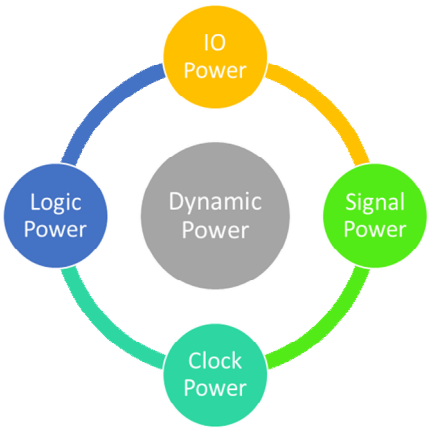

Figure 2: Components of Dynamic Power Dissipation

In this ALU, we are using LVCMOS I/O Standard in order to make energy efficient ALU and avoid transmission line reflection by matching the impedance of input port, output

port, transmission line used for input and output, device and intermediate signal.

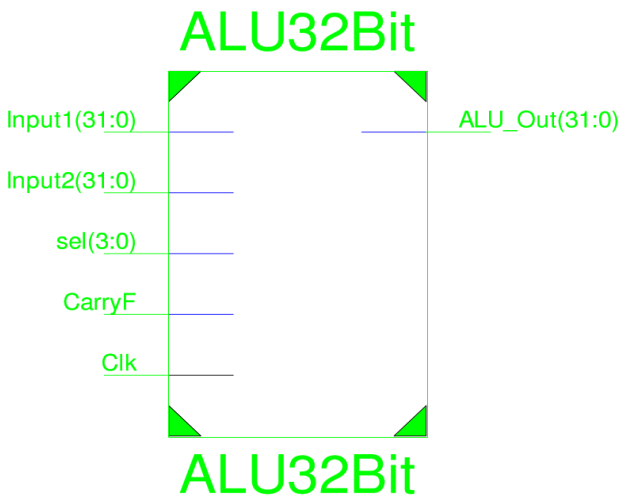

Figure 2: Schematic of Energy Efficient 32 bit ALU

There are 2 inputs and one output. In this 32-bit ALU design, there are 4 bit selection signal which covers 16 arithmetic and logic functions as shown in Figure 2.

II. Low Voltage Complimentory Metal Oxide Semiconductor

LVCMOS is energy efficient IO standards in compare to other energy efficient I/O standard like LVDCI, HSTL, SSTL, MOBILE DDR, and LVTTL and others too. There are five different type of LVCMOS IO standard on FPGA. These are LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25 and LVCMS33. LVCMOS12 is not available on 90nm FPGA. LVCMOS33 is only available in 28nm 7-series FPGA. Rest LVCMOS are available among 90nm, 65nm, 40nm and 28nm FPGA. FPGA is Field Programmable Gate Array. All power are measured in Watt (W). In the analysis our focus is on Clock power, Logic power, Signal power and I/O power dissipation by our 32-bit ALU design on FPGA.

A. Dyanamic Power With LVCMOS12 I/O Standard

Table 2: Power Dissipation with LVCMOS12

Power→ Frequency↓	Clock	Logic	Signal	IO
1GHz	0.022	0.011	0.017	1.184
2.9GHz	0.064	0.032	0.050	4.713
3.3GHz	0.073	0.036	0.057	5.363
3.6GHz	0.080	0.040	0.062	5.850
3.8GHz	0.084	0.042	0.066	6.175
4.0GHz	0.089	0.044	0.069	6.5

When there is no demand of peak performance, then we can save 75.28% clock power, 75% logic power, 75.36% signal power, 81.78% I/O power by operating our device with 1GHz frequency in place of 4GHz as shown in Table 2 and Figure 3.

We are operating our ALU with operating frequency of 2.9GHz, 3.3GHz, 3.6GHz, 3.8GHz and 4.0GHz as shown in Table 2-5 and Figure 3-6.

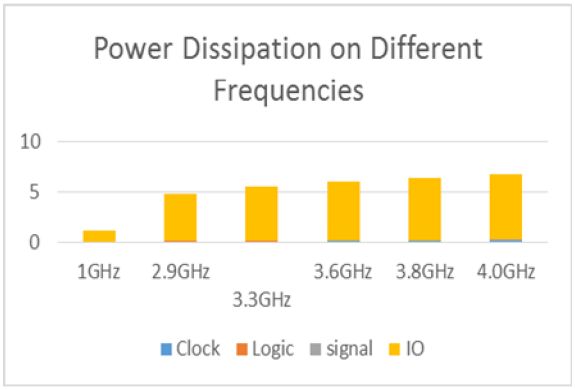

Figure 3: Power versus Frequency with LVCMOS12 I/O Standard.

B. Dyanamic Power With LVCMOS15 I/O Standard

Table 3: Power Dissipation with LVCMOS15

Power→ Frequency↓	Clock	Logic	Signal	IO
1GHz	0.022	0.011	0.017	1.811
2.9GHz	0.064	0.032	0.050	7.224
3.3GHz	0.073	0.036	0.057	8.220
3.6GHz	0.080	0.040	0.062	8.967
3.8GHz	0.084	0.042	0.066	9.465
4.0GHz	0.089	0.044	0.069	9.964

The reference voltage of LVCMOS is 1.5V. Using LVCMOS15 input/output standard, we are operating our device with speed of 1-4 GHz. When there is no demand of peak performance, then we can save 75.2% clock power, 75% logic power, 75.36% signal power, 81.82% I/O power by operating our device with 1GHz frequency in place of 4GHz as shown in Table 3 and Figure 4.

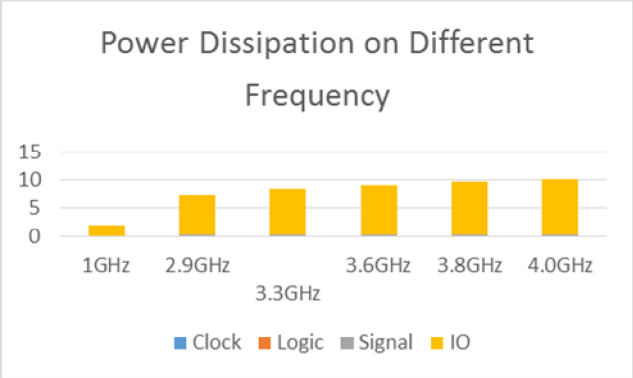

Figure 4: Power versus Frequency with LVCMOS15 I/O Standard.

C. Dyanamic Power With LVCMOS18 I/O Standard

Table 4: Power Dissipation with LVCMOS18

Power→ Frequency↓	Clock	Logic	Signal	IO

1GHz	0.022	0.011	0.017	2.383
2.9GHz	0.064	0.032	0.050	9.509
3.3GHz	0.073	0.036	0.057	10.820
3.6GHz	0.080	0.040	0.062	11.804
3.8GHz	0.084	0.044	0.069	12.460
4.0GHz	0.089	0.044	0.069	13.115

When we change the frequency from 4GHz to 2.9GHz , then there is 75.28% change in clock power, 75% change in logic power, 75.36% change in signal power, 81.82% chang e in I/O power as shown in Table 4 and Figure 5. Here, the reference voltage of LVCMOS is 1.8V. IO power is the highest among all component of dynamic power.

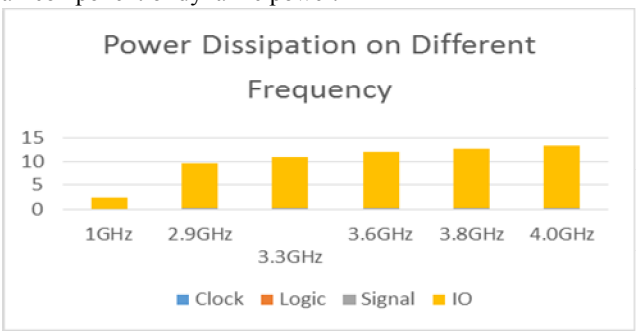

Figure 5: Power Dissipation versus Frequency with LVCMOS18 I/O Standard

D. Dyanamic Power with LVCMOS25 I/O Standard

Table 5: Power Dissipation with LVCMOS25

Power→ Frequency↓	Clock	Logic	Signal	IO
1GHz	0.022	0.011	0.017	3.888
2.9GHz	0.064	0.032	0.050	15.5311
3.3GHz	0.073	0.036	0.057	17.673
3.6GHz	0.080	0.040	0.062	19.280
3.8GHz	0.084	0.042	0.066	20.351
4.0GHz	0.089	0.044	0.069	21.422

When we change the frequency from 4GHz to 3.3GHz , then there is Change in 75.28% clock power, 75% logic power, 75.36% signal power, 81.85% I/O power as shown in Table 5 and Figure 6.

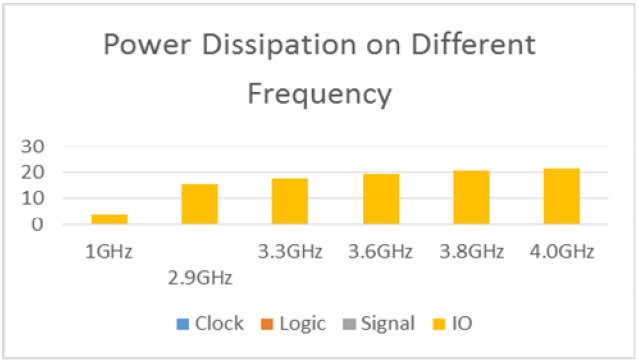

Figure 6: Power versus Frequency with LVCMOS I/O Standard.

III. POWER ANALYSIS OF 32-BIT ALU

Here, we are analyzing power with varition in LVCMOS on same frequency. Here, we observe that LVCMOS12 is the lowest power consumer and LVCMOS25 is the highest power consumer.

A. When Device operaring Frequency is 1GHz

Table 6: Power Dissipation with Different LVCMOS

LVCMOS→ Power↓	LVCMOS12	LVCMOS15	LVCMOS18	LVCMOS25
Clock	0.022	0.022	0.022	0.022
Logic	0.011	0.011	0.011	0.011
Signal	0.017	0.017	0.017	0.017
IO	1.184	1.811	2.383	3.388

When we use different classes of LVCMOS, then there is no change in clock power, logic power and signal power but LVCMOS25 having 65.05%, 46.61%, 29.66% more I/O power consumption with respect to LVCMOS12, LVCMOS15, LVCMOS18 respectively at 1 GHz as shown in Table 6 and Figure 6.

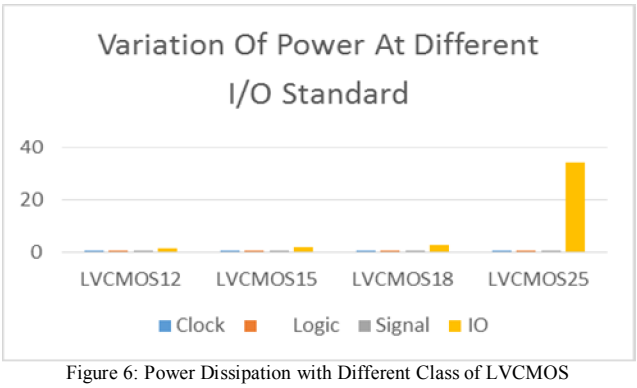

Figure 6: Power Dissipation with Different Class of LVCMOS

1 GHz is our initial criterion to deal with the condition when there is no peak performance demand from CPU. In next section, we are going to operate our 32-bit design with the available highest operating speed of 4th generation i7 processor. The maximum operating frequency of 4610Y, 4600U, 4600M, 4960HQ, 4790K is 2.9 GHz, 3.3 GHz, 3.6 GHz, 3.8GHz and 4.0 GHz respectively [9].

B. When Device operating Frequency is 2.9 GHz

Table 7: Power Dissipation with Different LVCMOS

LVCMOS→ Power↓	LVCMOS12	LVCMOS15	LVCMOS18	LVCMOS25
Clock	0.064	0.064	0.064	0.064
Logic	0.032	0.032	0.032	0.032
Signal	0.050	0.050	0.050	0.050
IO	4.713	7.224	9.509	15.531

There is no change in clock power, logic power and signal power but LVCMOS25 having 69.65%,53.48%,38.77% more I/O power consumption than LVCMOS12, LVCMOS15, LVCMOS 18 respectively at 2.9GHz as shown in Table 8 and Figure 8.

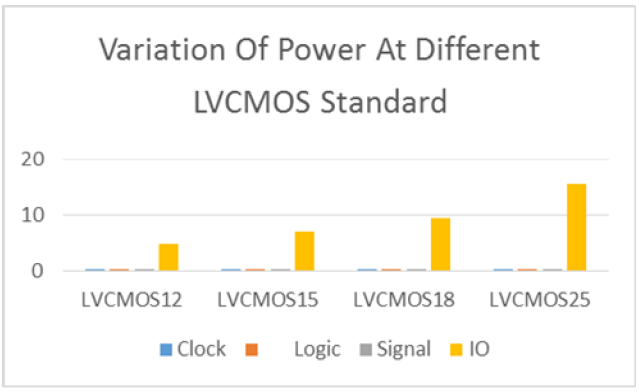

Figure 8 : Power Dissipation with Different LVCMOS

C. *When Device operating Frequency is 3.3 GHz*

Table 9: Power Dissipation with LVCMOS

LVCMOS→ Power↓	LVCMOS12	LVCMOS15	LVCMOS18	LVCMOS25
Clock	0.073	0.073	0.073	0.073
Logic	0.036	0.036	0.036	0.036
Signal	0.057	0.057	0.057	0.057
IO	5.363	8.220	10.820	17.673

When we are using different classes of LVCMOS, then there is no change in clock power, logic power and signal power but LVCMOS25 having 69.65%, 53.48%, 37.07% more I/O power consumption with respect to LVCMOS12, LVCMOS15, LVCMOS18 respectively at 2.9GHz as shown in Table 9 and Figure 9.

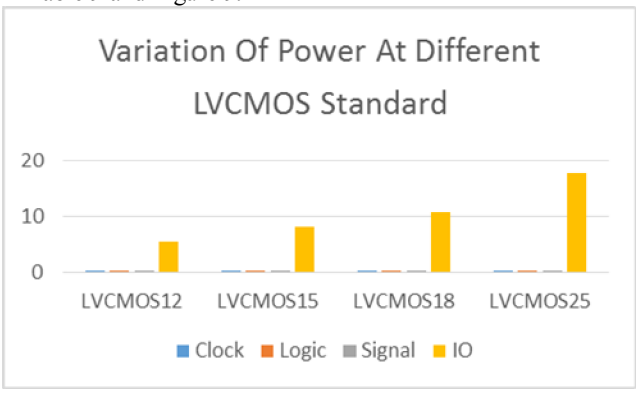

Figure 9: Power Dissipation with Different Classes of LVCMOS

D. *When Device operating Frequency is 3.6 GHz*

Table 10: Power Dissipation with Different LVCMOS

LVCMOS→ Power↓	LVCMOS12	LVCMOS15	LVCMOS18	LVCMOS25
Clock	0.080	0.080	0.080	0.080
Logic	0.040	0.040	0.040	0.040
Signal	0.062	0.062	0.062	0.062
IO	5.850	8.967	11.804	19.280

When we use different classes of LVCMOS, then there is no change in clock power, logic power and signal power but LVCMOS25 having 69.65%, 53.49%, 38.77% more I/O power consumption with respect to LVCMOS12, LVCMOS15, LVCMOS 18 respectively at 2.9GHz as shown in Table 10 and Figure 10.

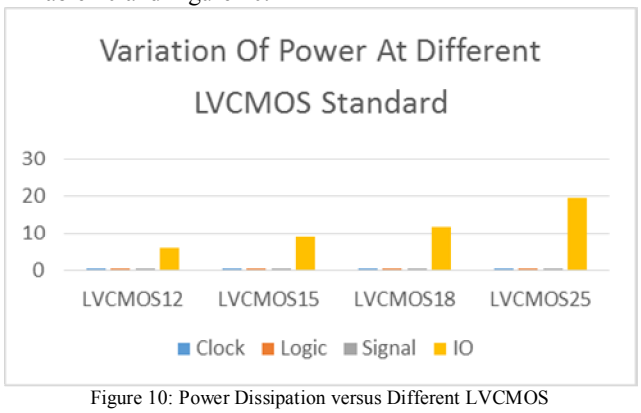

Figure 10: Power Dissipation versus Different LVCMOS

E. *When Device operating Frequency is 3.8 GHz*

Table 11: Power dissipation With Different LVCMOS

LVCMOS→ Power↓	LVCMOS12	LVCMOS15	LVCMOS18	LVCMOS25
Clock	0.084	0.084	0.084	0.084
Logic	0.042	0.042	0.042	0.042
Signal	0.066	0.066	0.066	0.066
IO	6.175	9.465	12.460	20.351

When we use different classes of LVCMOS, then there is no change in clock power, logic power and signal power but LVCMOS25 having 69.65%, 53.49%, 38.77% more I/O power consumption with respect to LVCMOS12, LVCMOS15, LVCMOS 18 respectively at 2.9GHz as shown in Table 11 and Figure 11.

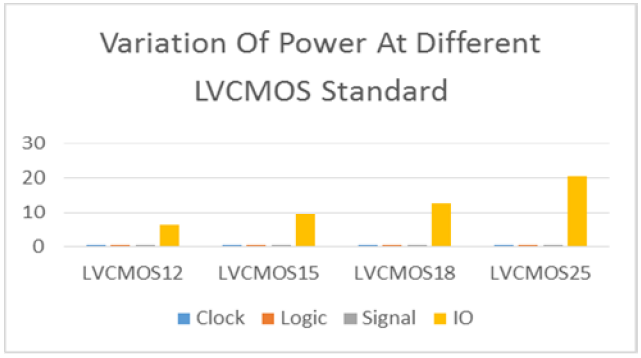

Figure 11: Power Dissipation with Different Class of LVCMOS

F. *When Device operating Frequency is 4.0 GHz*

Table 12: Power Dissipation With Different LVCMOS

LVCMOS→ Power↓	LVCMOS12	LVCMOS15	LVCMOS18	LVCMOS25
Clock	0.089	0.089	0.089	0.089
Logic	0.044	0.044	0.044	0.044
Signal	0.069	0.069	0.069	0.069
IO	6.500	9.964	13.115	21.422

When we use different classes of LVCMOS, then there is no change in clock power, logic power and signal power but LVCMOS25 having 69.96%, 53.48%, 38.77% more I/O

power consumption with respect to LVCMOS12, LVCMOS15, LVCMOS 18 respectively at 2.9GHz as shown in Table 12 and Figure 12.

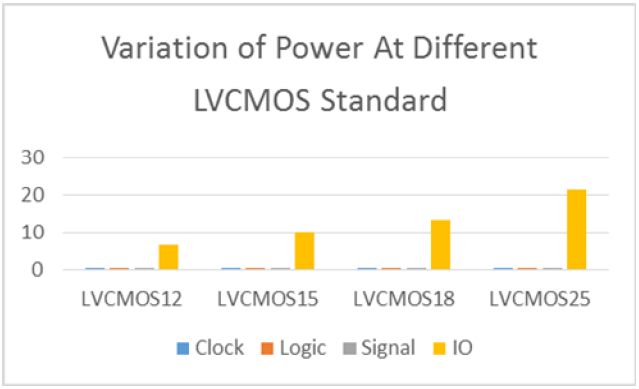

Figure 12: Power Dissipation Versus Different LVCMOS

IV. Conclusion

In our conclusion, what all we have studied in our research is by using LVCMOS, that it made a major difference in power dissipation. By applying different classes of LVCMOS, we have seen various variations in power in terms of clock, IO's, logic and signals. By using LVCMOS, we have also seen that we are getting good energy efficiency in terms of power. Besides, we observed that 69% IO power reduction with LVCMOS12, 53% IO power reduction with LVCMOS15 and 38% reduction with LVCMOS18 in compare to I/O power dissipation with LVCMOS25. Last but not the least, our research results in that it is fully compatible with exclusive 4th generation i7 microprocessor as it able to run with such various sort of frequencies (2.9, 3.3, 3.6, 3.8, 4.0GHz) so well. LVCMOS12 is the lowest power consumer and LVCMOS25 is the highest power consumer.

V. Future Scope

The future scope of our research, is that we are going to take a good use of other IO's standards like HSTL, SSTLLVDCI, and HSUL and so on. In order to make it more energy efficient. Like we worked on 32 bit ALU recently, so after this we will try to work on 64 bit, 128 bit and 256 bit upcoming. By using virtex-6, we achieved 38% to 69% power reduction. Likewise, in future with the help of using new technology based FPGA such as Kintex-7 FPGA, Airtex-7, we will get the high performance, good energy efficiency and portability as well. In future, this ALU architecture may re-design for programmable reversible computing device such as a quantum computer.

References

[1] M. Ramalatha, K.D. Dayalan, P. Dharani, & S.D. Priya, "High speed energy efficient ALU design using Vedic multiplication techniques", . International Conference on Advances in Computational Tools for Engineering Applications (ACTEA'09), pp. 600-603, 2009.

[2] S. Agarwal, V.K. Pavankumar, R. Yokesh., "Energy-efficient, high performance circuits for arithmetic units", *21st International Conference on VLSI Design, pp. 371-376, 2008.*

[3] D. Coleman and J. Di, "Analysis and Improvement of Delay-Insensitive Asynchronous Circuits Operating in Subthreshold Regime", Journal of Low Power Electronics, Volume 6, Number 2, pp. 320-324, 2010.

[4] M. Daumas, C. Finot, "Division of Floating Point Expansions with an Application to the Computation of the Determinant", Journal of Universal Computer Science, Vol. 1 No.6, pp 323-338, June 1999.

[5] R. Shalem, E. John, and L.K. John, "A novel low-power energy recovery full adder cell", Great Lakes Symposium on VLSI, pp.380-383, 1999.

[6] T. Kumar, Sweety, S.M.M. Islam, B. Pandey and T. Das, "Energy Conversion in 64-Bit ALU Design on FPGA Using Mechanics of Capacitance", International Journal of Current Engineering and Technology (IJCET), ISSN:2277–4106, 2347-5161(print), Special Issue-3 (April 2014).

[7] B. Pandey and M. Pattanaik, "Clock Gating Aware Low Power ALU Design and Implementation on FPGA", International Journal of Future Computer and Communication (IJFCC), Vol.2, No.5, pp. 461-465, October 2013, ISSN: 2010-3751.

[8] T. Das, B. Pandey, M.H. Minver, T. Kumar, "LVDCI I/O standard based green image ALU design on ultra scale FPGA", 8th IEEE International Conference on Industrial and Information Systems (ICIIS), 2013.

[9] Specification of 4th Generation Intel i7 Processor,www.intel.in.

[10] B.S Chowdhry, B. Pandey, T. Kumar, T. Das, "Mobile DDR IO Standard Based High Performance Energy Efficient Portable ALU Design on FPGA", **Springer** Wireless Personal Communications, An International Journal, Vol. 76, Issue 3, pp. 569-578, 2014.

[11] L. Vokorokos, J. Trelová, & N. Ádam, "Sequential Threads In Data Flow Computers", International Conference on Applied Electrical Engineering and Informatics, 54-58, 2010.

[12] B. Pandey, J. Yadav, M. Pattanaik, "IO Standard Based Energy Efficient ALU Design and Implementation on 28nm FPGA", 10th IEEE India Conference (INDICON) 2013, IIT Bombay, 13th-15th December 2013.

[13] B. Pandey, J. Yadav, Y. Singh, R. Kumar, S. Patel, "Energy Efficient Design and Implementation of ALU on 40-nm FPGA", IEEE International Conference on Energy Efficient Technologies for Sustainability-(ICEETs), Kanykumari, pp.45-50, 2013.

[14] Y. Syamala, and A. V. N. Tilak. "Reversible Arithmetic Logic Unit", 3rd International Conference on Electronics Computer Technology, 2011.