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Compact Electro-Thermal Modeling of a SiC MOSFET Power Module under Short-Circuit Conditions

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***Abstract* – A novel physics-based, electro-thermal model which is capable of estimating accurately the short-circuit behavior and thermal instabilities of silicon carbide MOSFET multi-chip power modules is proposed in this paper. The model has been implemented in PSpice and describes the internal structure of the module, including stray elements in the multi-chip layout, self-heating effect, drain leakage current and threshold voltage mismatch. A lumped-parameter thermal network is extracted in order to estimate the internal temperature of the chips. The case study is a half-bridge power module from CREE with 1.2 kV breakdown voltage and about 300 A rated current. The short-circuit behavior of the module is investigated experimentally through a non-destructive test setup and the model is validated. The estimation of overcurrent and temperature distribution among the chips can provide useful information for the reliability assessment and fault-mode analysis of a new-generation SiC high-power modules.**

Keywords—silicon carbide; power MOSFET; modeling; short-circuit

NOMECLATURE

A	Device chip area (cm^2).
c	Specific thermal capacity (J/K)
E_g	Band-gap energy (J)
ε_s	Semiconductor dielectric constant (F/cm)
I_{g_th}	Generation leakage current (A).
k_B	Boltzmann's constant (J)
λ	Thermal conductivity (W/(cm·K))
n_i	Carrier concentration (cm^{-3}).
N_c	Number of conduction states.
N_v	Number of valence states.
N_d	Drift doping concentration (cm^{-3}).
N_a	P-well doping concentration (cm^{-3}).
ρ	Density ($kg \cdot cm^{-3}$)
τ_g	SRH generation lifetime (s).
V_{DC}	DC bus voltage (V).

I. INTRODUCTION

The recent improvements in the manufacturing technology of wide bandgap (WBG) semiconductors has led to the development of a new generation of power electronic devices based on such materials [1]. In particular, the silicon carbide (SiC) material shows a number of attractive physical properties which allow the design of high-power-density, fast-switching devices and capable of operating at high temperature with increased efficiency in comparison to their silicon-based counterparts [2], [3]. SiC MOSFETs and diodes are becoming more and more popular in those power applications in which low weight, high efficiency and ruggedness to harsh environment are required [4]. Most of the research is currently focused on the design of compact high-power, multi-chip modules based on SiC devices in order to scale

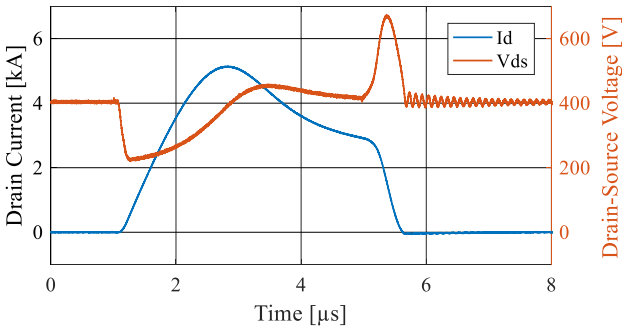

Fig. 1. Measured single-pulse short-circuit test: 4 µs pulse with 400 V V_{DC} at room temperature.

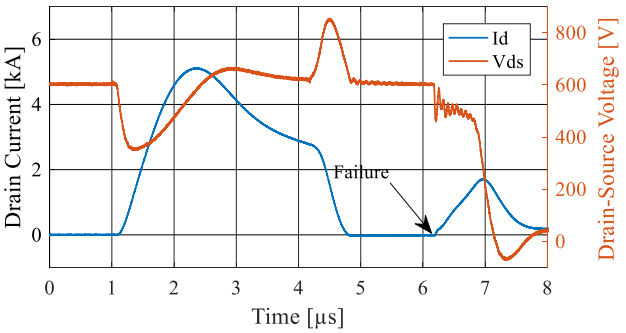

Fig. 2. Measured single-pulse short-circuit test: failure with 600 V V_{DC} at room temperature.

up the power [5]. A great challenge lies in the design of module packaging that can truly exploit the enhanced thermal and electrical performance of SiC devices, withstanding high-temperature operation (150-200 °C) and built in order to reduce the impact of stray elements. So far, a number of high power all-SiC MOSFET (also including SiC JBS as freewheeling diodes) modules are commercially available, with a breakdown voltage up to 1700 V and a rated current of about 300 A.

Nevertheless, the reliability evaluation and fault-mode analysis, as well as the availability of compact physics-based models, is still quite scarce for these modules, which in fact hinder their use in the design of power converters. The short circuit (SC) capability and robustness of discrete SiC MOSFETs have been extensively investigated [6]–[8] and modeled [9], while an assessment of the SC safe operating area for 1.2 kV modules is available in [10]. A number of compact behavioral and physical based models are available for discrete SiC MOSFETs and diodes [11], [12]. For example in [13] and [14] such models have been applied for multi-chip modules, while others have tried to investigate the behavior of parallel-connected chips e.g. in [15] and [16].

This work is focused on combining these contributions in a novel compact and physics-based model. The model is capable of describing the electrical and thermal behavior of the module, accounting for its internal layout and stray elements, as well as estimating the current sharing and temperature distribution among the chips under short-circuit occurrence. A 1.2 kV-300 A power module from CREE has been investigated as case study [17]. Single-pulse SC tests have already been carried out on modules of the same type, resulting in different kinds of failure [10]. The model has been implemented in PSpice and the simulation results are compared with experiments.

II. SiC Power MOSFET Short-Circuit Behavior

The short-circuit robustness is a key factor in the reliability of power devices. SiC MOSFETs thermal instabilities are studied in [18]. The studies in [10], [11] and [17] have shown how SiC devices and modules still exhibit a rather low capability to withstand short-circuit

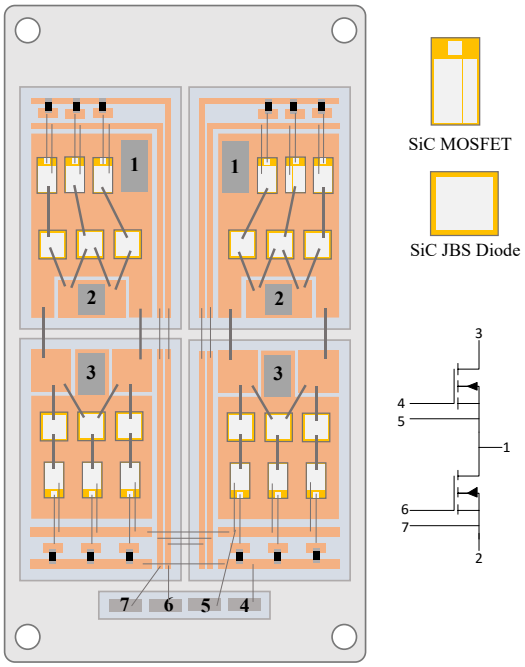

Fig. 3. Internal layout of the 1.2 kV-300 A CREE half-bridge power module. JBS: Junction Barrier Schottky.

for the nominal requirement of 10 µs, especially under repetitive stress conditions. The typical short-circuit behavior of a SiC power MOSFET is shown in Fig. 1, where a single 4 µs pulse is applied to a module operating with 400 V DC-bus voltage. The measurements have been carried out with the non-destructive test setup which is presented in [10]. The drain current increases rapidly, only limited by the stray inductance of the power loop, until the device operates in the channel saturation region. As the high SC energy is released in the dies, the junction temperature increases due to self-heating and the MOS channel and drift region electron mobility drops. Thus, the current presents a negative slope. If the temperature remains within the safe operating range the device can be turned off successfully. However, it can be observed in Fig. 2 that the device fails when the DC-bus voltage is increased up to 600 V. For a 3 µs pulse, and approximately

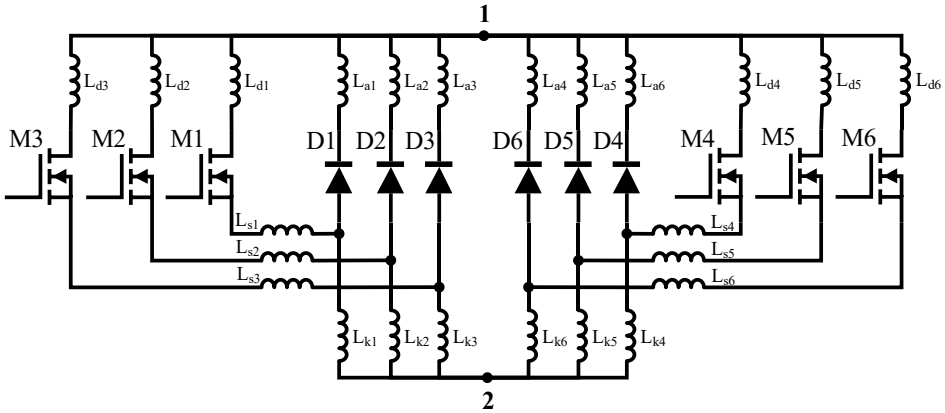

Fig. 4. Equivalent circuit for the bottom side of the half-bridge module (gate circuit not included) as shown in Fig. 3

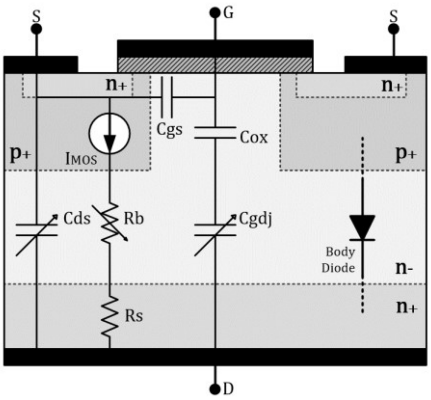

Fig. 5. SiC MOSFET model structure.

1.5 µs after turn off, the module presents a typical thermal runaway failure. The literature attributes this kind of failure, often occurring with some delay after turn off, to the rapid increase of the leakage current, due to thermal generation of minority carriers, eventually leading to the destruction of the device.

III. Electrical Model of SiC MOSFET

The internal structure of the 1.2 kV half-bridge module is sketched in Fig. 3. Six power MOSFET dies are paralleled with six JBS diode dies both at the top and in the bottom part of the leg. The devices are distributed among four direct bonded copper (DBC) substrate pads with 3 MOSFETs and 3 diodes. An asymmetrical circuit layout can have significant effects on the current sharing among the parallel-connected devices, as observed in [14] and [16]. An estimation of the stray elements has been made in order to obtain an equivalent circuit. The length of the bond-wires and of the DBC current paths have been considered when sizing the stray inductors. The lower side DUT has been used for the short-circuit test, and its equivalent circuit is drawn in Fig. 4.

The electrical model for the MOSFET die is based on the one presented in [19] and its structure is shown in Fig. 5. Several parameters in the model (gate threshold, carrier mobility, transconductance) are temperature-dependent. A datasheet-based parameter identification has been carried out, since the single chip could not be tested separately (the model takes into account each of the dies individually). A modified PSpice diode model has been used for the JBS chips, which actually have a minor role in the SC event, apart from increasing the overall parasitic capacitance. The temperature-dependent leakage current has been included in the model, according to the Shockley-Read-Hall (SRH) generation theory, by the following equation [7]:

$$I_{g\_th} = \frac{q\,A\,n_i}{\tau_g}\sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_d+N_a}{N_d\,N_a}\right)V_{DC}} \qquad (1)$$

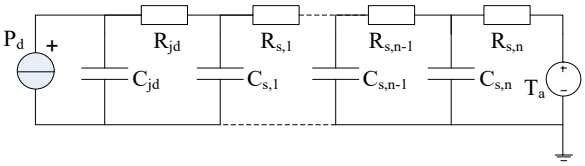

Fig. 6. Cauer-type thermal network used to estimate the junction temperature during short-circuit.

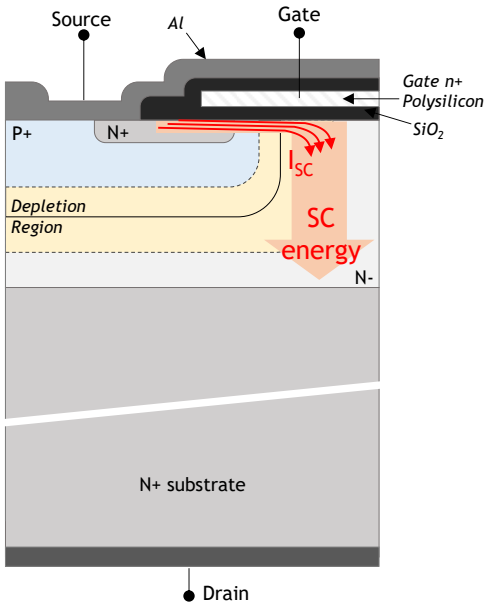

Fig. 7. Vertical cross-section view of the cell and heat spreading direction during the short circuit (not in scale).

Where τ_g is the SRH generation lifetime, A is the semiconductor area, N_d and N_a are respectively the doping density in the N-drift and the P- well region. The leakage current temperature dependency is included in the carrier concentration n_i as:

$$n_i = \sqrt{N_c\,N_v}\cdot e^{-\frac{E_g}{2k_BT}} \qquad (2)$$

Where T is the junction temperature of the device, N_c is the number of conduction states, N_v is the number of valence states and E_g is the bandgap energy.

IV. Thermal Model

The thermal behavior of the module has been modeled by means of a lumped impedance thermal network. A Cauer-type thermal network is available from the model provided by the manufacturer. It accounts for the self-heating of the single chip by dividing the drift and substrate regions in a number of equally thick layers, modelled by a chain of RC-elements, as shown in Fig. 6. The same method was used and validated in [20]. The thermal network coefficients for the drift region can be

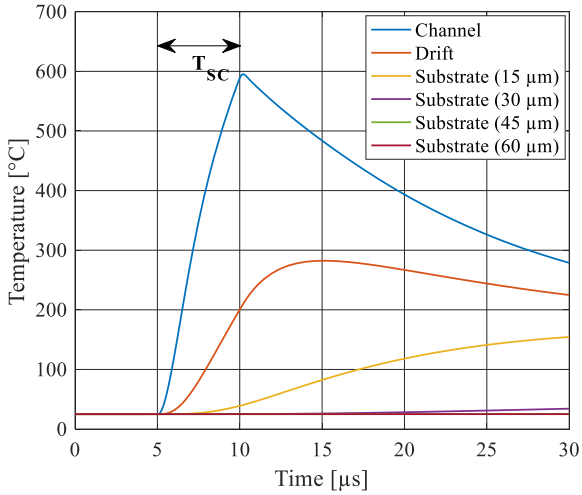

Fig. 8. Simulated temperature during short circuit for different layers of the chip (using a Cauer thermal network as in Fig. 6).

obtained as each element can be obtained by means of the following equations:

$$R_{jd} = \frac{1}{\lambda} \cdot \frac{d_{jd}}{A} \tag{3}$$

$$C_{jd} = c \cdot \rho \cdot d_{jd} \cdot A \tag{4}$$

Where d_{jd} is the thickness of the drift region, c is the specific heat capacity, λ is the thermal conductivity and ρ the density for 4H-SiC material. The thermal network coefficients for each of the n equivalent RC elements of the substrate can instead be obtained by:

$$R_{s,n} = \frac{1}{\lambda} \cdot \frac{d_{chip} - d_{jd}}{(n-1) \cdot A} \tag{5}$$

$$C_{s,n} = c \cdot \rho \cdot A \cdot \frac{d_{chip} - d_{jd}}{(n-1)} \tag{6}$$

Where d_{chip} is the thickness of the chip.

Moreover, the short duration of the short circuit event (few µs) leads to some assumptions for the thermal model. In the first place, because of the time constant in the thermal conductivity of the chip material, the huge amount of heat generated by the short circuit current will not reach the lower substrate layers before some milliseconds. This means that the base-plate temperature can be considered as constant and equal to the ambient temperature. The short circuit energy is actually only released in the channel and drift regions, as depicted in Fig. 7. A simulated temperature transient using the Cauer-network model is shown in Fig. 8. It is clear that, within the SC time, the heat does not propagate further than few tens of µm through the substrate, which is around 180 µm thick for these devices. This leads to a negligible temperature increase in the layers underneath. Moreover, the distance between the dies is long enough to neglect the cross-coupling thermal effects [21]. The module is also considered adiabatic from the top and lateral surfaces, for simplicity. Therefore, the resulting thermal network will be one-dimensional and all the heat is assumed to flow from the die downwards.

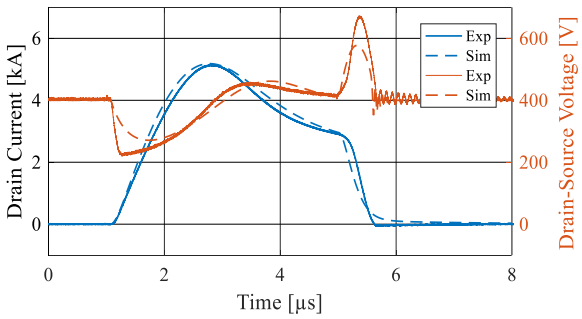

Fig. 9. Comparison of the simulated SC waveforms with the experimental results: 5 µs pulse at 400 V.

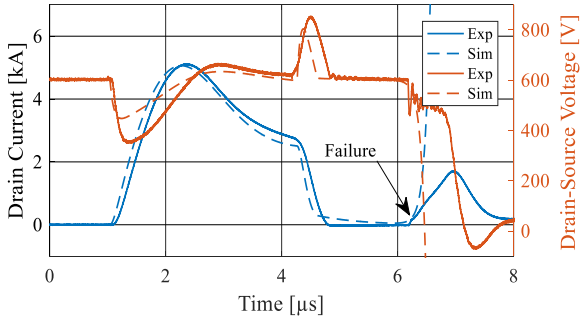

Fig. 10. Comparison of the simulated SC waveforms with the experimental results: 3 µs pulse at 600 V.

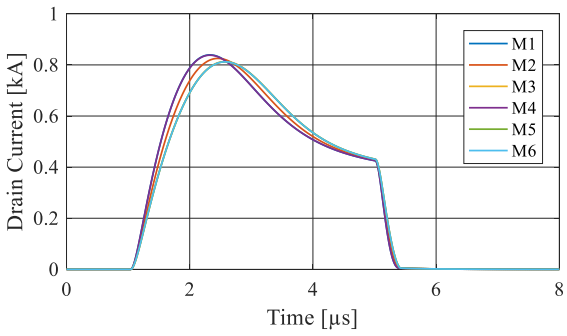

Fig. 11. Simulated drain current sharing among the dies without failure.

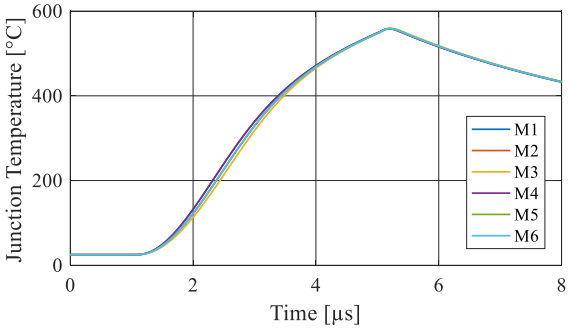

Fig. 12. Simulated junction temperature in each chip without failure.

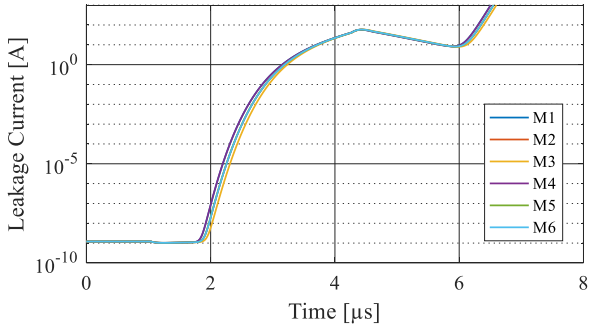

Fig. 13. Simulated evolution of the drain leakage current in each chip during failure.

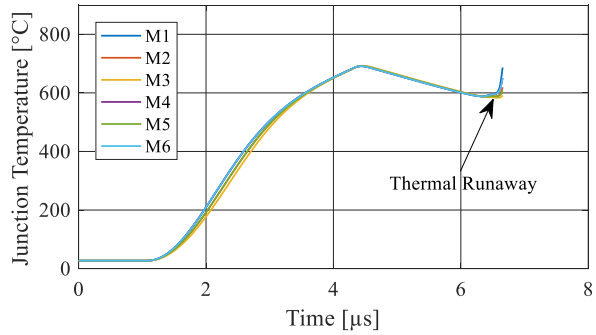

Fig. 14. Simulated evolution of the junction temperature in each chip during failure.

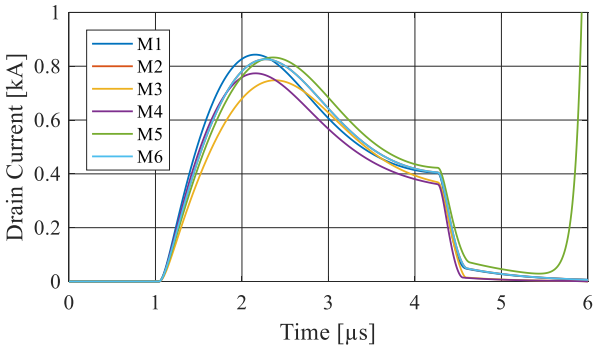

Fig. 15. Influence of gate threshold voltage mismatch (20%) on the current sharing among paralleled chips during SC.

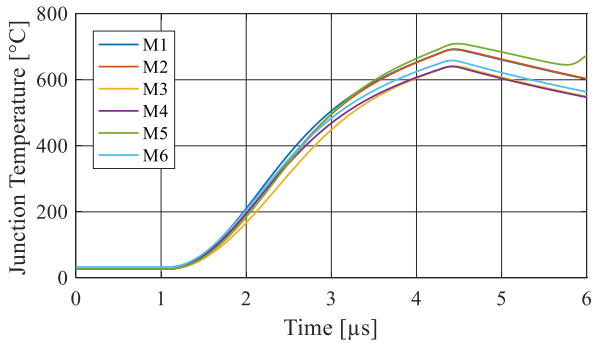

Fig. 16. Influence of gate threshold voltage mismatch on the temperature distribution among paralleled chips during SC.

V. Simulation Results and Model Validation

The results from the PSpice simulation are compared to the aforementioned SC test waveforms shown in Fig. 9 and 10. The model shows a good capability in estimating the real SC behavior and can approximately emulate the failure mode due to the increase of the leakage current. Most important is the fact that the temperature dependency is correctly estimated, showing the fast degradation of the carrier mobility due to self-heating and, at the same time, validating the chosen thermal model. The simulation also offers an insight into what happens inside the module. The current sharing among the dies is shown in Fig. 11 and the respective junction temperature distribution is plotted in Fig. 12. In this case, the applied DC-bus voltage is 400 V and the leakage current does not increase enough to determine instability (the temperature stays within the safety range). Nevertheless, it is worth pointing out how the different slopes in the current waveforms are due to the different stray inductances in the current path This also influences in a minor way the temperature increase.

Fig. 13 shows the evolution of the leakage current, whereas Fig. 14 shows the junction temperature for each of the MOSFET dies. In this case the applied DC bus voltage is 600 V and the temperature increase is larger than in the previous case. Eventually, an instability condition is reached and two of the chips start the thermal runaway process, which leads to failure. This also mainly depends on the module layout and the current sharing among the chips. Due to the exponential increase of the current, the simulation fails to converge at this point.

In order to understand the influence of the device internal parameter mismatch on the failure process, the gate threshold voltage has been varied for different chips up to 20% of the rated value. Such a variation is clearly observable in real MOSFETs when a characterization of different components with the same part number is performed [16], [22], [23]. The device with the lowest threshold voltage is bound to share more SC current than the other chips and it is often the one leading the whole module to failure. This can be observed in Fig. 15 and Fig. 16, where only M5, with the lowest voltage thresholds, triggers the thermal runaway. This mismatch effect appears to be way more critical than the one due to stray inductance.

VI. Conclusions

This novel PSpice electro-thermal model is capable to estimate with rather good accuracy the shot-circuit behavior of a 1.2 kV power MOSFET module, including failure mode due to thermal runaway. This is an original and unique feature for this kind of circuit-based models. An estimation of the junction temperature by means of a thermal network successfully allows the simulation of the current-capability degradation during SC. Moreover, the model has been implemented in a compact PSpice format and features fast simulation time, in the order of few

elements on both normal and abnormal operation can lead to improvements in the module layout design. In addition, the influence of manufacturing mismatches among the paralleled chips has been pointed out. The development and implementation of such models represents a useful tool for both the design of SiC-based converters and the reliability evaluation of SiC power modules. The model will soon be available at [24].

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