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Constant Power Load Instability Mitigation in DC Shipboard Power Systems Using Negative Series Virtual Inductor Method

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***Abstract*—DC distribution technology has become the new choice and the trending technology of shipboard power systems for its advancement over its AC counterpart. In DC shipboard power systems, the bus voltage stability is a critical issue. The presence of tightly controlled high-power constant power load can induce system-level voltage instability. To mitigate such a problem, a novel compensation method based on model-derived specially designed negative virtual inductance loop is proposed in this paper. The mechanism of the proposed method is presented in detail. In addition to that, the proposed compensation method is compliable with both voltage-controlled and droop-controlled converters. Simulations are carried out to validate the proposed method, and the results show enhanced stability margin and capability when feeding constant power loads.**

Keywords—All-electric ship; shipboard power system; constant power load; stability; virtual impedance.

I. INTRODUCTION

DC distribution technologies, especially in medium-voltage level (i.e. MVDC), have been considered as promising solution for future all-electric ships (AESs) [1-3]. While there are still advances in the AC solutions, DC distribution based solutions are expected to provide significant operational and economic benefits for future ships [2, 4, 5].

For DC shipboard power systems (SPSs), the system-level stability is a critical and challenging issue. As DC SPS is a typical example of power electronic based islanded power system, all the power generators and consumers are interfaced through power electronic converters (PECs). When acting as loads, the tightly controlled PECs have control bandwidth high enough to make the consumed power independent from the bus voltage variations, which is referenced as constant power load (CPL). When operating in DC systems, the CPLs will perform negative incremental resistance that decreases system damping, one step further, it can lead to bus voltage instability [6-7].

The study associated with CPL instability issue can be traced back to 1976, when the interaction among PECs and passive components was firstly analyzed in [8]. Extensive study of the CPL instability issue have been reported in [9-11]. At the same time, several approaches have been proposed to mitigate the CPL instability issue. In [12], passive damper design method is reported to mitigate CPL instability issue. In [13], active damping method is reported to solve the same problem. In [14] and [15] linearization via state feedback (LSF) method and corresponding parameter estimation method are introduced. In [16], loop-cancellation technique is reported to compensate CPL instability issue in automotive applications. At the same time, sliding mode control solution [17] and model predictive control solution [18] are also employed. However, considerable common problem of these non-linear methods is their sensitivity to the system parameter. It is also noteworthy that these methods are all designed for voltage control mode, droop control mode which is also a common grid-control method in MVDC SPS is not considered during their design procedure. In [19], linear quadratic regulator (LQR) is used to stabilize a droop-controlled system. In [20], more traditional virtual impedance method is implemented in droop-controlled DC microgrids with CPL instability issue. However, the virtual impedance based stabilizer presented in [20] is complex and it is divided into two branches connected in series to the output terminal and the DC capacitor, which require more efforts to implement in practical system.

In this paper, model-derived series virtual inductor method is proposed to mitigate CPL instability in DC SPSs. It differs from more conventional virtual impedance methods that the virtual inductor used in this paper is negative, instead of being positive, to cancel part of the intrinsic impedance of the PEC. The mechanism of CPL instability issue and proposed method are analyzed in the following parts of this paper. Simulations are carried out to validate the proposed method, the results show enhanced stability margin and capability of feeding CPLs.

II. CPL INSTABILITY ISSUE

A. Modeling Constant Power Load

For the constant power nature of tightly controlled PECs, the following expression will be satisfied within the control bandwidth of the controller:

$$i_{Load} = \frac{P_{Load}}{V_{dc}} \tag{1}$$

where V_{dc}, i_{Load}, and P_{Load} are the voltage, current and power of the CPL.

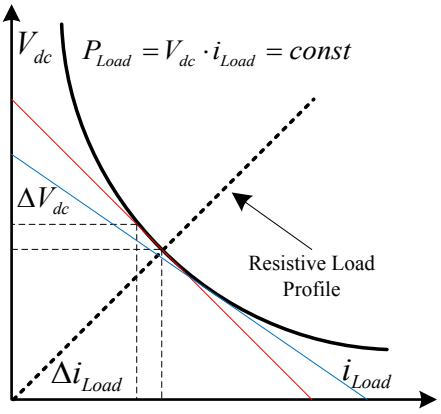


Fig. 1. Negative impedance behavior of CPLs.

As shown in Fig. 1, the incremental resistance of a CPL can be calculated by:

$$\frac{\partial V_{dc}}{\partial i_{Load}} = \frac{\partial}{\partial i_{Load}}\left(\frac{P_{Load}}{i_{Load}}\right) = -\frac{P_{Load}}{i^2_{Load}} = -\frac{V^2_{dc}}{P_{Load}} = R_{CPL} \qquad (2)$$

It indicates that the CPLs, although still consuming power, perform negative resistance in the system, which makes the system less damped and impacts the stability. A linearized equivalent circuit of a CPL can be derived from (2), which composed by the derived negative resistance and a controlled current source.

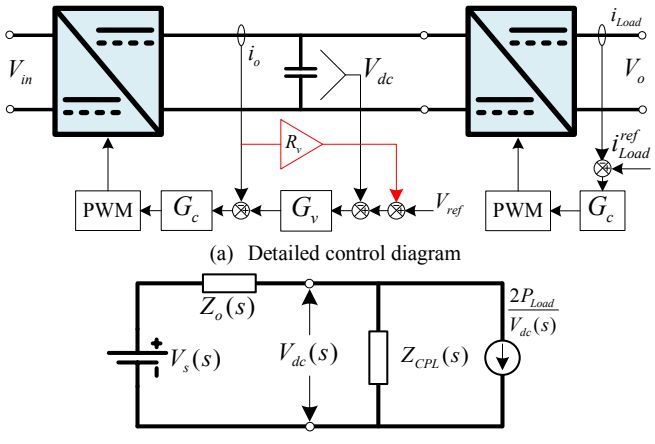


Fig. 2. Analytical circuit of CPL instability issue.

In addition to the negative resistance shown in (2), the limited control bandwidth of controller will perform additional frequency-dependent negative impedance characteristic in the frequency range above the controller's control bandwidth. In Fig. 2, the linearized analytical circuit of CPL instability issue is presented, in which the bus voltage is determined by:

$$V_{dc}(s) = \frac{V_s(s)Z_{CPL}(s)}{Z_o(s)+Z_{CPL}(s)} = \frac{V_s(s)}{T_m(s)}, T_m(s) = \frac{1}{1+Z_o(s)/Z_{CPL}(s)} \qquad (3)$$

where $V_s(s)$, $Z_o(s)$ and $Z_{CPL}(s)$ stand for source voltage, source-side output impedance and negative impedance of CPLs, all presented in frequency-domain transfer functions. $T_m(s)$ is the minor loop gain of the system, which is critical to the system stability analysis [8-11].

The sufficient condition of system stability is that all the dominant poles of $T_m(s)$ locate in the stable region. It requires the source-side output impedance to have smaller magnitude than the negative impedance, or at least fulfill the marginal stability condition. In Fig. 3, a generalized scenario of CPL stability issue is illustrated by bode diagram. Detail analysis and discussion on the source-side output impedance will be given in the following part of this paper.

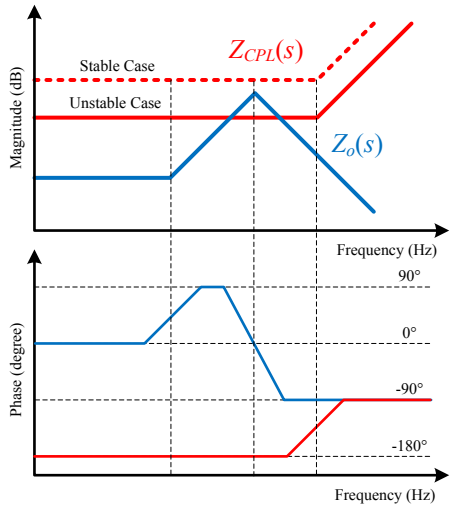


Fig. 3. Generalized frequency response of analytical circuit

B. Source-side Output Impedance: Voltage Control Mode

In Fig. 2(a), a generic control scheme for voltage control mode (VCM) and droop control mode (DCM) is illustrated. In this paper, conventional control architecture of PECs is used as the study case, in which PI controllers are used to regulate both voltage and current loops.

To analyzing the dynamic behavior of dual-loop controller, the inner current loop is commonly simplified as a first-order delay with a certain control bandwidth. Thus, the dynamic of DC-side output current in VCM can be descripted as:

$$I_o(s) = G_v(s)G_{clc}(s)\left[V_{ref}(s) - V_{dc}(s)\right] \qquad (4)$$

where $G_v(s)$ is the transfer function of voltage controller, $G_{clc}(s)$ is the simplified close-loop transfer function of the inner current loop.

Therefore, the source-side output impedance under VCM is calculated by:

$$Z_o(s) = Z_{con}(s) \| Z_c(s) = Z_{con}(s) \| \frac{1}{sC} \tag{5}$$

$$Z_{con}(s) = \frac{V_{ref}(s) - V_{dc}(s)}{I_o(s)} = \frac{1}{G_v(s)G_{clc}(s)} = \frac{1}{\frac{k(s+\alpha)}{s} \cdot \frac{\omega_c}{s+\omega_c}} \tag{6}$$

where $Z_{con}(s)$ stands for the inherent close-loop impedance of the PEC, C is the total capacitance in the DC bus. ω_c stands for the close-loop control bandwidth of the current loop, k is the proportional term of the voltage PI controller, and α presents the ratio of proportional and integral terms of the voltage PI controller.

From (5) and (6), an equivalent circuit can be derived to describe the dynamic of PEC, as shown in Fig. 4. Three virtual components are introduced, their parameters are shown as follow:

$$L_{d1} = \frac{1}{k\omega_c}, \quad L_{d2} = \frac{\omega_c - \alpha}{k\omega_c\alpha}, \quad R_d = \frac{\omega_c - \alpha}{k\omega_c}, \tag{7}$$

In Fig. 5, the derived frequency response of $Z_o(s)$, $Z_{con}(s)$, $Z_c(s)$ are illustrated. It can be seen from the bode diagram that the close-loop impedance $Z_{con}(s)$ under VCM is mostly inductive. When paralleled with DC capacitor, the output impedance $Z_o(s)$ got a peak near the intersection frequency.

C. *Source-side Output Impedance: Droop Control Mode*

From controller viewpoint, the main difference between DCM and VCM is the virtual resistance loop, which forms additional feedback loop to the controller. Similar to VCM, the dynamic of DCM controller can be descripted as:

$$I_o(s) = \frac{G_v(s)G_{clc}(s)}{1 + R_v G_v(s)G_{clc}(s)}\left[V_{ref}(s) - V_{dc}(s)\right] \tag{8}$$

where R_v stands for the virtual resistance, also named droop coefficient.

Thus, the close-loop impedance of converter under DCM will be:

$$Z_{con}(s) = \frac{1 + R_v G_v(s)G_{clc}(s)}{G_v(s)G_{clc}(s)} = R_v + \frac{1}{G_v(s)G_{clc}(s)} \tag{9}$$

It is seen from (9) that DCM have the same frequency-dependent impedance as VCM. In addition to that, the droop loop introduces an additional virtual resistor in series to the frequency-dependent impedance, as shown in Fig. 4(b).

In Fig. 6, the derived frequency response of $Z_o(s)$, $Z_{con}(s)$, $Z_c(s)$ are illustrated. Compared with the results shown in Fig.5, the close-loop impedance $Z_{con}(s)$ under DCM has resistive-inductive characteristic. Similar to the VCM case, the output impedance also has a peak near the intersection frequency. However, with the presence of virtual resistor, the peak value is more damped.

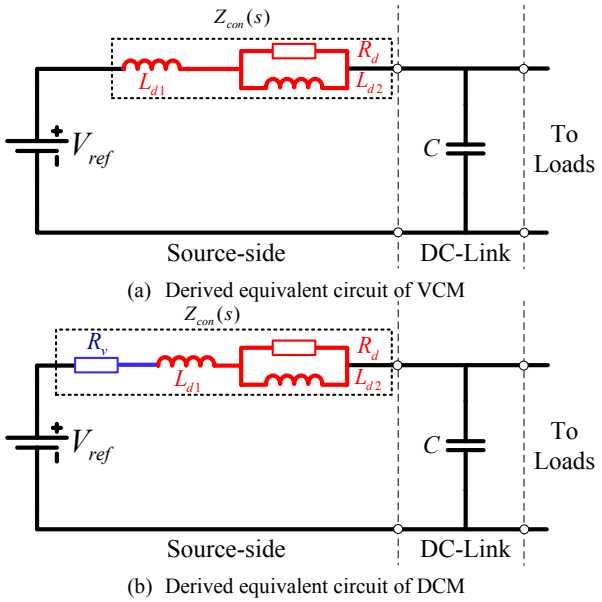


Fig. 4. Derived equivalent circuits of PEC with VCM and DCM controller.

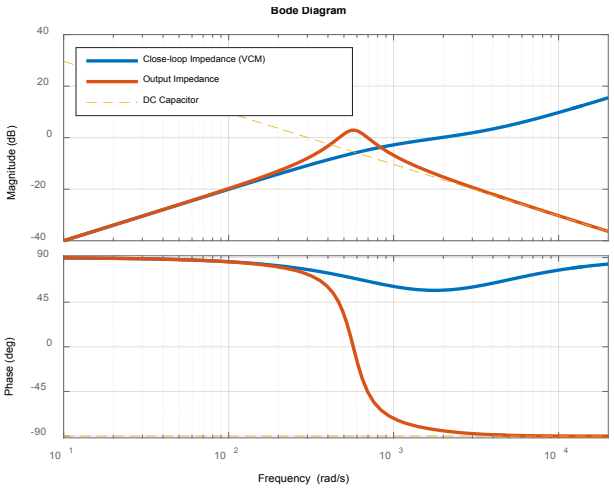


Fig. 5. Detailed frequency response of VCM controller .

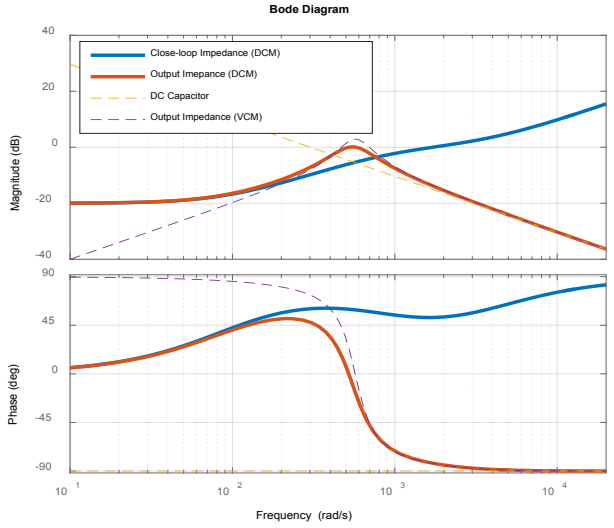


Fig. 6. Detailed frequency response of DCM controller.

III. PROPOSED METHOD

To mitigate the CPL instability issue discussed in the last section, a possible solution is to reduce the peak value of output impedance, therefore, the load-side performance will not be affected. It can be achieved by: (1) increase the series virtual resistance;(2) increase the capacitance of DC capacitor; (3) decrease the inductance of the equivalent circuit.

In case of DC SPS, the power ratings are considerably high, so that the virtual resistance must be much smaller than other applications. Otherwise, the voltage drop will exceed its operational limitation. At the same time, the increase of DC capacitance is costly in MVDC applications. In addition to that, it also results in more destructive DC-side short-circuit fault, which is critical to the system design. For these reasons, the impedance shaping method become a good choice to mitigate the CPL instability issue in DC SPS.

A. Mechanism of Negative Seires Virtual Inductor

As analyzed in the previous section, the virtual resistance based droop method is the simplest but typical example of virtual impedance method, in which only resistive virtual impedance is used. As conclusions of the analysis in the last section, several key features of the close-loop impedance can be summarized as following:

- The dual-loop controller itself performs an inductor in series to a *RL* paralleled branch, as shown in Fig. 4.
- The feedback loop used in droop method will perform additional component (marked blue) in series to the virtual components introduced by dual-loop controller (marked red).
- The additional component's resistance is decided only by the feedback loop and is independent to dual-loop controller. From (8) and (9), the same conclusion will be equally applicable to complex virtual impedance.

For these reasons, a specially designed virtual impedance can be used to enhance system stability. The designed virtual impedance shall be able to increase the equivalent resistance and/or to decrease the equivalent inductance.

As shown in Fig. 6, the virtual resistance can provide desired impedance shaping effect and damp the peak value of output impedance. However, as discussed previously, the high power of shipboard application strictly limits the feasible range of virtual resistance. In this case, the desired damping effect is hard to achieve with only virtual resistance method. In this case, negative series virtual inductor is proposed to decrease the equivalent inductance, thus mitigating the CPL instability issue.

To form a virtual inductor, a derivation controller with desired parameter will be needed. It is noteworthy that the designed negative virtual inductor is to cancel the virtual component L_{d1}, so that the following design rules must be fulfill to ensure the controller is individually stable:

$$Z_v(s) = sL_v, \qquad (-L_{d1} \le L_v \le 0) \tag{10}$$

In Fig. 7, the frequency response of output impedance using proposed method with different parameter settings (L_v=0~1.2L_{d1}) are shown. In Fig. 8, the poles and zeros of minor loop gain $T_m(s)$ is shown. Although the peak magnitude will continuously decreases with larger negative virtual inductor, the bus voltage got unstable once the stability boundary shown in (10) is exceeded.

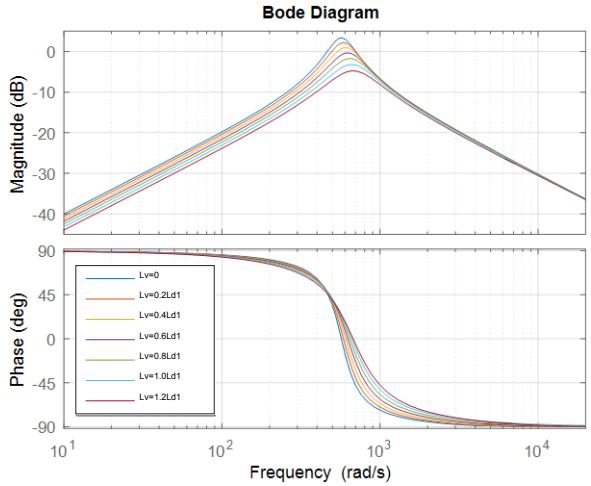


Fig. 7. Frequency response of output impedance with proposed method.

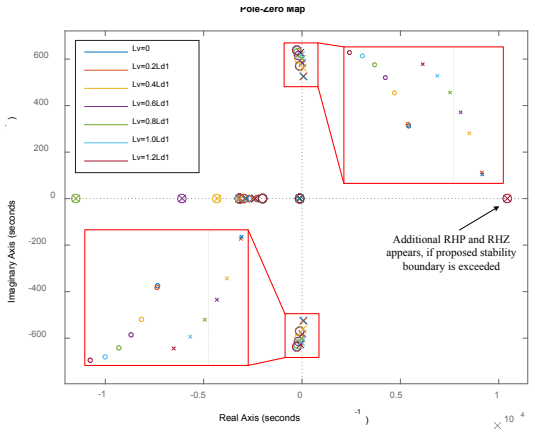
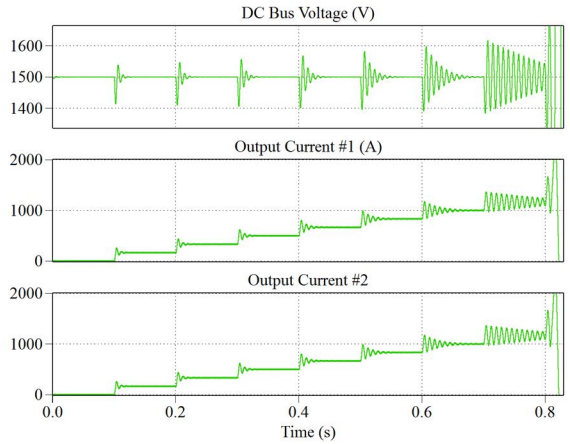


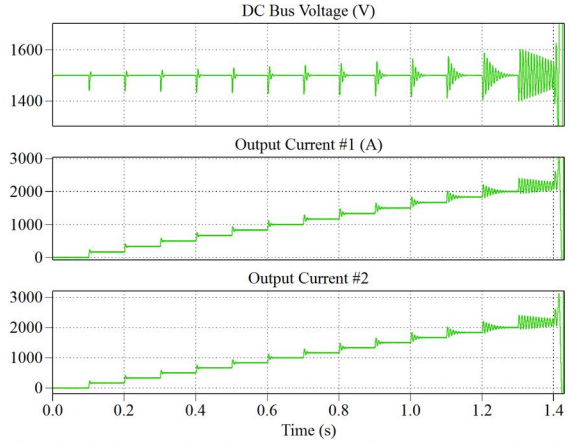
Fig. 8. Poles and zeros of $T_m(s)$ with proposed method.

IV. SIMULATION VERIFICATION

To validate the proposed negative series virtual inductor method, simulations are carried out with a simplified DC SPS composed by two source converters and controllable CPLs. Similar study cases have been presented in [14] and [15]. The simulations are carried out with detailed switching model established by using PLECS. The parameters used in the simulations are given in Table I. In Fig. 9, the simulation results of the system under VCM operation are shown. In Fig. 10, the simulation results of the system under DCM operation are shown. It can be seen from the simulation results that the system's stability margin and capability of feeding CPL is enhanced with the proposed method.

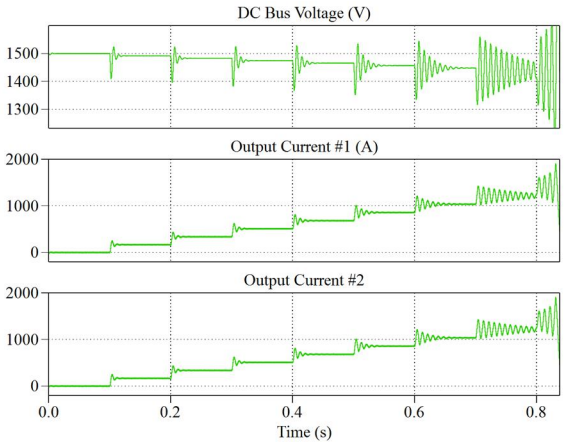


(a) Simulation results using only VCM controller

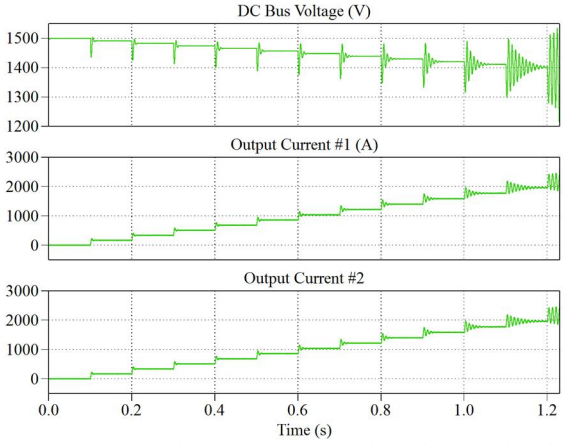


(b) Simulation results using VCM controller and proposed method

Fig. 9. Simulation results of VCM controller with/without proposed method.



(a) Simulation results using only DCM controller



(b) Simulation results using DCM controller and proposed method

Fig. 10. Simulation results of DCM controller with/without proposed method.

TABLE I. PARAMETERS OF SIMULATED STUDY CASE

Description of the Parameter	***Symbol***	***Value***
Voltage Reference	V_{ref}	1500 V
Source Voltage	E_1, E_2	3000 V, 3000 V,
Inductance of Buck Converters	L_1, L_2	8 mH, 8 mH
Stary Resistance of inductors,	r_1, r_2	0.1 Ω, 0.1 Ω
Switching Frequency	f_{sw}	2 kHz
Total Capacitance in DC Bus	C	3.3 mF
Proportion Term of Voltage Controller	K_{pv1}, K_{pv2}	1, 1
Integral Term of Voltage Controller	K_{iv1}, K_{iv2}	1000, 1000
Proportion Term of Current Controller	K_{pc1}, K_{pc2}	0.009, 0.009
Integral Term of Current Controller	K_{ic1}, K_{ic2}	0.1, 0.1
Virtual Resistances for Droop Control	R_{v1}, R_{v2}	0.05 Ω, 0.05 Ω,
CPL Control Bandwidth	ω_{CPL}	2000 rad/s
Load Profile	P_{Load}	500 kW/step 10 steps/s
Inductance of Negative Series Virtual Inductor	L_{v1}, L_{v2}	-0.243mH, -0.243mH, ($\approx -0.8L_{d1}$)

It can be seen from the simulation results that when using the proposed method, the system's capability of feeding CPL are improved. When operating in VCM, the maximum capable power of CPL is increased from 3.5 MW to 6.5 MW. As for operation under DCM control, the maximum capable power of CPL is increased from 3.5 MW to 5.5 MW.

It is noteworthy that theoretically DCM controller has a lower peak value of output impedance. However, the voltage drop will result in increased negative impedance of the same amount of CPL. Conversely, the capability of feeding CPL may decrease, when compared with VCM.

V. CONCLUSIONS

In this paper, model-derived negative series virtual inductor is presented as a compensating method to mitigate the CPL instability issue in DC SPSs. It differs from conventional virtual resistance or virtual impedance methods that specially designed negative virtual inductor is used to modify system stability when feeding CPL. The mechanism of CPL instability and the proposed method are briefly introduced. The output impedance characteristic of VCM and DCM controllers are analyzed. Simulation results are carried out to validate the proposed method, the results show enhanced stability and capability of feeding CPL.

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