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# Low Power FPGA Based Solar Charge Sensor Design Using Frequency Scaling

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***Abstract*— Resources of energy are degrading day by day the concept of energy saving is very important. Solar chargers are very most widely used devices which saves our energy resources. Use of Solar charges is now extremely increased. But the performance and effective output of these chargers depend upon how they are charged and discharged. Concept here is to use the solar Charger Sensor that regulates the charging and discharging process of Solar Chargers. These Solar charger Sensors should consume least power and hence make overall lifespan of these batteries to increase. Virtex6 Field Programmable Gate Array is used to Design the same Sensor for Solar Chargers for LVCMOS family. Frequency Scaling is used and reductions in Power consumed are observed.**

*Keywords- Energy Resources, Frequency Scaling, Solar Charger Sensor, Output, Discharging, Conservation*

## I. INTRODUCTION

Solar energy is best source for energy conservation concept and to use solar energy Solar Chargers are used. Solar chargers are commonly made up of number of cells which are connected together to store energy. The stored energy can be further used for many purposes like heating water or running electrical appliances and so on. The life span of solar chargers plays a very important role. If batteries are charged more than required as well as charging degrades below minimum level the performance will be affected. So, it is important for efficient output to charge them with utmost care. Solar Charge sensor can be used for this purpose. They sense the amount of voltage and stop and start charging the solar cells accordingly. We have done analyses on making these sensors low power and more precise. Frequency scaling is done for LVCMOS12, LVCMOS15, LVCMOS18 and LVCMOS25. The frequencies used are from 0.01GHz to 100GHz. Virtex6 Field Programmable array is used for implementing the design. The data is studied carefully and percentage changes for the factors that contribute to total power consumption of the sensor are calculated as shown in figure1, figure2, figure 3 and figure4.

## II. RELATED WORK

The concept of frequency scaling on FPGA is used by many researchers before for many Designs to minimize the power consumptions. LVCMOS based energy efficient charger [1] is analyzed before by using frequency scaling but the frequencies are different. The work is done for different LVCMOS Standards at different Frequencies used in our research. The frequencies used in related paper are 900MHz, 5GHz and 60 GHz and Low voltage Complementary Metal Oxide used are LVCMOS15, LVCMOS18, LVCMOS25 and LVCMOS33. LVCMOS33 is not used by us in our paper and frequency range is also

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different. But in both the papers results are taken out from Xilinx tool. Some other papers that have somehow similar work as ours are Energy efficient processor design using frequency scaling [2], dynamic Frequency and voltage control for clock domain micro architecture [3], Efficient charging of capacitors for increasing lifespan of wireless sensor nodes [4] which works for energy conservation.

# III. DATA ANALYSIS AND INTERPRETATION

## A. Result for LVCMOS12

Table 1: Readings of I/Os, Leakage and Total Power for LVCMOS12 at frequency range from 0.01GHz to 100GHz

| Frequency GHz | 0.01 | 0.1 | 1 | 10 | 100 |
|---|---|---|---|---|---|
| I/Os | 0.000 | 0.001 | 0.007 | 0.065 | 0.653 |
| Leakage | 0.710 | 0.710 | 0.711 | 0.715 | 0.760 |
| Total Power | 0.710 | 0.712 | 0.731 | 0.921 | 2.809 |

Readings noted in Table1 are analyzed and decrease in power consumption is noticed. The data can be analysed clearly from Figure3 for LVCMOS12 and Percentage decrease are as follows. Decrease in I/O is 90.4%, 98.92%, 99.84% and 100% when frequency is reduced from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively. Decrease in Leakage is 5.92%, 6.44%, 6.57% and 6.57% when frequency is reduced from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. Decrease in Total Power is 67.2%, 73.97%, 74.65% and 74.72% when frequency is reduced from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 1.

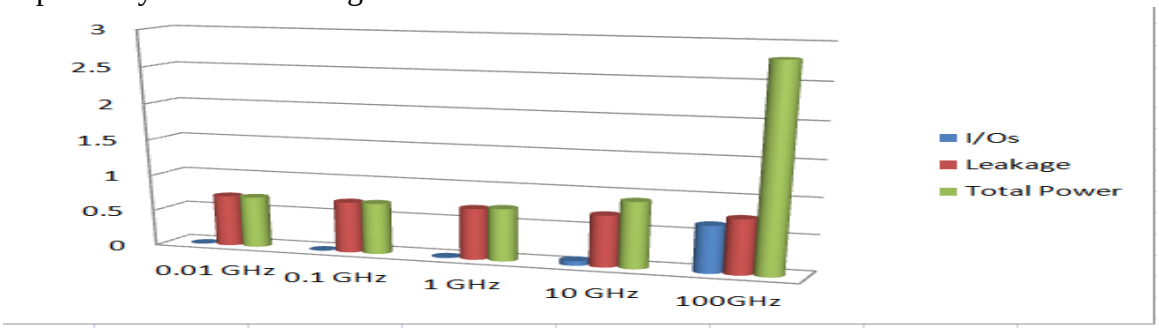


Figure1: Graphical Representation of I/O, Leakage and Total Power for LVCMOS12

## B. Result for LVCMOS15

Table 2: Readings of I/Os, Leakage and Total Power for LVCMOS15 at frequency range from 0.01GHz to 100GHz

| Frequency GHz | 0.01 | 0.1 | 1 | 10 | 100 |
|---|---|---|---|---|---|
| I/Os | 0.000 | 0.710 | 0.007 | 0.072 | 0.723 |
| Leakage | 0.711 | 0.711 | 0.711 | 0.716 | 0.762 |
| Total Power | 0.711 | 0.713 | 0.732 | 0.928 | 2.881 |

Readings noted in Table 2 are analyzed and decrease in power consumption is noticed. The data can be analysed clearly from Fig. 2 for LVCMOS15 and Percentage decrease are as follows. Decrease in I/O is 90.4%, 99.03%, 99.86% and 100% when frequency is reduced from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. Decrease in Leakage is 6.03%, 6.69%, 6.69% and 6.69% when frequency is reduced from 100GHz to 10GHz, 1GHz,

0.1GHz, and 0.01GHz respectively. Decrease in Total Power is 67.78%, 74.59%, 75.25% and 75.32% when frequency is reduced from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 2.

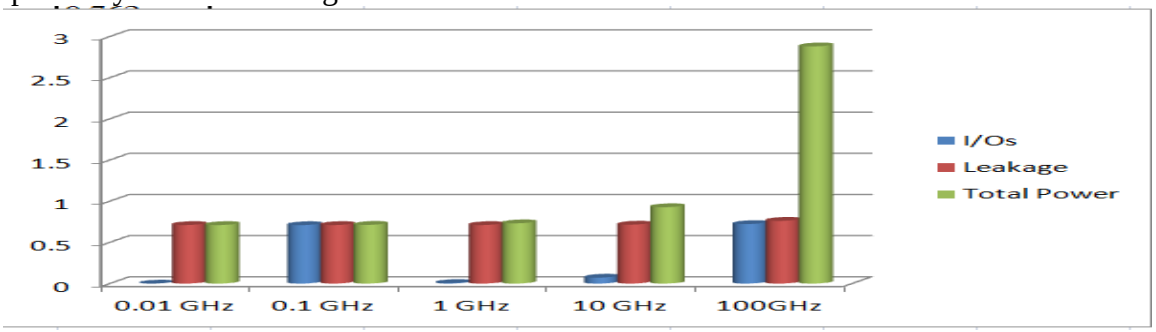


Figure2: Graphical Representation of I/O, Leakage and Total Power for LVCMOS15

## C. Result for LVCMOS18

Table 3 : Readings of I/Os, Leakage and Total Power for LVCMOS18 at frequency range from 0.01GHz to 100GHz

| Frequency GHz | 0.01 | 0.1 | 1 | 10 | 100 |
|---|---|---|---|---|---|
| I/Os | 0.000 | 0.001 | 0.08 | 0.079 | 0.786 |
| Leakage | 0.711 | 0.711 | 0.711 | 0.716 | 0.764 |
| Total Power | 0.711 | 0.713 | 0.733 | 0.935 | 2.947 |

Readings noted in Table3 are analyzed and decrease in power consumption is noticed. The data can be analyzed clearly from Figure3 for LVCMOS18 and Percentage decrease are as follows. Decrease in I/O is 89.94%, 98.98%, 99.87% and 100% when frequency is reduced from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively. Decrease in Leakage is 6.28%, 6.93%, 6.93% and 6.93% when frequency is reduced from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively. Decrease in Total Power is 68.27%, 75.12%, 75.80% and 75.97% when frequency is reduced from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively as shown in Fig. 3.

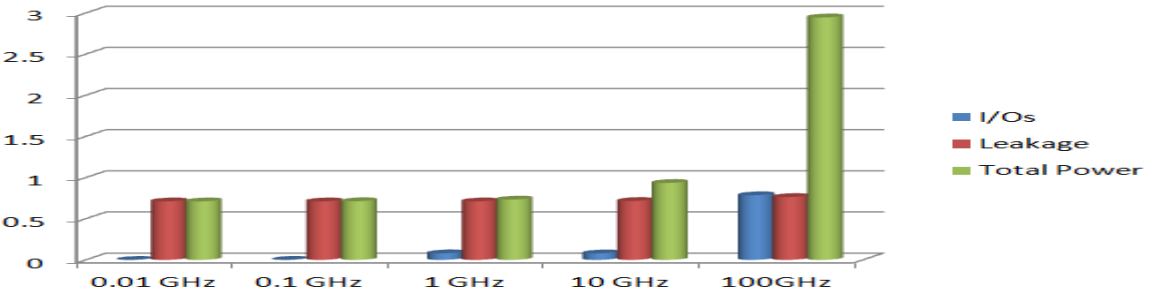


Figure3: Graphical Representation of I/O, Leakage and Total Power for LVCMOS18

## D. Result for LVCMOS25

Table 4: Readings of I/Os, Leakage and Total Power for LVCMOS25 at frequency range from 0.01GHz to 100GHz

| Frequency GHz | 0.01 | 0.1 | 1 | 10 | 100 |
|---|---|---|---|---|---|
| I/Os | 0.001 | 0.000 | 0.010 | 0.095 | 0.953 |
| Leakage | 0.712 | 0.712 | 0.712 | 0.717 | 0.769 |
| Total Power | 0.714 | 0.736 | 0.736 | 0.953 | 3.119 |

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Readings noted in Table4 are analyzed and decrease in power consumption is noticed. The data can be analyzed clearly from Figure3 for LVCMOS25 and Percentage decrease are as follows. Decrease in I/O is 90.4%, 98.92%, 99.84% and 100% when frequency is reduced from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. Decrease in Leakage is 5.92%, 6.44%, 6.57% and 6.57% when frequency is reduced from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. Decrease in Total Power is 67.2%, 73.97%, 74.65% and 74.72% when frequency is reduced from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Fig. 4.

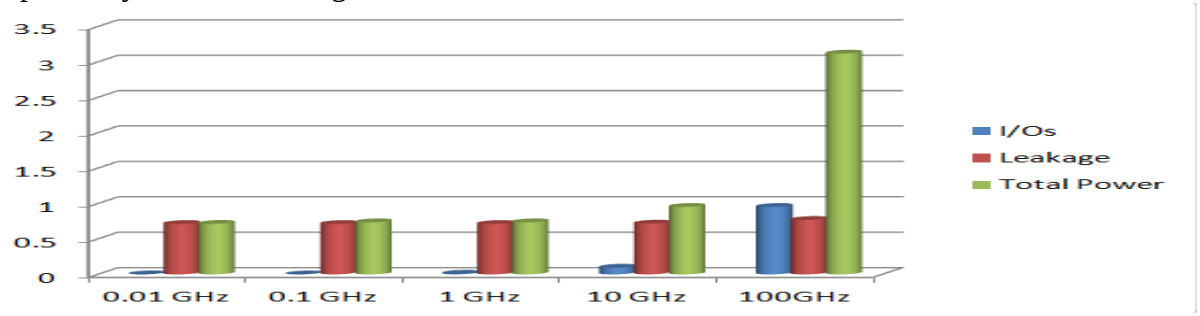


Fig. 4: Graphical Representation of I/O, Leakage and Total Power for LVCMOS25

## IV. CONCLUSION

Work is done successfully and results are analyzed for percentage reductions in leakage, IOs and total amount of power. The maximum decrease in power for LVCMOS12 is 74.72%, for LVCMOS15 is 75.32%, for LVCMOS18 is 75.975and for LVCMOS25 is 77.17%. From these results it can be concluded that among LVCMOS12, LVCMOS15, LVCMOS18 and LVCMOS25, default standard i.e. LVCMOS 25 shows maximum amount of decrease in power. Percentage decrease in power also increases as we increase the frequency for all the standards.

## V. FUTURESCOPE

These solar charge sensors will play very important role if used for solar batteries and can conserve large amount of energy as the life span of charging cells will be increased. Number of modifications can be done for reliable design .Voltage Scaling or capacitance scaling can also be used for further work. Time analyses can be done in future. The same can be performed for no of standards present like HSTL, LVDCI [5], SSTL and PCI3_33 etc. Many Field programmable Gate arrays like Virtex-7, Kintex-7, Artix-7 [6] can be used for more study and results for efficient system.

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