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Reduction in Power Consumption of Packet Counter on VIRTEX-6 FPGA by Frequency Scaling

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***Abstract*—In Today's World it is very easy to share the information fast may be within seconds or even may be less. However, the required data is shared so it is the main concern. We share data over web and data is transferred in the form of packets. How these data packets are transmitted is all concept of Networking. This paper focuses on making of a packet counter that consumes least power for its operation. Packet counters are used for counting data packets at transmitter and receiver end and hence finding the number of packets or data lost in whole process. The Design is implemented for LVCOMS_25, LVDCI_25, SSTL_15 and HSTL_III I/O standards for Virtex6 Field Programmable Gate Array. Percentage Change in power consumed is calculated by scaling frequency and hence efficient packet counter is achieved.**

Keywords- *Data Transmission, Networking, Packet Counter, Frequency Scaling, FPGA, Efficient*

I. INTRODUCTION

When we transfer data on internet there are number of possibilities of some data being missed or delayed in reaching data at its destination. Therefore, it is very important to have a check over the system to ensure that data is being received and sent properly and contains required information. This paper is about making packet counter which helps in monitoring the data packets sent and received over network. It is important to check every node during transmission to make sure that no data packets are lost in between as they can contain important information. Computer Networking is a term that is used for transferring data packets from source to destination. There are many intermediate devices used between transmission like switches, routers etc. Packet counter will keep on every intermediate stage also whether the count of data packets is same as input. The counter will increase its value or make a count if any data packet is either missing or wrong. Here the approach is made to see the power consumption of these counters for different I/O standards using a range of frequency from 1-20 GHz. Other components which finally add up to total power consumption are also taken care. Data communication occurs through TCP/IP protocol [1]. How Data packets are received and transmitted is done through different layers of the model. There are five TCP/IP layers which are as shown below in figure1.

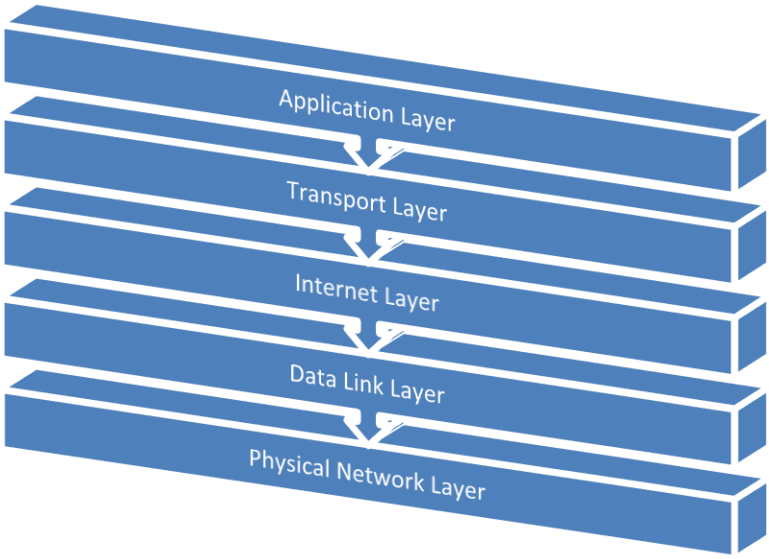

Figure 1: **Layers of TCP/IP model**

- Application layer is the layer where the communication is started It makes the packet appropriate to handle by Transport Layer.
- At Transport Layer data encapsulation is started.
- At Internet Layer data packets are ready for delivery.
- Data Link Layer is used for framing.
  When the packets come at the receiving end the same process is followed in reverse order. The RTL view of packet counter using Xilinx ISE Design Suite 12.1 is shown in figure2.

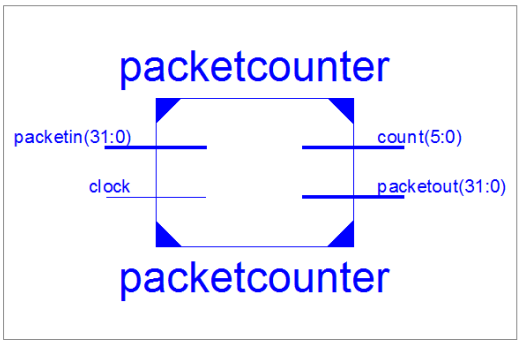

Figure 2: Schematic View of Traffic Light Controller

II. RELATED WORK

Some work is done for better transmission of data over the web. However, least is done in terms of efficiency. There are many papers about counting the data packets whether the number of data packets transmitted is same as number of data packets received. This design is made on Virtex6 Field programmable array in which work is done to make the design performance better by reducing the total amount of power consumed by the system. Some of the papers which used data packet counter in similar or dissimilar way are described below. They are useful in differentiating and matching our work with already done work.

1. **Deep packet inspection using parallel Bloom filters [2]**

This Paper has concern about matching the previous signatures in the packet payload. This is achieved by using bloom filters. They have used hardware bloom filters for finding the matching string in the payload. Conclusion is that with FPGA a large string can be examined at very high speed. This work is not that much related to our but only thing is Field Programmable Gate array is used. No work is done in terms of saving power consumption of the system.

2. **Data packet switch using a primary processing unit [3]**

This paper consists of primary processing unit based on software which is responsible for transmitting and receiving the data packet streams. There is no need of processing data further by primary processing unit. The concern is different from our work and has no focus on energy saving as we have done using Field Programmable Gate Array Design.

3. **Regular expression matching for reconfigurable packet inspection [4]**

In this paper the synthesis is done using VHDL and data is collected for Virtex4 Virtex2 devices. The work is done to reduce the packet payload content. In this way more complex expressions can be supported. But approach used by us is of frequency scaling to make packet counter efficient by reducing its power consumption.

There are more paper like design of multiplier based on HSTL IO Standard [5], DES Algorithm Design which is low power [6] and Arithmetic Logic Unit Design on 28nm FPGA which is based on SSTL [7] which works in the same area to reduce the amount of power used and hence making the performance curve increase by different types of scaling.

III. DATA ANALYSIS AND INTERPRETATION

1. Result For LVCMOS_25

Table 1: Values of Clock, Logic and Signal, I/O, Leakage, Total Power for LVCMOS_25

Frequency	1GHz	5GHz	10GHz	15GHz	20GHz
Clock	0.015	0.077	0.154	0.232	0.309
Logic	0.000	0.001	0.002	0.002	0.002
Signal	0.002	0.011	0.021	0.032	0.042
I/O	0.429	4.436	8.872	13.309	17.745
Leakage	0.722	0.828	0.968	1.029	1.029
Total Power	1.169	5.353	10.017	14.603	19.127

Percentage reduction in clock is 24.9%, 50.16%, 75.08% and 95.14% when drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively and Percentage reduction in Logic is 0%, 0%, 50% and 100% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively. Percentage reduction in Signal is 23.80%, 50%, 73.80% and 95.23% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively and Percentage reduction in I/O is 24.99%, 50%, 75% and 97.58% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively. Percentage reduction in Leakage is 0%, 5.928%, 19.53% and 29.83% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively and Percentage reduction in Total Power is 23.65%, 47.62%, 72.01% and 93.88% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively as shown in Table 1. Graphical representation of all the factors contributing to total power reduction is shown in Fig. 3.

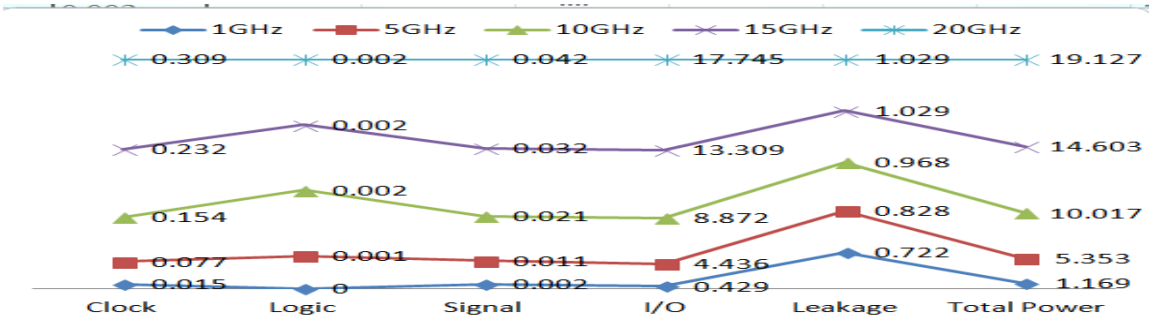

Figure3: Graph of Clock, Logic and Signal, I/O, Leakage and Total Power at different frequencies for LVCMOS_25

2. Result For LVDCI_25

Table 2: Values of Clock, Logic and Signal, I/O, Leakage, Total Power for LVDCI_25

Frequency	1GHz	5GHz	10GHz	15GHz	20GHz
Clock	0.015	0.077	0.154	0.232	0.309
Logic	0.000	0.001	0.002	0.002	0.002
Signal	0.002	0.012	0.025	0.037	0.050
I/O	0.491	4.007	7.896	11.785	15.675
Leakage	0.724	0.816	0.936	1.029	1.029
Total Power	1.233	4.914	9.013	13.085	17.065

Percentage reduction in clock is 24.9%, 50.16%, 75.08% and 95.14% when drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively and Percentage reduction in Logic is 0%, 0%, 50% and 100% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively. Percentage reduction in Signal is 26%, 50%, 76% and 96% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively and Percentage reduction in I/O is 24.81%, 49.26%, 74.43% and 96.86% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively. Percentage reduction in Leakage is 0%, 9.03%, 20.69% and 29.64% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively and Percentage reduction in Total Power is 23.32%, 47.184%, 71.20% and 92.77% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively as shown in Table 2. Graphical representation of all the factors contributing to total power reduction is shown in Fig. 4.

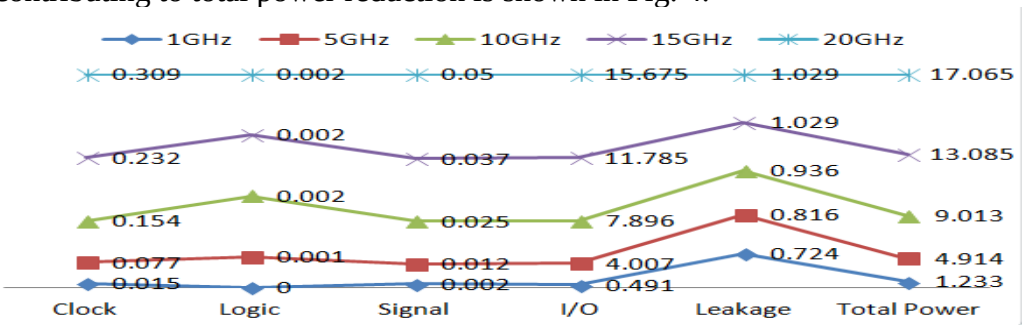

Figure 4: Graph of Clock, Logic and Signal, I/Os, Leakage and Power at different frequencies for LVDCI_25

3. Result For SSTL_15

Table 3: Values of Clock, Logic and Signal, I/O, Leakage, Total Power for SSTL_15

Frequency	1GHz	5GHz	10GHz	15GHz	20GHz
Clock	0.016	0.077	0.154	0.232	0.309
Logic	0.000	0.001	0.002	0.002	0.002

Signal	0.003	0.016	0.032	0.047	0.063
I/O	0.727	1.051	2.679	3.707	4.734
Leakage	0.728	0.753	0.782	0.812	0.844
Total Power	1.475	2.498	3.648	4.799	5.952

Percentage reduction in clock is 24.9%, 50.16%, 75.08% and 95.14% when drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively and Percentage reduction in Logic is 0%, 0%, 50% and 100% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively. Percentage reduction in Signal is 25.39%, 49.20%, 74.60% and 95.23% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively and Percentage reduction in I/O is 21.69%, 43.40%, 77.79% and 84.64% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively. Percentage reduction in Leakage is 3.79%, 7.34%, 10.78% and 13.74% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively and Percentage reduction in Total Power is 19.37%, 38.70%, 58.03% and 75.21% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively as shown in Table 3. Graphical representation of all the factors contributing to total power re222duction is shown in Fig. 5.

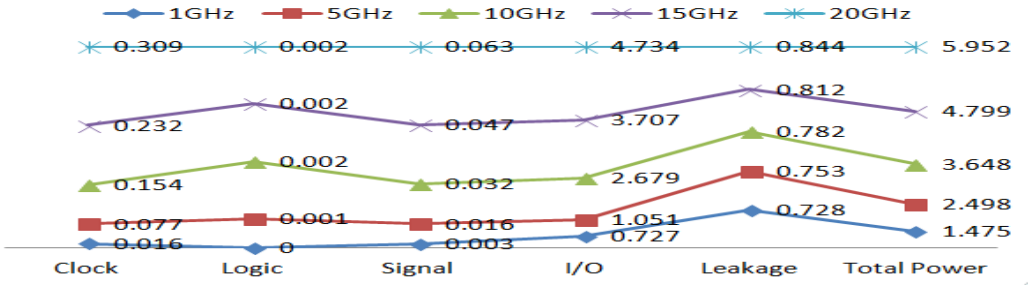

Figure 5: Graph of Clock, Logic and Signal, I/Os, Leakage and Power at different frequencies for SSTL_15

4. Result For HSTL_III

Table 4: Values of Clock, Logic and Signal, I/O, Leakage, Total Power for HSTL_III

Frequency	1GHz	5GHz	10GHz	15GHz	20GHz
Clock	0.016	0.077	0.154	0.232	0.309
Logic	0.000	0.001	0.002	0.002	0.002
Signal	0.003	0.016	0.032	0.047	0.063
I/O	0.669	1.831	3.122	4.412	5.703
Leakage	0.727	0.758	0.794	0.832	0.872
Total Power	1.416	2.683	4.103	5.525	6.949

Percentage reduction in clock is 24.9%, 50.16%, 75.08% and 95.14% when drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively and Percentage reduction in Logic is 0%, 0%, 50% and 100% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively. Percentage reduction in Signal is 25.39%, 49.20%, 74.60% and 95.23% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively and Percentage reduction in I/O is 22.63%, 45.25%, 67.89% and 88.26% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively. Percentage reduction in Leakage is 5.61%, 8.94%, 13.07% and 16.62% when we drop off frequency from 20GHz to 15GHz, 10GHz, 5GHz and 1GHz respectively and Percentage reduction in Total Power is 20.49%, 40.95%, 61.39% and 79.62% when we drop off frequency from 20GHz to

15GHz, 10GHz, 5GHz and 1GHz respectively as shown in Table 4. Graphical representation of all the factors contributing to total power reduction is shown in Fig. 6.

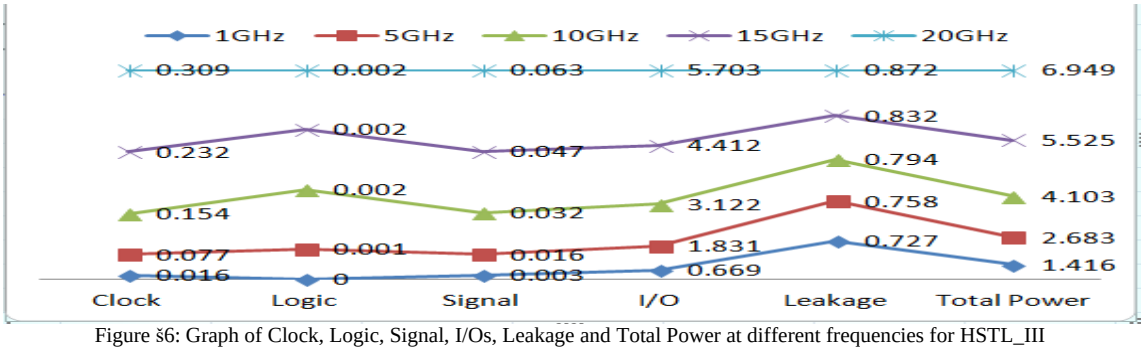

Figure š6: Graph of Clock, Logic, Signal, I/Os, Leakage and Total Power at different frequencies for HSTL_III

IV. CONCLUSION

There is noteworthy change in all the factors that contribute to total power consumption of the packet counter design for different I/O standards at different frequencies. Frequency is scaled form 20GHz to 15GHz, 10GHz, 5GHz and 1 GHz for four different I/O Standards i.e. LVCMOS_25, LVDCI_25, SSTL_15 and HSTL_III. For LVCMOS_25 maximum percentage reduction and minimum percentage reductions in total power are 93.88%, 23.65% when frequency is changed from 20 to 15GHz and 1GHz respectively. Similarly for SSTL-15 maximum value of reduced powers is 75.21% and minimum is 19.37%. For LVDCI_25 maximum fall is and minimum decrease are92.77% and 23.32% respectively and for HSTL_III total power is maximum reduced to 79.62% and minimum 20.49%.

V. FUTURESCOPE

Transfer of data packets will never going to reduce in future but has become an ideal mode for communicating data over web. So it is always important to check that the transmission is done as required or not. For this the design must require as much less power as possible. For achieving the same work can be done for other I/O standards like PCI3_33 or Mobile DDR etc. Also the field programmable array families like Airtex-7, Virtex-7[8] Kintex-7 and many more can be used for different types of scaling. Time Analysis can also be done to improve the speed of the system.

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