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Published in:
I E E E Transactions on Industry Applications

DOI (link to publication from Publisher):
10.1109/TIA.2016.2628895

Publication date:
2017

Document Version
Early version, also known as pre-print

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A Short Circuit Safe Operation Area Identification Criterion for SiC MOSFET Power Modules

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***Abstract*— This paper proposes a new method for the investigation of the Short-Circuit Safe Operation Area (SCSOA) of state-of-the-art SiC MOSFET power modules rated at 1.2 kV based on the variations in SiC MOSFET electrical parameters (e.g., short-circuit current and gate-source voltage). According to the experimental results, two different failure mechanisms have been identified, both reducing the short-circuit capability of SiC power modules in respect to discrete SiC devices. Based on such failure mechanisms, two short-circuit safety criteria have been formulated: (i) the short circuit current-based criterion and, (ii) the gate voltage-based criterion. The applicability of these two criteria makes possible the SCSOA evaluation of SiC MOSFETs with some safety margins in order to avoid unnecessary failures during their SCSOA characterization. SiC MOSFET power modules from two different manufacturers are experimentally tested in order to demonstrate the procedure of the method. The obtained results can be used to have a better insight of the SCSOA of SiC MOSFETs and their physical limits.**

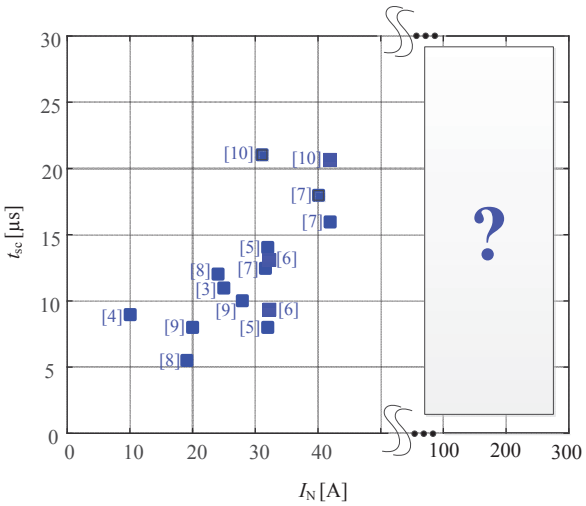

Fig. 1. Maximum short circuit time of state-of-the-art SiC MOSFETs rated at 1.2 kV. Testing conditions T = 25°C and V_{DS} = 600 V [3]–[10].

I. Introduction

Over the last decades, silicon has been the major semiconductor choice for power electronic devices. As state-of-the-art silicon semiconductors slowly approach their limits in terms of power losses, reduced size, safe operation area boundaries and maximum allowable junction temperature, Wide-Bandgap semiconductors (WBG) have emerged as a potential substitute to overcome such limitations [1]. Among the WBG semiconductors, Silicon Carbide (SiC) has demonstrated a good compromise between its high-frequency switching capability and high temperature performance, especially if one includes the overall converter cost saving due to smaller passives and smaller chip area [2]. As a consequence of these advantages, various types of SiC devices are nowadays commercially available, such as Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETS), Junction Field-Effect Transistors (JFETs), Super Junction Transistors (SJTs) and Bipolar Junction Transistors (BJTs). During the last years, the SiC MOSFET has become dominant over the available SiC devices. It is of great interest to assess its performance under static and dynamic conditions and even more interesting, its performance under short circuit conditions. To that end, SiC MOSFETs have been selected for the purpose of this study.

Although the claimed superior performance of SiC power devices over traditional Si devices has been the major driving force for most applications, the ability to withstand stressful and harsh conditions may alter the attitude of this conclusion. For instance, prior-art research on the Short Circuit (SC) capability of 1.2 kV SiC MOSFETs has indirectly proved so [3]–[10]. The static and dynamic performances of SiC MOSFETs have been compared to Si IGBTs in [7], [11] and to Si MOSFETs in [11], [12], where the advantages of WBG devices have been demonstrated (i.e., lower losses, higher operation temperature). In [4], SiC MOSFETs have shown high junction operation temperature capabilities (i.e., beyond 250°C) for long-term reliability, nevertheless, the short circuit capability has proven to be equivalent to its silicon counterparts. Additionally, the Short Circuit Safe Operation Area (SCSOA) of the latest discrete 1.2 kV SiC MOSFET devices have been lately investigated, evidencing a large variation between different manufacturers (i.e, typically Cree, Rohm, GE) [5]–[7] and testing conditions (i.e., DC link voltage, case temperature, and gate voltage) [8], [9], [13]. Other studies have focused on the development of an electro-thermal model for predicting the SCSOA, including failure time and simulated junction temperature at different testing conditions, such as those in [10], [14].

According to the aforementioned literature, Fig. 1 gives the latest results of 1.2 kV SiC MOSFETs as a function of their nominal current and their maximum short circuit time. The short circuit operating conditions are T = 25°C and V_{DS} = 600 V. Based on these results, discrete SiC MOSFETs have proved to withstand 6 to 15 μs, evidencing for some of the cases lower robustness compared to the Si IGBTs, where the typical short circuit withstanding time is 10 μs at the highest operating temperature [15]. The lower SCSOA of SiC MOSFETs raises a new challenge for SiC gate drivers, in which the protection circuit needs to rapidly detect the short circuit condition having in mind the higher switching frequencies of such devices and their interaction with the noisy environment. Methods for short circuit detection and protection for SiC MOSFETs have been proposed in [16]–[18]. Furthermore, Fig. 1 highlights that the short circuit robustness of high current SiC MOSFET power modules has yet to be addressed. This fact rises new opportunities for investigation since the SCSOA of modules is completely different compared to discrete devices due to current sharing imbalances among the paralleled chips. This possible imbalance is very likely to happen as the experimental results presented in this paper prove so. To that end, this paper contributes on the SCSOA of SiC MOSFET power modules to provide an insight into the the short circuit performances of state-of-the-art SiC MOSFET power modules.

The failure mechanisms in SiC MOSFETs under short circuit conditions are mainly temperature-related. SiC devices, theoretically, have a much higher intrinsic thermal limit than Si devices due to lower intrinsic carrier concentration and wider band gap. However, SiC devices have smaller chip area and higher current density than the corresponding Si devices, resulting in higher temperature rising rate, and thus lower SC withstanding capability. The aim of this paper is to identify which are the operating conditions in which the device can survive under a short circuit event. Specifically, this work presents the short circuit behaviour of 1.2 kV/ 300 A SiC MOSFET power modules from Cree and 1.2 kV/ 180 A SiC MOSFET power modules from Rohm. Two different failure mechanisms have been identified. Based on such failure mechanisms, two short-circuit safety criteria (i.e., short circuit current-based criterion and gate voltage-based criterion) are proposed as a method for defining the Short-Circuit Safe Operation Area. The proposed method can be used for plotting the SCSOA of power devices at different testing conditions avoiding its self-destruction. This solution is practical and cost-effective when testing expensive technologies, such as SiC.

This paper is organized as follows: Section II presents the Non-Destructive Short Circuit Tester adopted for the SCSOA characterization of SiC MOSFET power modules. Section III shows the short-circuit experimental results of the studied SiC MOSFET power modules up to failure. Section IV illustrates the proposed criterion for SCSOA evaluation based on the failure mechanisms observed in Section III. Section V validates the two suggested short-circuit safety criteria for the studied SiC MOSFET power modules. Finally, concluding remarks are given.

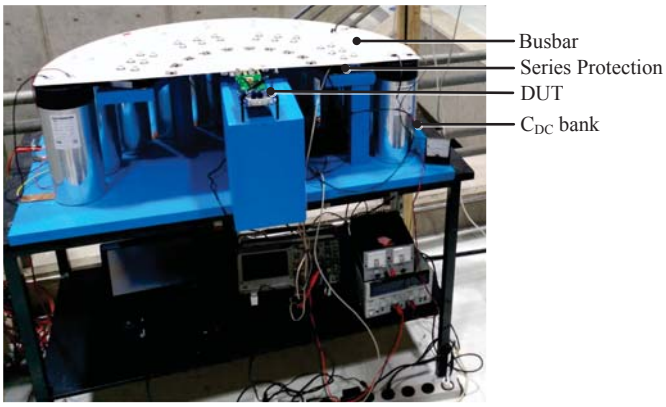

Fig. 2. Picture of the 10 kA/ 2.4 kV Non-Destructive Testing setup.

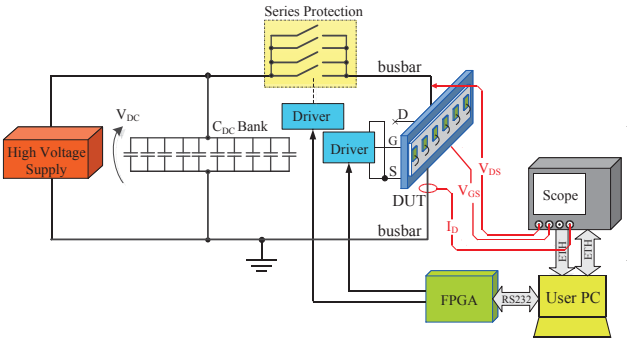

Fig. 3. Principle schematic of the constructed Non-Destructive Tester.

II. Description of the Short Circuit Testing Setup

A. Hardware Implementation

The following commercial SiC MOSFET power modules have been considered for the SCSOA investigation: Cree's 1.2 kV/ 300 A and Rohm's 1.2 kV/ 180 A. A Non-Destructive Tester (NDT) has been built with the current and voltage limits of 10 kA and 2.4 kV in the laboratory of the Energy Technology Department at Aalborg University, Denmark [19]. The basic principle of the non-destructive testing technique is to perform repetitive tests up to the physical limits of the Device Under Test (DUT) while avoiding the device destruction. Referring to Figs. 2 and 3, the tester structure includes the following parts: a high-voltage power supply V_{DC} which charges up a capacitor bank C_{DC} consisting on ten capacitors, whose energy is used to perform the tests; four series protection switches working as a circuit breaker right after the short circuit test, and thus preventing explosions of the DUT in the case of failure and allowing for post-failure analysis; a computer-designed round busbar ensuring even current distribution among the parallel devices; a 100 MHz Field-Programmable Gate Array (FPGA) providing the driving signals for the DUT and the protection switches, together with the trigger used for acquiring the measurements. The total inductance including busbar, intrinsic inductances of the series protection and capacitors is about 50 nH, which is larger than the external inductance that the manufacturers use to test their

devices, but it is a realistic value for the end-users applications. A Personal Computer (PC) is used for the data acquisition and remote control, which is connected via an Ethernet link to the LeCroy HDO6054-MS oscilloscope and via an RS-232 bus to the FPGA board.

A commercial SiC MOSFET gate driver recommended by Cree is used for testing both DUTs, namely CGD15HB62P, whose desaturation protection has been inhibited in order to perform the short-circuit tests. The experiments have been done for gate-emitter voltage equal to +20 V/ -6 V and external gate resistance equal to 5 Ω. The gate resistance has been chosen according with the datasheet recommendation and ensuring a good turn-on and turn-off controllability. The case temperature of the modules was at about 25°C.

B. Software Implementation

In order to perform short circuit tests in a repeatable and consistent way, an original automated tool having a user-friendly Graphical User Interface (GUI) has been developed and implemented in MATLAB® (see Fig. 4). Such an interface provides the possibility to perform repetitive tests with a set of parameters defined by the user as well as the total number of tests to be performed and the time between pulses. The developed GUI provides a list of limits (pass conditions) to be verified to proceed automatically for the next test. After setting up the test parameters, the user sets the high voltage power supply to the operating voltage and starts the repetitive test sequence (START button in Fig. 4). Tests are performed completely equal to each other, according with the time sequence set by the user and the time between pulses (e.g., the off-time has been selected to 30 seconds allowing enough time to cool down the device). The GUI communicates to the FPGA the exact time sequence at the beginning of every test through the instrumentation bus. A data check protocol has been implemented in order to avoid communication errors that would eventually lead to a fatal test. To make the user aware of the last parameters sent to the FPGA, a local echo is included on the left-hand side of the GUI. At the end of every test, the waveforms sampled by the oscilloscope are acquired through Active-X functions, in order to fully exploit the instrument capabilities. The acquired waveforms are stored including test index and time-stamp.

Fig. 4. Graphical User Interface (GUI) developed in MATLAB® to perform the SCSOA characterization. A sample violation condition has been evidenced in the picture.

III. Experimental Results

In this section the experimental results will be presented. To determine the short circuit capability of the investigated devices, the NDT shown in Fig. 2 has been used. The short circuit failure limit was determined by increasing the short circuit pulse width after each successful pulse in steps of normally 100 ns until failure. Different bias voltages from 200 V up to 800 V were applied.

A. 1.2 kV/ 300 A SiC MOSFET

Fig. 5a shows a single short-circuit event where the 1.2 kV/ 300 A SiC MOSFET fails within a relatively short pulse duration of 3.2 μs for a bias voltage of 600 V and ambient temperature of 25°C. In these test conditions, the device survived single short-circuit pulse durations up to 3.1 μs. In fact, the next short-circuit pulse with a duration of 3.2 μs causes the device failure. Initially, the drain current dramatically increases and reaches its saturation level at about 5 kA - 15 times greater than its nominal value. A significant decrease of drain current suggests a fast temperature increase inside the device due to reduction on the channel carrier mobility with increasing temperature. As it can be seen in Fig. 5a, the device is apparently able to turn off the short-circuit current, but after 2 μs, a delayed failure occurs forcing the drain current to increase out of control. Post-failure analysis demonstrated a burn-out of one of the six paralleled SiC chips as well as a short circuit among the three terminals, as it is shown in Fig. 5b. This delayed failure is commonly recognized as a thermal runaway failure mechanism which typically occurs when the device is in off-state at high junction temperatures. Previous studies [9], [10] have identified trough numerical validation that a thermal runaway failure is possible due to high off-state drain leakage current. Such high drain leakage current may activate the parasitic *npn* BJT inside the MOSFET. If the parasitic BJT is turned on, the drain current rapidly increases leading to a device failure due to typical second breakdown failure mechanisms and associated thermal runaway. This type of failures could be avoided if the energy dissipated during the short circuit is lower than the critical one - in this case the calculated critical energy from the experimental waveforms is equal to 6.9 J.

Another failure mechanism has been observed for the short circuit testing of the 1.2 kV/ 300 A SiC MOSFET. During the second round of tests, the short circuit energy was kept below the calculated critical one (E_{crit} = 6.9 J). Fig. 6 shows a single short-circuit event where the 1.2 kV/ 300 A SiC MOSFET fails within 1.9 μs at 800 V DC-link voltage. The device failed due to a short circuit between the gate and source terminals which could have been triggered by a high local temperature close to the gate oxide causing the increase of the gate leakage current. Gate oxide reliability issues in SiC MOSFETs have previously been pointed out in [4], [6], [13]. In contrast to Si MOSFETs, the higher electric field and thinner thickness of the SiC MOSFET gate oxide causes a large leakage current to flow from the gate to the source if not well-designed. This issue becomes more evident at higher drain-source voltages because the electric field deeper penetrates into the P-base

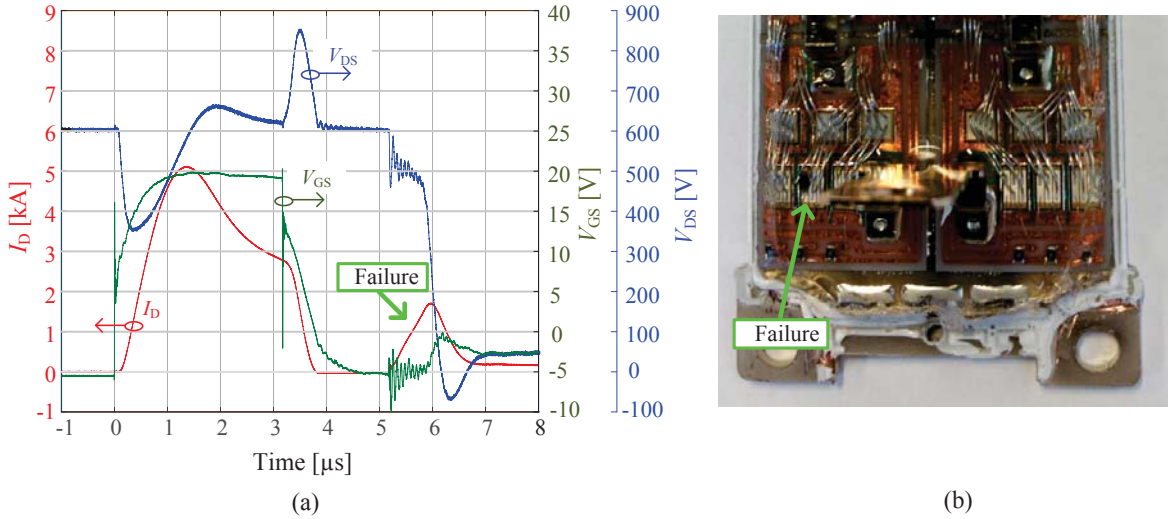

Fig. 5. Short circuit thermal runaway failure of the 1.2 kV/ 300 A SiC MOSFET module within 3.2 μs at V_{DS} = 600 V and T = 25°C : (a) measured waveforms, and (b) observed failure.

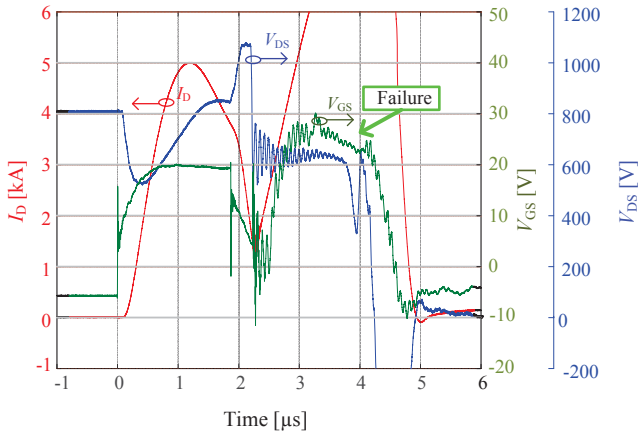

Fig. 6. Short circuit gate breakdown failure of the 1.2 kV/ 300 A SiC MOSFET module within 1.9 μs at V_{DS} = 800 V and T = 25°C.

region. Additionally, higher temperatures also increase the gate leakage current. This has been confirmed by the results in Fig. 6, where the gradual reduction of the gate voltage could be interpreted as an increase in the gate leakage current.

B. 1.2 kV/ 180 A SiC MOSFET

To the same extent, short circuit tests were carried out on the 1.2 kV/ 180 A SiC MOSFET from Rohm. Fig. 5a shows the short circuit failure within 7.2 μs and V_{DC} = 800 V. A similar failure mechanism has been seen as the one observed in Fig. 5a, in which the device apparently turns off the short circuit current, but after 7 μs a thermal runaway failure occurs. Fig. 5b shows the burn-out of one of the SiC MOSFET chips due to the short circuit failure. Here, a large current tail is observed which progressively increases with the pulse length, confirming that a high drain leakage current is flowing inside the device. The calculated critical energy for the 1.2 kV/ 180 A DUT is 8.2 J. Additionally, the gradual reduction of the gate-source voltage is also observed, indicating that the second failure mechanism as mentioned before may be triggered.

The 1.2 kV/ 180 A SiC module featured higher robustness against short circuit conditions when compared with the 1.2 kV/ 300 A device. One may note that the 1.2 kV/ 180 A device offers lower drain saturation current, about 10 times of its nominal value, resulting in lower temperature stress handling during its operation. However, a good indicator to understand which device handles the higher temperature stress is the critical short circuit energy, where the 1.2 kV/ 300 A SiC MOSFET critical energy calculated from the experiments is 6.9 J and the 1.2 kV/ 180 A SiC MOSFET critical energy calculated from the experiments is 8.2 J.

IV. Proposed Criterion for Short-Circuit Safe Operation Area Evaluation

The new proposed method gives a general guideline in order to characterize the Short-Circuit Safe Operation Area of SiC MOSFETs based on the monitoring of two parameters: (i) the short-circuit current, and (ii) the gate-source voltage. According to the experimental results, both parameters are good indicators for predicting short circuit failures in SiC MOSFETs and thus helping to avoid them. The steps of the proposed algorithm are shown in Fig. 8. Before starting the algorithm, the user sets two limit values, namely, the short-circuit current limit $I_{D,SOA}$, and the gate-source voltage limit $V_{G,SOA}$. The selection of these limits will be explained later based on the formulation of two short-circuit safety criteria: (i) short-circuit current-based criterion, and (ii) gate voltage-based criterion. The next step is to set the high voltage power supply to the operating voltage and the short-circuit pulse length (e.g., the starting pulse length could be set to 1 μs). It is worth to note that the proposed method requires a pass/fail evaluation after each test. To do that, the experimental short-circuit waveforms, i.e., the short-circuit current and gate-source voltage waveforms, are acquired by means of an oscilloscope and analyzed at the end of each test. There are two

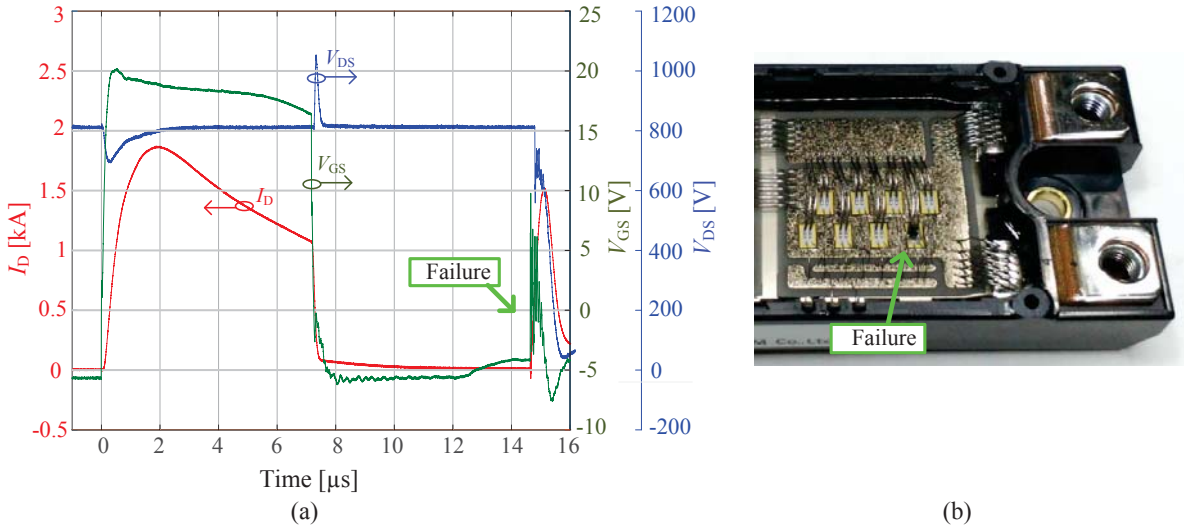

Fig. 7. Short circuit thermal runaway failure of the 1.2 kV/ 180 A SiC MOSFET module within 7.2 μs at V_{DS} = 800 V and T = 25°C: (a) measured waveforms, and (b) observed failure.

pass/fail conditions which are compared between the acquired experimental waveforms and the predefined parameter limits set by the user. In case that one of the limits is violated, the drain-source voltage and the short-circuit pulse length is stored for producing the SCSOA of the DUT. On the other hand, when the limits have not yet been met, the user continues with the short-circuit experiments by increasing the short-circuit pulse length; for instance in steps of 100 ns. The detailed discussions on the procedure and its validation under various DC-link voltages are provided in the following section.

V. Short Circuit Safe Operation Area Analysis of the 1.2 kV SiC MOSFETs

To safely operate the device under SC events, two SC safety criteria have been adopted: a) the SC current-based criterion and b) the gate voltage-based criterion. These two criteria have been identified based on the previous experiments on SiC MOSFET power modules.

A. Short Circuit Current-Based Criterion

Based on short circuit failures related to thermal runaway instabilities, an original approach is developed, which relies on the negative dependence between the SC current and the junction temperature [20]. The idea is to define during the short circuit event a drain current level, which corresponds to the maximum allowable junction temperature that the device can withstand up to failure. For instance, in Fig. 5 the critical temperature value which leads to thermal runaway corresponds with a short circuit current of 3 kA. In order to avoid this type of failure, a new method is proposed consisting in applying a short circuit pulse no longer than the one needed to heat it up to the critical temperature. Since the junction temperature of the chip is difficult to measure, a minimum short circuit current level is defined ensuring lower short circuit energy dissipation - the 1.2 kV/ 300 A SiC MOSFET limit is selected to be 4 kA.

To validate that this approach could be implemented as a new method for short circuit protection in the future modern SiC gate drivers, several tests have been done for various DC-link voltages in which the short circuit pulse is not further increased if the short circuit current reaches the selected limit (e.g., 4 kA). Fig. 9a demonstrates that the device operates safely when the short circuit current-based criterion is applied at different DC-link voltages. The driving strategy of these devices becomes critical: it is shown that the higher the DC-link voltage, the shorter pulse length due to the large dissipated power. For instance, the gate driver must be designed to detect the short circuit condition and protect the device within 1.8 μs at 800 V.

One further verification of the short circuit current-based criterion is given by applying the proposed method to the 1.2 kV/ 180 A SiC MOSFET. As can be seen in Fig 7, the critical temperature value leading into thermal runaway corresponds to a short circuit current of 1 kA. For that reason, the maximum short circuit current level is selected to be 1.5 kA for the 1.2 kV/ 180 A device. Similarly as before, the DUT has been tested under different DC-link voltages without violating the short circuit current-based criterion. Fig. 9b shows the short-circuit robustness when the proposed approach is applied.

B. Gate Voltage-Based Criterion

Based on short circuit failures related with the degradation of the gate oxide, another approach is proposed based on the reduction of the gate voltage level during the short circuit event. The approach consists on defining a gate voltage level which corresponds with the maximum allowable gate leakage current that the device can withstand up to failure. For instance, in Fig. 7 the final gate voltage value which leads to the gate destruction is about 19.4 V. In order to avoid this failure, a second method is proposed consisting in applying a short circuit pulse no longer than a selected gate voltage value

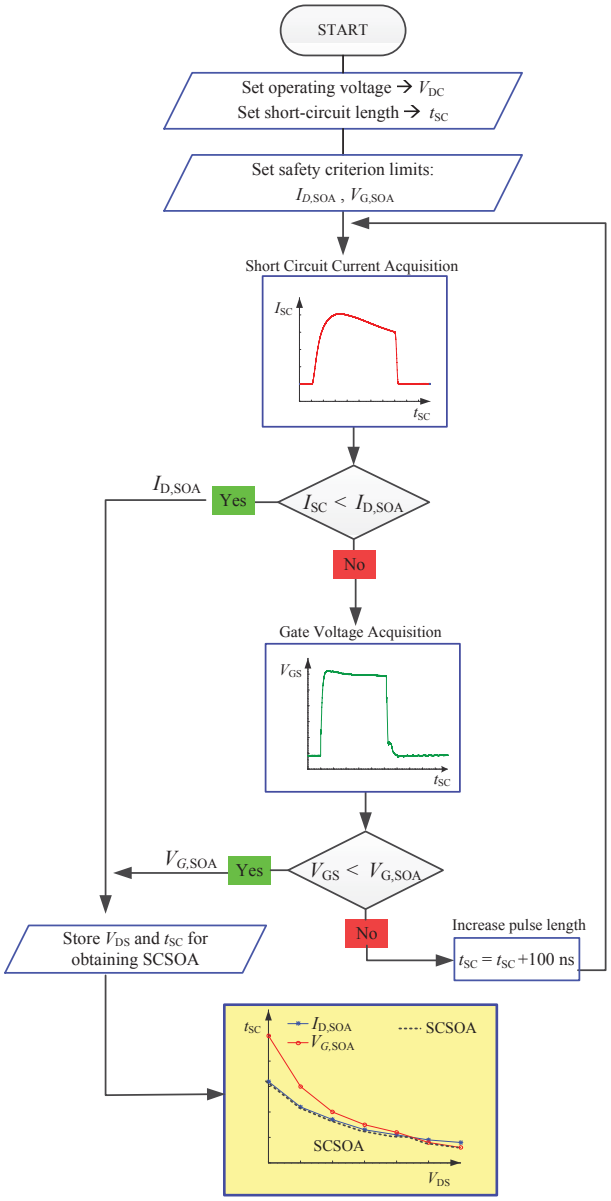

Fig. 8. Flowchart of the new proposed guideline for obtaining the Short-Circuit Safe Operation Area of SiC MOSFETs: $I_{D,SOA}$, the short-circuit current limit, and $V_{G,SOA}$, the gate-source voltage limit.

- the 1.2 kV/ 300 A SiC MOSFET limit is selected to be 19.5 V.

The validation of the gate voltage-based criterion is demonstrated in Figs. 10a and 10b for the 1.2 kV/ 300 A SiC MOSFET and the 1.2 kV/ 180 A SiC MOSFET, respectively. Several tests have been done for various DC-link voltages in which the pulse length is not further increased if the gate voltage decreases below the selected limit (e.g., V_{GS} = 19.5 V for the first device and V_{GS} = 19.4 V for the second one). Fig. 10 reveals that the two devices survive if the gate voltage-based criterion is applied at different DC-link voltages. One important aspect is that when the DUTs are tested at low DC-link voltages, i.e., 200 V or 300 V, the gate voltage-based

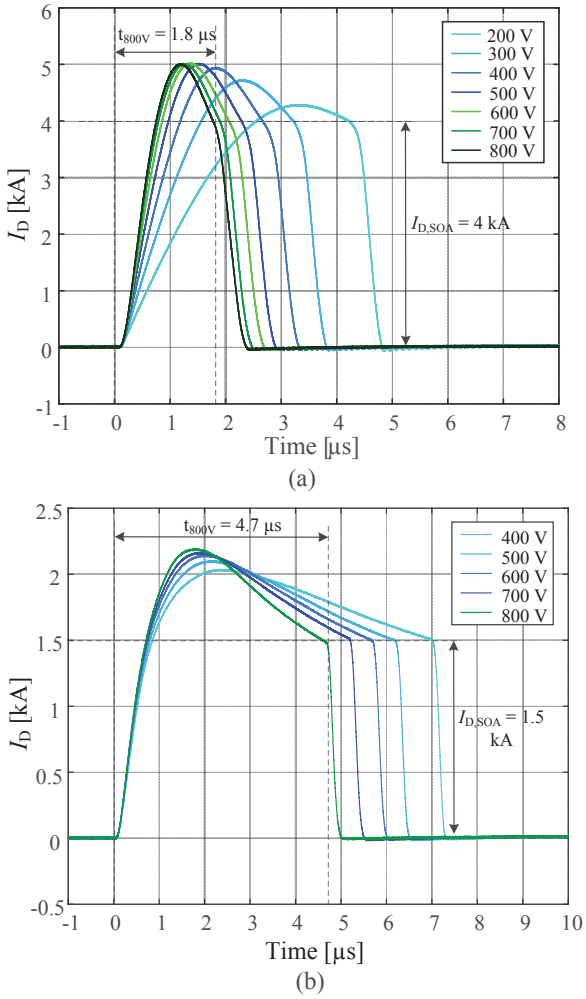

Fig. 9. Validation of the short circuit current-based criterion at different DC-link voltages: (a) the 1.2 kV/ 300 A SiC MOSFET in which the short circuit current limit is 4 kA, and (b) the 1.2 kV/ 180 A SiC MOSFET in which the short circuit current limit is 1.5 kA.

criterion is not met, instead the short circuit current-based criterion has firstly been met and longer short circuit times are not applied.

C. Short-Circuit Safe Operation Area

In order to identify the operating conditions where the SiC device can survive under a short circuit event, two parameters are usually studied: the SC withstanding time, t_{sc}, and the critical SC energy, E_{crit}. Typically, t_{sc} is around 10 μs at the maximum rated operating temperature, which may be a possible thread for SiC MOSFETs power modules since their SC robustness remains unknown. In this regard, this section will experimentally illustrate the SC capability of the two SiC MOSFET power modules. The SCSOA of the DUTs has been formulated based on two original short circuit criteria: (a) the short circuit current-based criterion, $I_{D,SOA}$, and (b) the gate voltage-based criterion, $V_{G,SOA}$. To that end, Fig. 11 shows the SCSOA of the two studied SiC MOSFET power modules as a function of the drain-source voltage and short circuit time

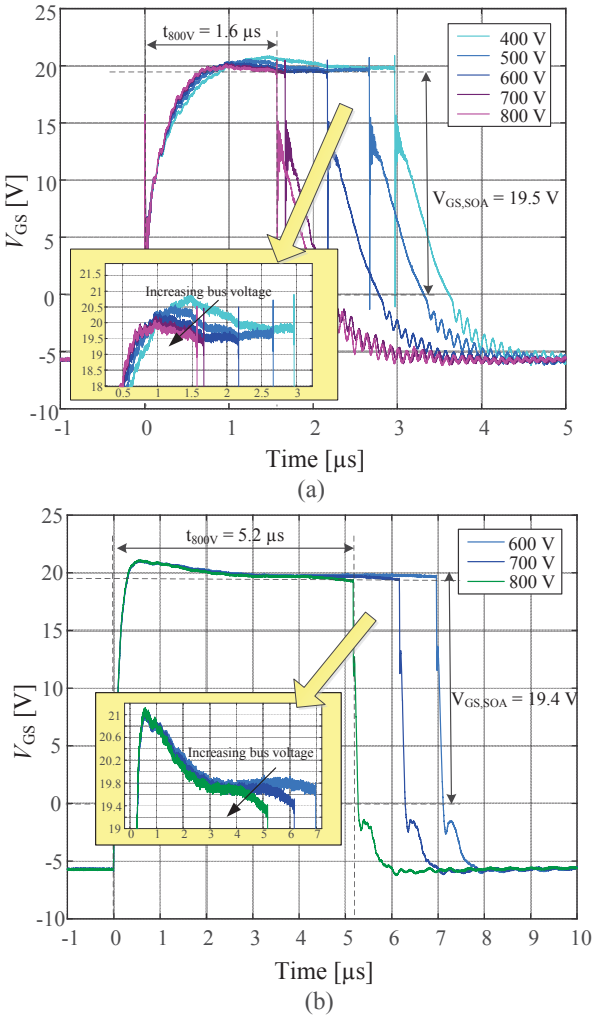

Fig. 10. Validation of the gate voltage-based criterion at different DC-link voltages: (a) the 1.2 kV/ 300 A SiC MOSFET in which the gate voltage limit is 19.5 V, and (b) the 1.2 kV/ 180 A SiC MOSFET in which the gate voltage limit is 19.4 V.

at room temperature. As it can be observed Fig. 11, the short circuit-current based criterion seems to be more restrictive than the gate voltage-based criterion, although at higher DC-link voltages, it is worth to note that the gate voltage-based criterion becomes more crucial. The more restrictive criterion will be selected as the final SCSOA as indicated with a dashed line in Fig. 11.

Furthermore, it is worth to point out that in order to take advantage of SiC MOSFET power modules benefits, more stringent requirements are needed in the design of gate driver fault protection circuits. For instance, if both modules are to be operated at 600 V bias voltage, the gate driver must be able to protect the device within 2 μs for the 1.2 kV/ 300 A DUT and within 5.8 μs for the 1.2 kV/ 180 A DUT as it is shown in Fig. 11. From these results, one may conclude that the short SC withstanding capability of SiC power module devices in this study is lower than the one of Si IGBT power modules. Nevertheless, the authors would like to emphasize that Si IGBTs do not always fulfil the typical SC withstanding time of

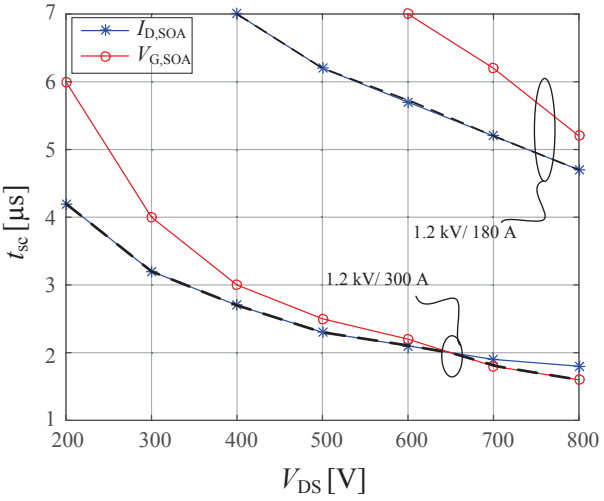

Fig. 11. Short circuit SOA of the two SiC MOSFET power modules based on the two proposed criteria at T = 25°C. $I_{D,SOA}$ - short circuit current-based criterion and $V_{G,SOA}$ - gate voltage-based criterion. Dashed line corresponds with the final SCSOA.

10 μs, as it is demonstrated in [21], [22]. For future activities, the new proposed guideline for the SCSOA evaluation of SiC MOSFETs could also be provided as a function of the operating junction temperature. It is worth to note that the proposed method relies on temperature-dependent indicators which could easily be applied for SCSOA characterization at different temperatures. Furthermore, prior studies have already pointed out a linear dependence of the SCSOA with the initial junction temperature [23], [24]. For this reason, the expected outcome would be a linear shift towards lower SCSOA with increasing temperature.

VI. Conclusion

In this study an investigation of the SCSOA of commercial 1.2 kV SiC MOSFET power modules is presented by looking at their characteristics, trying to understand potentials and possible limitations, and drawing initial conclusions on how such devices must be operated in order to ensure a good SC withstanding capability. Two failure mechanisms have been observed in this work, which are in agreement with the ones found in the literature for discrete SiC MOSFETs. The first one occurs on both gate and drain terminals due to the high drain leakage current in the off state as a consequence of the high energy dissipated during the short circuit event. A local fusion on the surface metallization of the device is observed when the module is opened. The second failure occurs in the gate side simultaneously with the destruction between drain and source during the short circuit turn-off. The main contributor is thought to be the high gate leakage current due to degradation of the material properties of the gate oxide, which are more crucial at high temperatures. Based on the observed short circuit failures, two SC criteria have been adopted in order to predict their robustness under short circuit conditions: a) the SC current-based criterion and b) the gate voltage-based criterion. A new guideline is proposed to define the SCSOA of the two studied SiC MOSFET power modules by applying

the two short-circuit safety criteria with the aim of providing some margin in order to avoid unnecessary failures for the typical SCSOA characterization.

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