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Investigation on the Short Circuit Safe Operation Area of SiC MOSFET Power Modules

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***Abstract*— This paper gives a better insight of the short circuit capability of state-of-the-art SiC MOSFET power modules rated at 1.2 kV by highlighting the physical limits under different operating conditions. Two different failure mechanisms have been identified, both reducing the short-circuit capability of SiC power modules in respect to discrete SiC devices. Based on such failure mechanisms, two short circuit criteria (i.e., short circuit current-based criterion and gate voltage-based criterion) are proposed in order to ensure their robustness under short-circuit conditions. A Safe Operation Area (SOA) of the studied SiC MOSFET power modules is formulated based on the two proposed criteria.**

I. Introduction

Over the last decades, silicon has been the major semiconductor choice for power electronic devices. As state-of-the-art silicon semiconductors slowly approach their limits in terms of power losses, reduced size, safe operation area boundaries and maximum allowable junction temperature, Wide-Bandgap semiconductors (WBG) have emerged as a potential substitute to overcome such limitations [1]. Among the WBG semiconductors, Silicon Carbide (SiC) has demonstrated a good compromise between its high-frequency switching capability and high temperature performance, especially if one includes the overall converter cost saving due to smaller passives and smaller chip area [2]. As a consequence of these advantages, various types of SiC devices are nowadays commercially available, such as Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETS), Junction Field-Effect Transistors (JFETs), Super Junction Transistors (SJTs) and Bipolar Junction Transistors (BJTs). During the last years, the SiC MOSFET has become dominant over the available SiC devices. It is of great interest to assess its performance under static and dynamic conditions and even more interesting, its performance under short circuit conditions. To that end, SiC MOSFETs have been selected for the purpose of this study.

Although the claimed superior performance of SiC power devices over traditional Si devices has been the major driving force for most applications, the ability to withstand stressful and harsh conditions may alter the attitude of this conclusion. For instance, prior-art research on the Short Circuit (SC) capability of 1.2 kV SiC MOSFETs has indirectly proved so [3]–[10]. The static and dynamic performances of SiC MOSFETs have been compared to Si IGBTs in [7], [11] and to Si MOSFETs in [11], [12], where the advantages of WBG

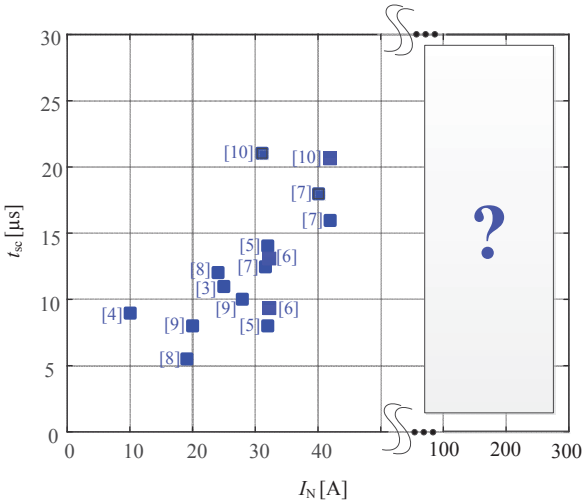

Fig. 1. Maximum short circuit time of state-of-the-art SiC MOSFETs rated at 1.2 kV. Testing conditions T = 25°C and V_{DS} = 600 V [3]–[10].

devices have been demonstrated (i.e., lower losses, higher operation temperature). In [4], SiC MOSFEts have shown high junction operation temperature capabilities (i.e., beyond 250°C) for long-term reliability, nevertheless, the short circuit capability has proven to be equivalent to its silicon counterparts. Additionally, the Short Circuit Safe Operation Area (SCSOA) of the latest discrete 1.2 kV SiC MOSFET devices have been lately investigated, evidencing a large variation between different manufacturers (i.e, typically Cree, Rohm, GE) [5]–[7] and testing conditions (i.e., DC link voltage, case temperature, and gate voltage) [8], [9], [13]. Other studies have focused on the development of an electro-thermal model for predicting the SCSOA, including failure time and simulated junction temperature at different testing conditions, such as those in [10], [14].

According to the aforementioned literature, Fig. 1 gives the latest results of 1.2 kV SiC MOSFETs as a function of their nominal current and their maximum short circuit time. The short circuit operating conditions are T = 25°C and V_{DS} = 600 V. Based on these results, discrete SiC MOSFETs have proved to withstand 6 to 15 μs, evidencing for some of the cases lower

robustness compared to the Si IGBTs, where the typical short circuit withstanding time is 10 μs at the highest operating temperature [15]. The lower SCSOA of SiC MOSFETs raises a new challenge for SiC gate drivers, in which the protection circuit needs to rapidly detect the short circuit condition having in mind the higher switching frequencies of such devices and their interaction with the noisy environment. Methods for short circuit detection and protection for SiC MOSFETs have been proposed in [16], [17]. Furthermore, Fig. 1 highlights that the short circuit robustness of high current SiC MOSFET power modules has yet to be addressed. This paper contributes on the SCSOA of SiC MOSFET power modules to provide an insight into the the short circuit performances of state-of-the-art SiC MOSFET power modules.

The failure mechanisms in SiC MOSFETs under short circuit conditions are mainly temperature-related. SiC devices, theoretically, have a much higher intrinsic thermal limit than Si devices due to lower intrinsic carrier concentration and wider band gap. However, SiC devices have smaller chip area and higher current density than the corresponding Si devices, resulting in higher temperature rising rate, and thus lower SC withstanding capability. The aim of this paper is to identify which are the operating conditions in which the device can survive under a short circuit event. Specifically, this work presents the short circuit behaviour up to failure of 1.2 kV/ 300 A SiC MOSFET power modules from Cree and 1.2 kV/ 180 A SiC MOSFET power modules from Rohm. Two different failure mechanisms have been identified. Based on such failure mechanisms, two short-circuit safety criteria (i.e., short circuit current-based criterion and gate voltage-based criterion) are proposed. To solve this issue, a Short-Circuit Safe Operation Area (SCSOA) of the studied SiC MOSFET power modules is defined in this paper, based on the proposed approach.

II. Description of the Short Circuit Testing Setup

The following commercial SiC MOSFET power modules have been considered for the SCSOA investigation: Cree's 1.2 kV/ 300 A and Rohm's 1.2 kV/ 180 A. A Non-Destructive Tester (NDT) has been built with the current and voltage limits of 10 kA and 2.4 kV in the laboratory of the Energy Technology Department at Aalborg University, Denmark [18]. The basic principle of the non-destructive testing technique is to perform repetitive tests up to the physical limits of the Device Under Test (DUT) while avoiding the device destruction. Referring to Figs. 2 and 3, the tester structure includes the following parts: a high-voltage power supply V_{DC} which charges up a capacitor bank C_{DC} consisting on ten capacitors, whose energy is used to perform the tests; four series protection switches working as a circuit breaker right after the short circuit test, and thus preventing explosions of the DUT in the case of failure and allowing for post-failure analysis; a computer-designed round busbar ensuring even current distribution among the parallel devices; a 100 MHz Field-Programmable Gate Array (FPGA) providing the driving signals for the DUT and the protection switches, together with the trigger used for acquiring the measurements. The total

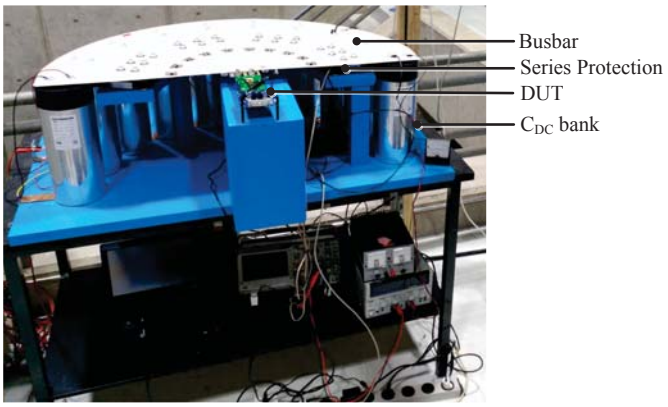

Fig. 2. Picture of the 10 kA/ 2.4 kV Non-Destructive Testing setup.

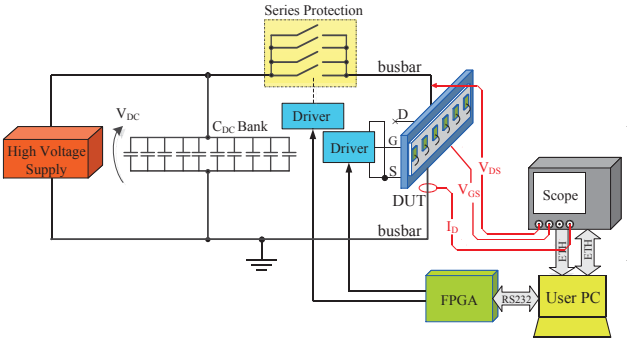

Fig. 3. Principle schematic of the constructed Non-Destructive Tester.

inductance including busbar, intrinsic inductances of the series protection and capacitors is about 50 nH, which is larger than the external inductance that the manufacturers use to test their devices, but it is a realistic value for the end-users applications. A Personal Computer (PC) is used for the data acquisition and remote control, which is connected via an Ethernet link to the LeCroy HDO6054-MS oscilloscope and via an RS-232 bus to the FPGA board.

A commercial SiC MOSFET gate driver recommended by Cree is used for testing both DUTs, namely CGD15HB62P, whose desaturation protection has been inhibited in order to perform the short-circuit tests. The experiments have been done for gate-emitter voltage equal to +20 V/ -6 V and external gate resistance equal to 5 Ω. The case temperature of the modules was at about 25°C.

III. Experimental Results

In this section the experimental results will be presented. To determine the short circuit capability of the investigated devices, the NDT shown in Fig. 2 was used. The short circuit failure limit was determined by increasing the short circuit pulse width after each successful pulse in steps of normally 100 ns until failure. Different bias voltages from 200 V up to 800 V were applied.

Fig. 4 shows a single short-circuit event where the 1.2

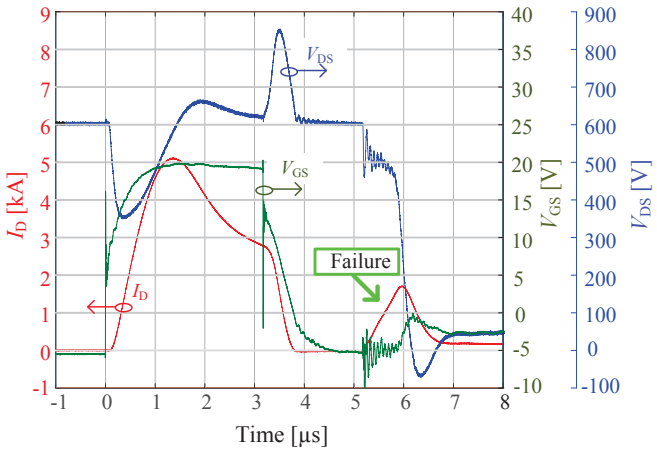

Fig. 4. Short circuit failure of the 1.2 kV/ 300 A SiC MOSFET module within 3.2 μs at V_{DS} = 600 V and T = 25°C.

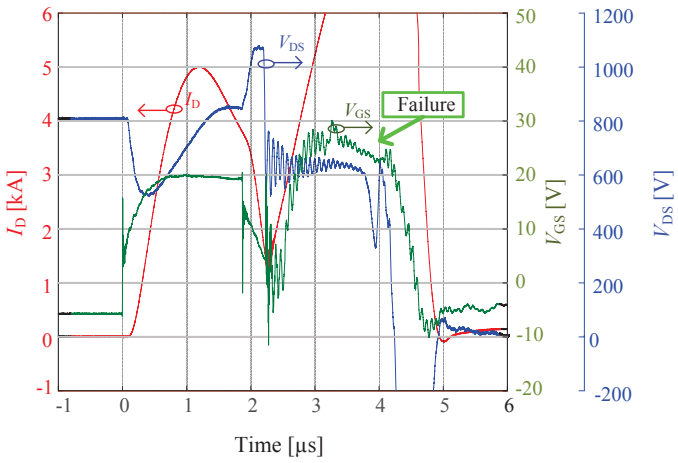

Fig. 5. Short circuit failure of the 1.2 kV/ 300 A SiC MOSFET module within 1.9 μs at V_{DS} = 800 V and T = 25°C.

kV/ 300 A SiC MOSFET fails within a relatively short pulse duration of 3.2 μs for a bias voltage of 600 V and ambient temperature of 25°C. In these test conditions, the device survived single short-circuit pulse durations up to 3.1 μs. In fact, the next short-circuit pulse with a duration of 3.2 μs causes the device failure. Initially, the drain current dramatically increases and reaches its saturation level about 5 kA - 15 times greater than its nominal value. A significant decrease of drain current suggests a fast temperature increase inside the device due to reduction on the channel carrier mobility with increasing temperature. As it can be seen in Fig. 4, the device apparently is able to turn off the short-circuit current, but after 2 μs, a delayed failure occurs making the drain current increasing out of control. Post-failure analysis demonstrated a burn-out of one of the six paralleled SiC chips as well as a short circuit among the three terminals. This delayed failure is commonly recognized as a thermal runaway failure mechanism which typically occurs when the device is in off-state at high junction temperatures. Previous studies [9], [10] have identified trough numerical validation that a thermal runaway failure is possible due to high off-state drain leakage current. Such high drain leakage current may activate the parasitic *npn* BJT inside the MOSFET. If the parasitic BJT is turned on, the drain current rapidly increases leading to a device failure due to typical second breakdown failure mechanisms and associated thermal runaway. This type of failures could be avoided if the energy dissipated during the short circuit is lower than the critical one - in this case the critical energy is equal to 6.9 J.

Another failure mechanism has been observed for the short circuit testing of the 1.2 kV/ 300 A SiC MOSFET. During the second round of tests, the short circuit energy was kept below the calculated critical one (E_{crit} = 6.9 J). Fig. 5 shows a single short-circuit event where the 1.2 kV/ 300 A SiC MOSFET fails within 1.9 μs at 800 V DC-link voltage. The device failed due to a short circuit between the gate and source terminals which could have been triggered by a high local temperature close to the gate oxide causing the increase of the gate leakage current. Gate oxide reliability issues in SiC MOSFETs have previously been pointed out in [4], [6], [13]. In contrast to Si MOSFETs, the higher electric field and thinner thickness of the SiC MOSFET gate oxide causes a large leakage current to flow from the gate to the source if not well-designed. This issue becomes more evident at higher drain-source voltages because the electric field deeper penetrates into the P-base region. Additionally, higher temperatures also increase the gate leakage current. This has been confirmed by the results in Fig. 5, where the gradual reduction of the gate voltage could be interpreted as an increase in the gate leakage current.

To the same extent, short circuit tests were carried out on the 1.2 kV/ 180 A SiC MOSFET from Rohm. Fig. 6 shows the short circuit failure within 7.2 μs and V_{DC} = 800 V. A similar failure mechanism has been seen as the one observed in Fig. 4, in which the device apparently turns off the short circuit current, but after 7 μs a thermal runaway failure occurs. Here, a large current tail is observed which progressively increases with the pulse length, confirming that a high drain leakage current is flowing inside the device. The calculated critical energy for the 1.2 kV/ 180 A DUT is 8.2 J. Additionally, the gradual reduction of the gate-source voltage is also observed, indicating that the second failure mechanism as mentioned before may be triggered.

The 1.2 kV/ 180 A SiC module featured higher robustness against short circuit conditions when compared with the 1.2 kV/ 300 A device. One may note that the 1.2 kV/ 180 A device offers lower drain saturation current, about 10 times of its nominal value, resulting in lower temperature stress handling during its operation. However, a good indicator to understand which device handles the higher temperature stress is the critical short circuit energy, where the 1.2 kV/ 300 A SiC MOSFET critical energy is 6.9 J and the 1.2 kV/ 180 A SiC MOSFET critical energy is 8.2 J.

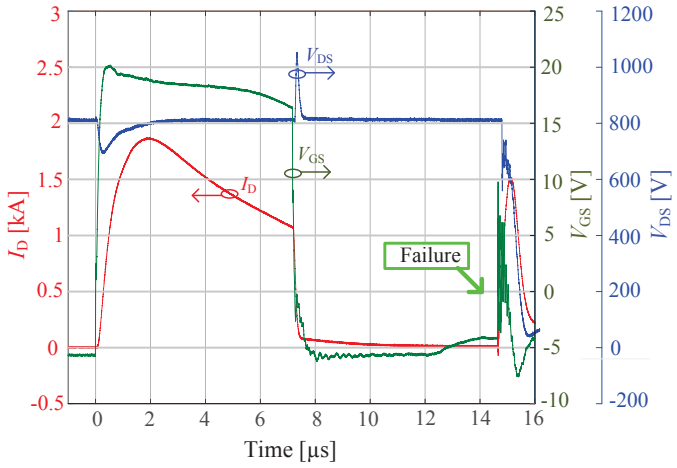

Fig. 6. Short circuit thermal runaway failure of the 1.2 kV/ 180 A SiC MOSFET module within 7.2 μs at V_{DS} = 800 V and T = 25°C.

IV. Short Circuit Safe Operation Area

To safely operate the device under SC events, two SC criteria have been adopted: a) the SC current-based criterion and b) the gate voltage-based criterion. These two criteria have been identified based on the previous experiments on SiC MOSFET power modules.

A. Short Circuit Current-Based Criterion

Based on short circuit failures related to thermal runaway instabilities, an original approach is developed, which relies on the negative dependence between the SC current and the junction temperature [19]. The idea is to define during the short circuit event a drain current level, which corresponds to the maximum allowable junction temperature that the device can withstand up to failure. For instance, in Fig. 4 the critical temperature value which leads into thermal runaway corresponds with a short circuit current of 3 kA. In order to avoid this type of failure, a new method is proposed consisting in applying a short circuit pulse no longer than the one needed to heat it up to the critical temperature. Since the junction temperature of the chip is difficult to measure, a maximum short circuit current level is defined ensuring lower short circuit energy dissipation - the 1.2 kV/ 300 A SiC MOSFET limit is selected to be 4 kA.

To validate that this approach could be implemented as a new method for short circuit protection in the future modern SiC gate drivers, several tests have been done for various DC-link voltages in which the short circuit pulse is not further increased if the short circuit current reaches the selected limit (e.g., 4 kA). Fig. 7a demonstrates that the device operates safely when the short circuit current-based criterion is applied at different DC-link voltages. The driving of these devices becomes critical: it is shown that the higher the DC-link voltage, the shorter pulse length due to the large dissipated power. For instance, the gate driver must be designed to detect

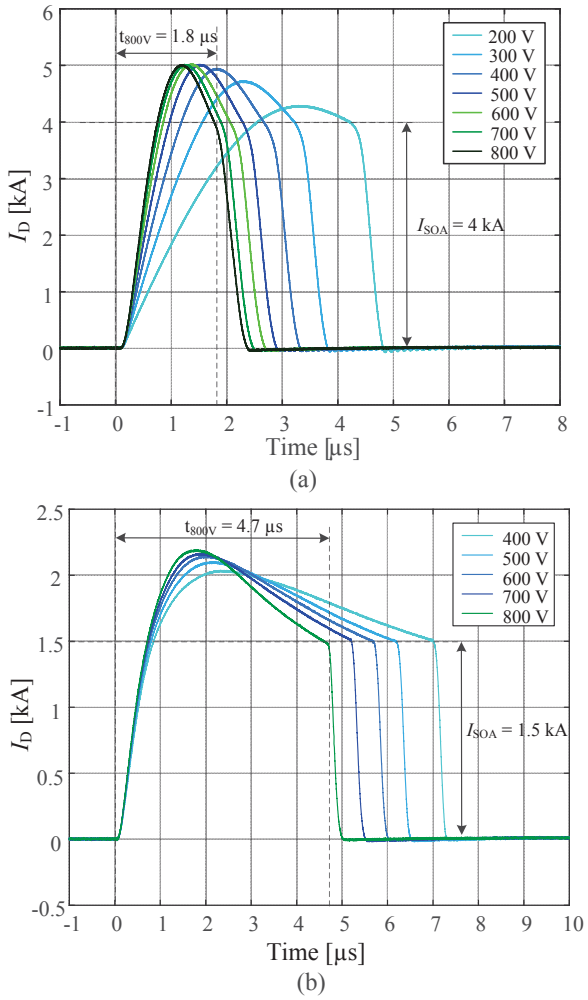

Fig. 7. Validation of the short circuit current-based criterion at different DC-link voltages: (a) the 1.2 kV/ 300 A SiC MOSFET in which the short circuit current limit is 4 kA, and (b) the 1.2 kV/ 180 A SiC MOSFET in which the short circuit current limit is 1.5 kA.

the short circuit condition and protect the device within 1.8 μs at 800 V.

One further verification of the short circuit current-based criterion is given by applying the proposed method to the 1.2 kV/ 180 A SiC MOSFET. As can be seen in Fig 6, the critical temperature value leading into thermal runaway corresponds to a short circuit current of 1 kA. For that reason, the maximum short circuit current level is selected to be 1.5 kA for the 1.2 kV/ 180 A device. Similarly as before, the DUT has been tested under different DC-link voltages without violating the short circuit current-based criterion. Fig. 7b shows the short-circuit robustness when the proposed approach is applied.

B. Gate Voltage-Based Criterion

Based on short circuit failures related with the degradation of the gate oxide, another approach is proposed based on the reduction of the gate voltage level during the short circuit event. The approach consists on defining a gate voltage

level which corresponds with the maximum allowable gate leakage current that the device can withstand up to failure. For instance, in Fig. 6 the final gate voltage value which leads to the gate destruction is about 19.4 V. In order to avoid this failure, a second method is proposed consisting in applying a short circuit pulse no longer than a selected gate voltage value - the 1.2 kV/ 300 A SiC MOSFET limit is selected to be 19.5 V.

The validation of the gate voltage-based criterion is demonstrated in Figs. 8a and 8b for the 1.2 kV/ 300 A SiC MOSFET and the 1.2 kV/ 180 A SiC MOSFET, respectively. Several tests have been done for various DC-link voltages in which the pulse length is not further increased if the gate voltage decreases below the selected limit (e.g., V_{GS} = 19.5 V for the first device and V_{GS} = 19.4 V for the second one). Fig. 8 reveals that the two devices survive if the gate voltage-based criterion is applied at different DC-link voltages. One important aspect is that when the DUTs are tested at low DC-link voltages, i.e., 200 V or 300 V, the gate voltage-based criterion is not met, instead the short circuit current-based criterion has firstly been met and longer short circuit times are not applied.

C. Safe Operation Area Evaluation

In order to identify the operating conditions where the SiC device can survive under a short circuit event, two parameters are usually studied: the SC withstanding time, t_{sc}, and the critical SC energy, E_{crit}. Typically, t_{sc} is around 10 μs at the maximum rated operating temperature, which may be a possible thread for SiC MOSFETs power modules since their SC robustness remains unknown. In this regard, this section will experimentally illustrate the SC capability of the two SiC MOSFET power modules. The Safe Operation Area (SOA) of the DUTs has been formulated based on two original short circuit criteria: (a) the short circuit current-based criterion, I_{SOA}, and (b) the gate voltage-based criterion, $V_{G,SOA}$. Fig. 9 shows the SCSOA of the two studied SiC MOSFET power modules as a function of the drain-source voltage and short circuit time at room temperature. As it can be observed Fig. 9, the short circuit-current based criterion seems to be more restrictive than the gate voltage-based criterion, although at higher DC-link voltages, it is worth to note that the gate voltage-based criterion becomes more crucial. Furthermore, it is noticed that in order to take advantage of SiC MOSFET power modules benefits, more stringent requirements are needed in the design of gate driver fault protection circuits. For instance, if both modules are to be operated at 600 V bias voltage, the gate driver must be able to protect the device within 2 μs for the 1.2 kV/ 300 A DUT and within 5.8 μs for the 1.2 kV/ 180 A DUT as indicated in Fig. 9. From these results, one may judge that the short SC withstanding capability of the SiC power module devices in this study prove to be much less robust than Si IGBT power modules. Nevertheless, the authors would like to emphasize that Si IGBTs do not always fulfil the typical SC withstanding time of 10 μs, as it is demonstrated in [20], [21]. Additionally, for future activities, the SCSOA could also

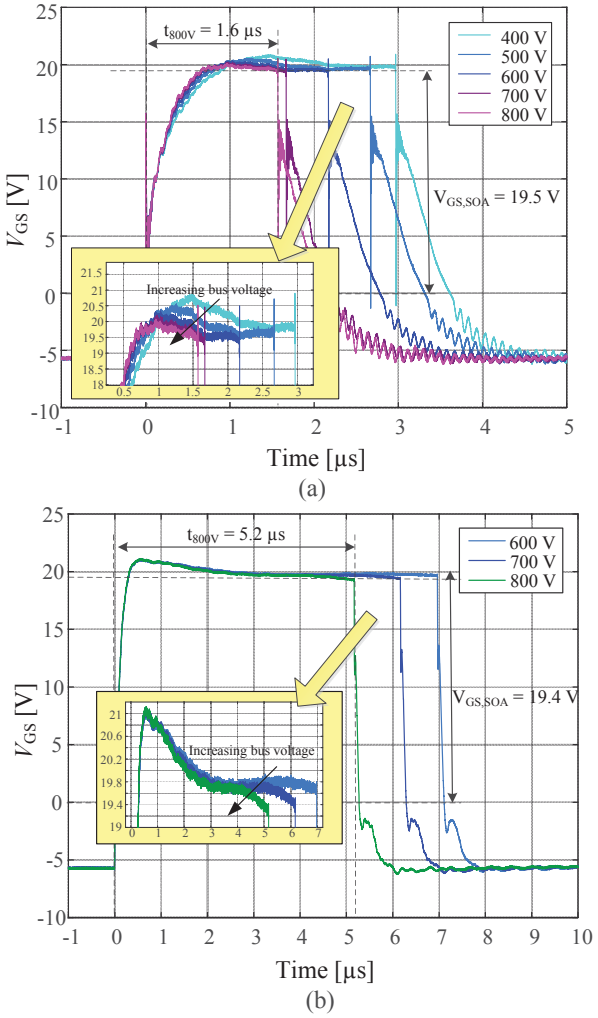

Fig. 8. Validation of the gate voltage-based criterion at different DC-link voltages: (a) the 1.2 kV/ 300 A SiC MOSFET in which the gate voltage limit is 19.5 V, and (b) the 1.2 kV/ 180 A SiC MOSFET in which the gate voltage limit is 19.4 V.

be provided as a function of the initial temperature since it exists a linear restriction of the SCSOA with the operating temperature, as mentioned in [22].

V. Conclusion

In this study an investigation of the SCSOA of commercial 1.2 kV SiC MOSFET power modules is presented by looking at their characteristics, trying to understand potentials and possible limitations, and drawing initial conclusions on how such devices must be operated in order to ensure a good SC withstanding capability. Two failure mechanisms have been observed in this work, which are in agreement with the ones found in the literature for discrete SiC MOSFETs. The first one occurs on both gate and drain terminals due to the high drain leakage current in the off state as a consequence of the high energy dissipated during the short circuit event. A local fusion on the surface metallization of the device is observed when

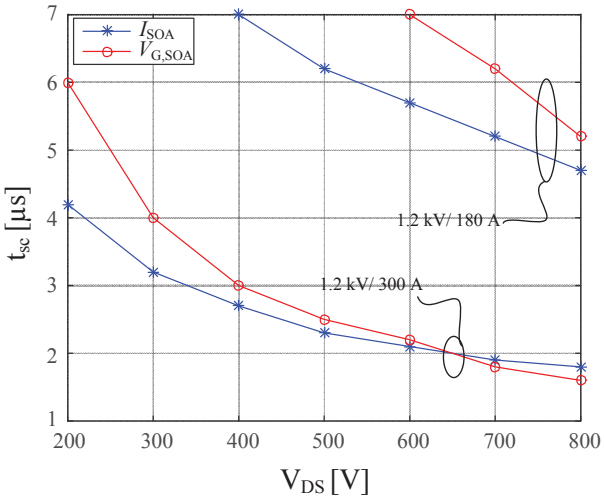

Fig. 9. Short circuit SOA of the two SiC MOSFET power modules based on the two proposed criteria at T = 25°C. I_{SOA} - short circuit current-based criterion and V_{GS} - gate voltage-based criterion.

the module is opened. The second failure occurs in the gate side simultaneously with the destruction between drain and source during the short circuit turn-off. The main contributor is thought to be the high gate leakage current due to degradation of the material properties of the gate oxide, which are more crucial at high temperatures. Based on the observed short circuit failures, two SC criteria have been adopted in order to predict their robustness under short circuit conditions: a) the SC current-based criterion and b) the gate voltage-based criterion. A Safe Operation Area (SOA) of the two studied SiC MOSFET power modules has been drawn by applying the two new methods and thus revealing the short circuit robustness of state-of-the-art 1.2 kV SiC MOSFET power modules. The possibility to implement the above mentioned short circuit criteria in the future SiC MOSFET gate drivers bring new ideas to improve the device robustness against short circuit events.

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