Investigation on Capacitor Switching Transient Limiter with a Three phase Variable Resistance

Naderi, Seyed Behzad; Jafari, Mehdi; Zandnia, Amir; Jalilian, Amin; Davari, Pooya; Negnevitsky, Michael; Blaabjerg, Frede

Published in:
Proceedings of 2017 Australasian Universities Power Engineering Conference (AUPEC)

DOI (link to publication from Publisher):
10.1109/AUPEC.2017.8282395

Publication date:
2017

Document Version
Accepted author manuscript, peer reviewed version

Investigation on Capacitor Switching Transient Limiter with a Three phase Variable Resistance

[1]Seyed Behzad Naderi, [2]Mehdi Jafari, [2]Amir Zandnia, [3]Amin Jalilian, [4]Pooya Davari, [1]Michael Negnevitsky, [4]Frede Blaabjerg

[1]*School of Engineering and ICT, University of Tasmania, Hobart, TAS, 7000, Australia*
[2]*Department of Electrical and Computer Engineering, Michigan Technological University, Houghton, MI, USA*
[3]*Young Researchers and Edit Club, Kermanshah Branch, Islamic Azad University, Kermanshah, Iran*
[4]*The Department of Energy Technology, Aalborg University, Aalborg, Denmark*

***Abstract*—In this paper, a capacitor switching transient limiter based on a three phase variable resistance is proposed. The proposed structure eliminates the capacitor switching transient current and over-voltage by introducing a variable resistance to the current path with its special switching pattern. This topology has high damping capability due to its resistance nature and low voltage drop and low power losses due to complete bypass of its resistor. Therefore, it does not need auxiliary circuit to compensate voltage drop in normal condition. Also, because of smooth bypass of resistance, it does not make transients on capacitor after bypassing. Analytic Analyses for this structure in transient cases are presented in details and simulations are performed by MATLAB software to prove its effectiveness.**

***Keywords*: capacitor bank, capacitor switching transient limiter, power factor correction, switching transient current, variable resistance.**

I. Introduction

POWER capacitors are widely utilised in power systems to compensate load side power factor and improve voltage profile. Most of power system administrators force their industrial customers to install power factor correction capacitors to decrease reactive power consumption. In distribution system, capacity of all installed capacitors is between 25 percent and 30 percent of total load. However, these capacitors make undesired disturbances during transients such as energising, back to back switching and short circuit fault condition. Nowadays, more sensitive loads are connected to power grid and these disturbances can cause malfunction or failure of their performance. In addition, they increase the operation costs of power systems [1]-[4].

There are three cases that capacitors make significant transients in the power system. First case, during energising, large magnitude inrush current with high frequency, which flows from source side to the capacitors, leads to decrease the lifetime of capacitors and series connected equipment such as switching devices. Also, it makes voltage oscillation at Point of Common Coupling (PCC), which causes voltage quality issues for parallel connected loads. Second case, in back to back switching, large current circulates between capacitors in addition to the current coming from the source side. Third case, during short circuit faults in the power system, out-rush current flows through the capacitors, which feeds the fault point [5]-[6].

There are several methods, which have been introduced in literature, to limit the transients associated with the capacitors [7-11]. These techniques can be classified in two main approaches: switching at zero voltage and inserting an impedance in series with the capacitor bank. In first method, source voltage zero crossing is detected and the capacitor is connected to the power system in the zero voltage. Therefore, the capacitor bank does not encounter step change in its terminal voltage and consequently, the transients will not appear in its current. In the approach of using series impedance in the capacitor current path, two types of impedance including resistance and inductance can be employed.

Zero voltage switching requires precise zero-crossing detection at switching time . Furthermore, due to phase difference in three phase voltages, switch closure for each phase should not happen at the same time. So, this approach needs a complicated control system. About the second method, inserting a fixed impedance in series with the capacitor may cause some issues. When the impedance is going to be bypassed, another transient may happen. Also, if an inductance is employed, it can make resonance problem with the capacitor and cause over-voltage on the circuit breaker during de-energising [12]-[14].

To solve these issues, dc inductance type capacitor switching transient limiters have been studied in [13] and [14]. Using the dc inductance cancels out the resonance risk and de-energising over-voltage problem. Also, it does not require to be bypassed. As a result, the dc inductance type capacitor switching transient limiter does not have transient issue. However, the structures using a large dc inductance to properly limit the transients, which results in some other problems. First and foremost, they have considerable power losses due to the large value of dc inductance and its internal resistance. It is important to note that the dc inductance is

always in the current path in these structures. Furthermore, it has significant voltage drop, which leads to necessity of an auxiliary circuit to compensate the voltage drop during normal condition.

Considering these mentioned above discussions, an ideal capacitor switching transient limiter should have the following characteristics: high limiting and damping capability of transient current, smooth bypass in order to avoiding another transient, and low power loss and voltage drop during normal condition. In this paper, a three phase variable resistance type capacitor switching transient limiter (VR-CSTL) is proposed. The proposed structure inserts a high resistance to the current path at the beginning of switching, and then changes its value in a descending rate to zero for smooth bypass. This structure is capable of limiting transient current's peak and fast damping of those transients. In the proposed approach, the source side voltage does not experience high disturbances and then, the voltage quality could be improved. The VR-CSTL has low power losses due to bypassing the resistance in normal condition and also does not have the transient issue when its resistance is going to be bypassed.

II. Power Circuit Topology of the Proposed VR-CSTL and Principles of Operation

A. Power Circuit Topology the proposed VR-CSTL

The three phase power circuit topology of the proposed VR-CSTL is shown in Fig. 1. This structure is composed of four main parts, which are described as follows:

1) The three phase isolation transformer;
2) The three phase diode rectifier bridge;
3) A semiconductor switch (*SW*), which is in parallel connection with a large resistance (*R*). This is the main component of the VR-CSTL, which plays the main current limiting characteristic.
4) And finally, a small dc inductance to prevent sever *di/dt* on the semiconductor switch. Because of its very small value, it can be designed with air core to prevent its saturation and it has very low power losses. In addition, it does not cause considerable voltage drop. Therefore, this structure does not require the auxiliary circuit to compensate the voltage drop compared to [14].

The isolation transformer is required to direct the line current to the current limiting part. The three phase diode bridge is ac/dc converting tool for the VR-CSTL. Parallel connection of the resistance *R* and the semiconductor switch is expected to generate a variable resistance with special switching pattern during capacitor switching instant.

B. Principles of Operation

The main idea of this structure is to generate a variable resistance during capacitor switching transients with special switching pattern. When the transient current, which is caused by the capacitor switching, is detected, the proposed VR-CSTL inserts a high resistance value to the current path.

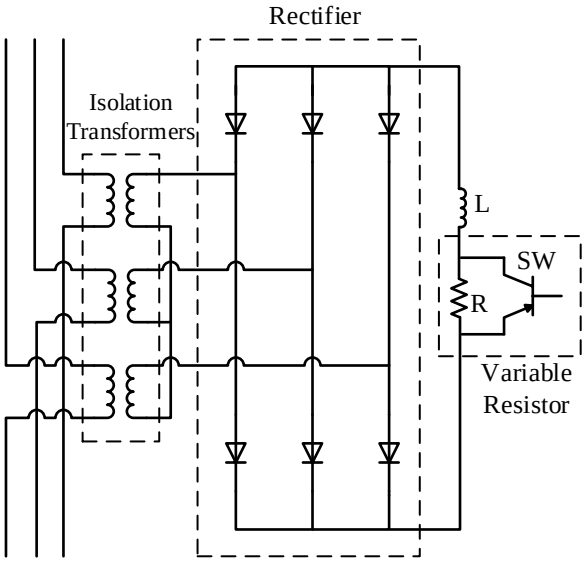


Fig. 1. Power circuit topology of the proposed VR-CSTL.

The switching pattern of the structure is to decrease equivalent series resistance and bypass it with a ramp rate to make a smooth retreat.

To illustrate the operation principle of the proposed structure, it is assumed that the voltage drop on the small dc inductance is negligible. So, after detecting the capacitor switching transient, dc side voltage will drop on variable resistor part of structure as follows:

$$V_{dc} = \frac{6}{\pi}\sin(\frac{\pi}{3})aV_p \tag{1}$$

whereby, V_p and a are the peak of ac side voltage and the isolation transformer ratio, respectively. The resistance appears in the dc side due to switching can be written as follow:

$$R_{dc} = (1-D)R \tag{2}$$

whereby, D is the duty cycle of the semiconductor switch, which can be any function of time. It is important to note that the resistance value in the dc side of the rectifier bridge is different from its ac side value. By neglecting power losses in the isolation transformer and the diodes in the rectifier bridge and regarding the equality of active power in the ac and the dc sides, it is possible to calculate the equivalent resistance value, which appears in the capacitor switching transient current path as follow:

$$\frac{3}{2}\frac{V_p^2}{R_{ac}} = \frac{\frac{6}{\pi}\sin(\frac{\pi}{3})aV_p}{R_{dc}} \tag{3}$$

Therefore, the following expression can be concluded:

$$R_{ac} = \left(\frac{\pi^2}{18a^2}\right)R_{dc} \tag{4}$$

Equations (2) and (4) indicate that with a fixed resistance value and a time-variable duty cycle, it is possible to generate the variable resistance in terms of the time-variable duty cycle

from power system point of view. Control system for the proposed VR-CSTL to generate the variable resistance is shown in Fig. 2. The dc side current is measured and compared to a reference value, which is maximum permissible current in the power system. It should be noticed that the dc current is the peak of the ac current flowing to the capacitor bank. If the current exceeds the reference value, it is considered as a transient case and the semiconductor switch starts switching with the predefined switching pattern. An ascending ramp is defined for the duty cycle value, which is compared to a carrier wave with high switching frequency to generate gate signals of the semiconductor switch. Fig. 3 shows the ramp function for the duty cycle and related gate signal for the switch. By this switching method, a descending resistance will appear at the transient current path from it maximum value to zero and suppress the current effectively.

III. Analytic Analysis of the Proposed VR-CSTL

To analyse the operation of structure, it is assumed that the VR-CSTL is located at connecting line of the capacitor bank. In this case, equivalent circuit can be derived as Fig. 4. The expression describing circuit current *i* can be written as follow:

$$\frac{d^2i}{dt^2}+\frac{R_T}{L_T}\frac{di}{dt}+\frac{1}{L_TC}i=-\frac{\omega V_m}{L_T}\sin(\omega t) \quad (5)$$

where, $R_T=R_{source}+R_{line}+R_{ac}$, $L_T=L_{source}+L_{line}+L_{Transf.}$, ω is source angular frequency and V_m is the source voltage peak. It should be mentioned that the source voltage is sinusoidal wave. But due to the high frequency of capacitor switching transients compared to the power system frequency, it can be considered as a dc voltage during the transient interval. By solving (5), the transient current can be expressed as follow:

$$i(t)=Ae^{-\alpha t}\cos(\omega_d t)+B\cos(\omega t-\varphi) \quad (6)$$

where

$\alpha=R_T/2L_T$, $\omega_0=1/\sqrt{L_TC}$, then, $\omega_d=\sqrt{\omega_0^2-\alpha^2}$,

$\varphi=\tan^{-1}\left(\frac{L_T\omega}{R_T}-\frac{1}{R_TC\omega}\right)$, $B=\frac{\omega V_m}{\sqrt{(L_T\omega^2-\frac{1}{C})^2+{R_T}^2\omega^2}}$, and

$A=-B\cos(\varphi)$.

Equation (6) reveals three important characteristics about the capacitor transient current, which includes the transient current peak value, frequency of oscillations and damping ratio. The peak of transient current flowing to the capacitors and its damping ratio are function of *R*. By increasing the *R*, the current magnitude decreases and it will be damped in less time. Meanwhile, the oscillation frequency will be decreased with *R*. The voltage of capacitor terminal can be written as (7). This voltage will have some transient oscillations in terms of the circuit's natural frequency due to energising. However, increasing the *R* changes the transient oscillation frequency from the under-damped frequency to critically damped or over-damped frequency.

$$v_C(t)=Ae^{-\alpha t}\left[\frac{\omega_d}{{\omega_d}^2+\alpha^2}\sin(\omega_d t)-\frac{\alpha}{{\omega_d}^2+\alpha^2}\cos(\omega_d t)\right]+\frac{B}{\omega}\sin(\omega t-\varphi) \quad (7)$$

The same equations can be written for the back to back switching mode. Because of adding a capacitor with initial charge to the circuit as shown in Fig. (5), the difference is in the peak of transient current and its frequency.

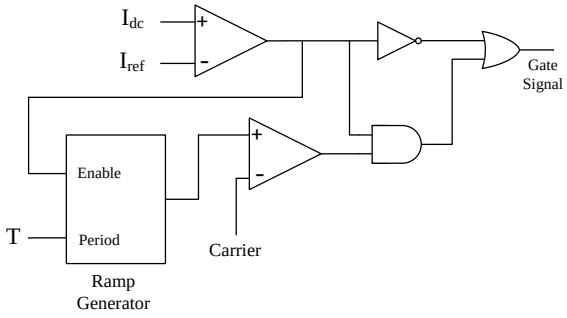


Fig. 2. Control system of the proposed VR-CSTL.

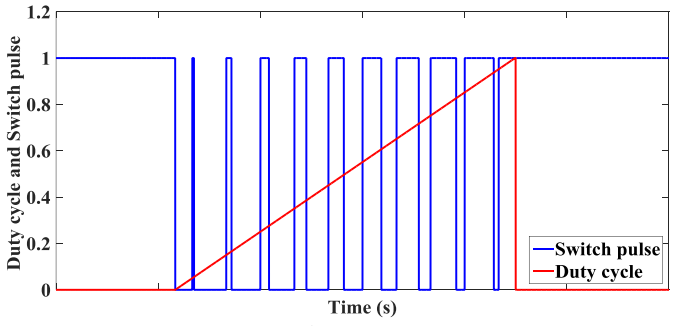


Fig. 3. Duty cycle and gate signal of the semiconductor switch.

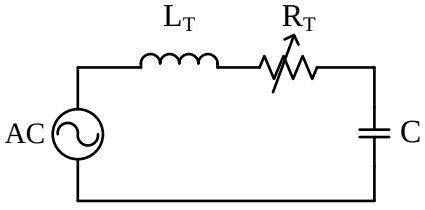


Fig. 4. Equivalent circuit of the capacitor energising with the proposed VR-CSTL.

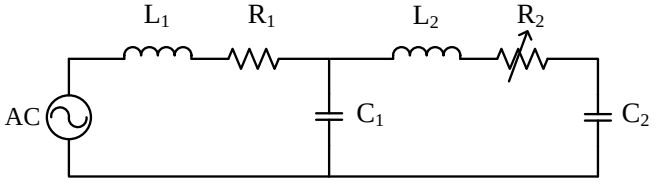


Fig. 5. Equivalent circuit of the back to back switching with the proposed VR-CSTL.

IV. SIMULATIONS

Simulations are carried out in MATLAB on the power circuits of Fig. 6(a) and 6(b). Table I shows the parameters of simulation. To study the performance of the proposed VR-CSTL on limiting the capacitor switching transients, two case studies are considered in the simulation:

Case (A): Energising a single capacitor bank;

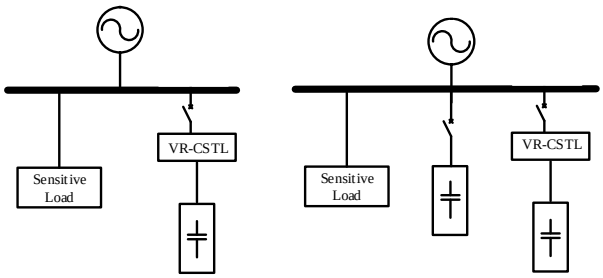
Case (B): Energising a capacitor bank while parallel capacitors are connected (back to back switching).

In case A, a circuit breaker connects the capacitor bank to the grid at the peak of source voltage to make the worst condition from the switching transient's point of view. Fig. 7(a) and 7(b) show the capacitor transient current without and with using the VR-CSTL, respectively. As shown in these figures, the transient current peak is limited from about 6p.u. to 1.5p.u. and it is also damped in shorter time due to the resistance added to the circuit by the VR-CSTL. Small distortions, which are appeared on the current, are mostly due to switching of the resistance. Effective limiting the transient currents results in improving the voltage quality in the connected bus, which is shown in Fig. 8(a) and 8(b). Bus voltage without using the VR-CSTL has high frequency oscillations with first peak of more around 2p.u. (Fig. 8 (a)). But, utilising the proposed structure eliminates the voltage transient and very small distortion appears on the voltage waveform (Fig. 8 (b)), which could protect the parallel loads from the voltage quality issues.

Fig. 9(a) and 9(b) show the voltage of capacitor terminal before and after using the VR-CSTL. By employing the proposed structure, the capacitor will not experience over-voltages during energising. As before mentioned, the capacitor transient current and over-voltages would decrease its lifetime. In fact, limiting these transients aids to prevent its failure.

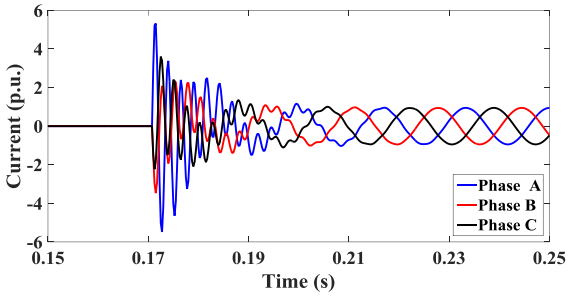
Table I. Simulation parameters

Power system parameters	***Source***	220V, rms, L-L, 60Hz, X=1mH, R=0.1 Ω
	Connecting cables	X=0.1mH, R=0.05 Ω
	Capacitor banks	50uF, 250kVAR, Delta connection
The VR-CSTL data	***dc side parameters***	R=10Ω, L=1mH, VDF=0.9V, Vsw=1V
	Isolation transformer parameters	10kVA, a=1, X=0.1p.u.

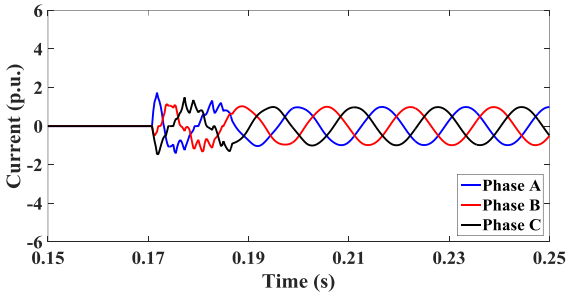


(a) (b)

Fig. 6. Simulation power circuits: (a) the energising condition, (b) back to back switching condition.

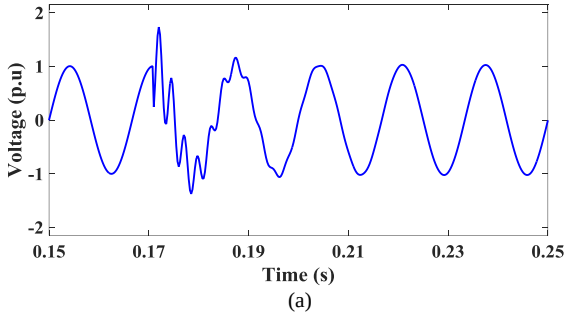


(a)

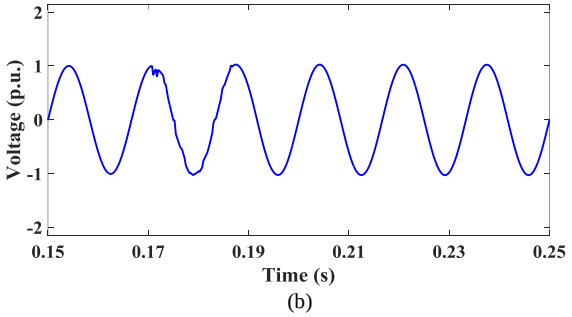


(b)

Fig. 7. The capacitor current (a) without and (b) with employing the VR-CSTL.



(a)



(b)

Fig. 8. Bus voltage (a) without and (b) with using the VR-CSTL.

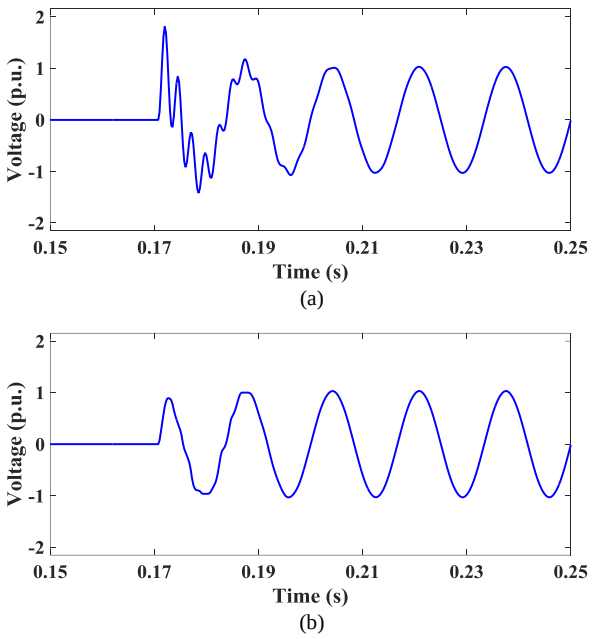


Fig. 9. Capacitor terminal voltage (a) without and (b) with using the VR-CSTL.

In case B of the simulation, the back to back switching of capacitor banks in considered. In this case, capacitor *C1* is connected to the system and the circuit breaker connects the capacitor *C2* to the power source. Fig. 10(a) and 10(b) show the capacitor *C2* current with and without the VR-CSTL. The capacitor *C2* current has two transient parts, one from the source and other from the capacitor *C1*. So, it has higher peak more than 10p.u. and higher oscillation frequency due to changing the natural frequencies of the circuit (Fig. 10 (a)). However, employing the VR-CSTL limits the transient current peak to almost 1.2p.u. and damps it in less time (Fig. 10 (b)).

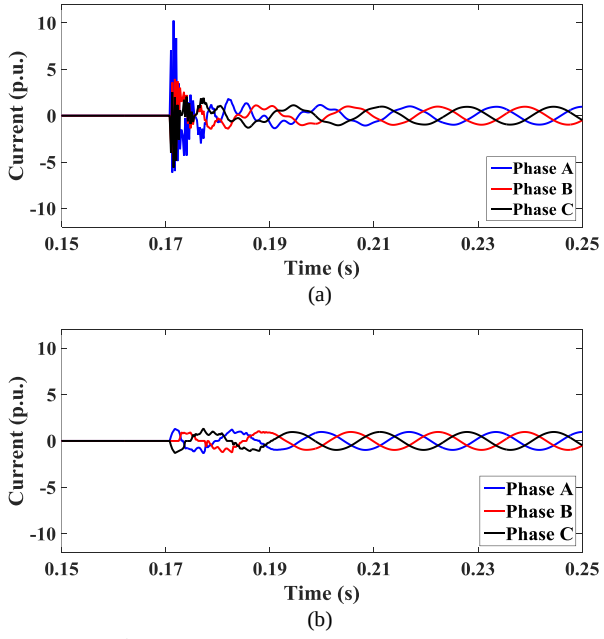


Fig. 10. Current of capacitor C2 (a) without and (b) with using the VR-CSTL.

Also, in this case, using the VR-CSTL limits the current transients of capacitor *C1* as shown in Fig. 11(a) and 11(b).

For the source side voltage, the VR-CSTL could reduce the transient over-voltages on the connected bus and improve the voltage profile as shown in Fig. 12(a) and 12(b). Capacitor *C2* voltage will also experience less transient over-voltages (Fig. 13(a) and 13(b)).

Considering the presented figures, the proposed VR-CSTL could effectively restrict the transient currents and the over-voltages in both case studies and enhance the bus voltage quality on one hand and capacitor bank's lifetime on the other hand. In addition, reliability of the switchgear operation will increase by utilising the proposed structure.

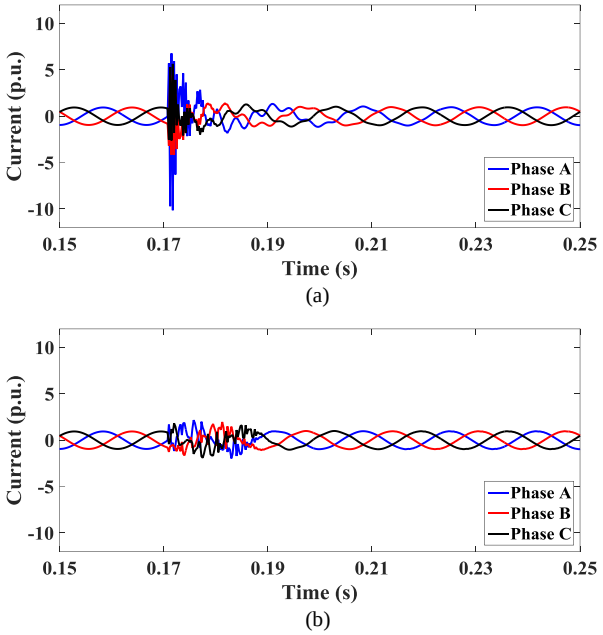


Fig. 11. Current of capacitor C1 (a) without and (b) with using the VR-CSTL.

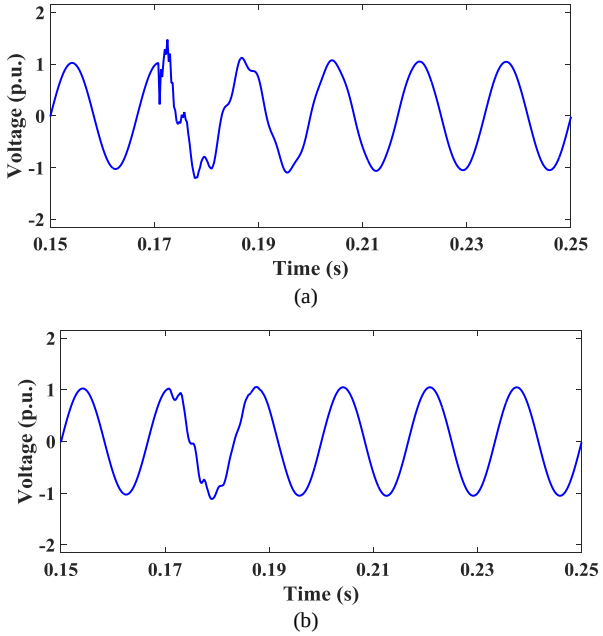


Fig. 12. Connected bus voltage (a) without and (b) with using the VR-CSTL.

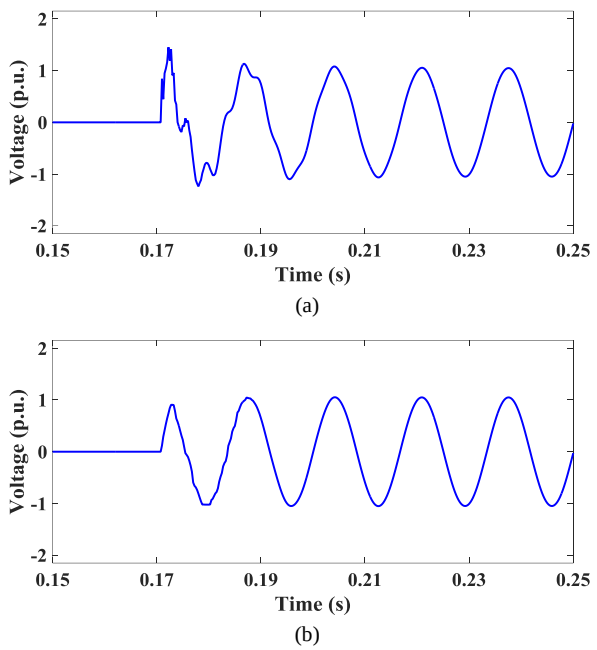


Fig. 13. Capacitor C2 terminal voltage (a) without and (b) with using the VR-CSTL

V. Conclusion

In this paper, a variable resistance type capacitor switching transient limiter is proposed. This structure inserts a variable resistance to the transient current path with the special switching pattern and limits the current peak and quickly damps it. Because of the resistive nature of this structure, the proposed VR-CSTL is capable of quick damping. Also, the special switching method eliminates the transients, when the resistance of the VR-CSTL is going to be bypassed. Meanwhile, during normal operation, due to complete bypass of the resistance and very small value of the dc inductance, the proposed approach has lower power loss and voltage drop compared to other structures. Therefore, it does not need any auxiliary circuit to compensate the voltage drop in normal condition. Analytical analyses and the simulations indicate the effective performance of the proposed VR-CSTL in both the energising and the back to back switching cases. In general, the VR-CSTL is able to limit the capacitor transients in an acceptable way and improve the voltage quality of the connected distribution bus.

References

[1] T. M. Blooming and D. J. Carnovale, "Capacitor application issues," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1013–1026, Jul./Aug. 2008.

[2] S. B. Naderi, M. Jafari, M. Tarafdar Hagh, "Parallel Resonance Type Fault Current Limiter," *IEEE Trans. Ind. Electron.* Early Access, 2012.

[3] B. Moridian, D. Bennett, N. Mahmoudian, W. W. Weaver, and R. Robinnett, " Autonomous Power Distribution System: Path planning and Control," in proc. 19th *International Federation of Automatic Control (IFAC)*, vol. 19, part. 1, pp 7-12, 2014.

[4] M. T. Hagh, M. Jafari, S. B. Naderi, "Controllable resistive type fault current limiter (CR-FCL) with frequency and pulse duty-cycle," *International Journal of Electrical Power and Energy Systems*, vol. 61, pp. 11–19, 2014.

[5] J. L. Dur´an-G´omez and P. N. Enjeti, "A new approach to mitigate nuisance tripping of PWM ASDs due to utility capacitor switching transients (CSTs)," *IEEE Trans. Power Electron.*, vol. 17, no. 3, pp. 799–806, Sep.2002.

[6] T. E. Grebe, "Application of distribution system capacitor banks and their impact on power quality," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 714–719, May/Jun. 1996.

[7] IEEE Guide for Application of Shunt Power Capacitors, IEEE Standard 1036-2010, Jan. 2011.

[8] J. C. Das, "Analysis and control of large-shunt-capacitor-bank switching transients," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1444–1451, Nov. 2005.

[9] S. G. Abdulsalam and W. Xu, "Sequential phase energisation technique for capacitor switching transient reduction," *Inst. Eng. Technol. Gen. Transmiss. Distrib.*, vol. 1, no. 4, pp. 596–602, Jul. 2007.

[10] Teymoor Ghanbari, Ebrahim Farjah, Amir Zandnia, "Solid-state transient limiter for capacitor bank switching transients," *IET Gener. Transm. Distrib.*, vol. 7, Iss. 11, pp. 1272–1277, 2013.

[11] J. C. Wu, H. Jou, K. Wu, and N. Shen, "Hybrid Switch to Suppress the Inrush Current of AC Power Capacitor," *IEEE Trans. Power Deliv.*, vol. 20, no. 1, Jan. 2005.

[12] S. Tseng, J. Chen, and T. Liang, "Symmetrical Structure Transient Limiter for Suppression of Capacitor Switching Transients," *IEEE Trans. Power Deliv.*, vol. 26, no. 4, Oct. 2011.

[13] S.-T Tseng, J.-F. Chen, "Capacitor energising transient limiter for mitigating capacitor switch-on transients," *IET Electr. Power Appl.*, vol. 5, iss. 3, pp. 260–266, 2011.

[14] H. Tseng and J. Chen, Single-DC Reactor-Type Transient Limiter for Reducing Three-Phase Power Capacitor Switching Transients," *IEEE Trans. Power Electron.*, vol. 27, no. 4, Apr. 2012.