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Correction for Metastability in the Quantification of PID in Thin-Film Module Testing

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***Abstract* — A fundamental change in the analysis for the accelerated stress testing of thin-film modules is proposed, whereby power changes due to metastability and other effects that may occur due to the thermal history are removed from the power measurement that we obtain as a function of the applied stress factor. In this work, initial thermal treatment of the module is performed before application of the independent variable stress of system voltage so that any temperature–dependent processes (*e.g.*, diffusion) that affect the module power are largely activated beforehand. Secondly, the power of reference modules normalized to an initial state—undergoing the same thermal and light exposure history but *without* the applied stress factor such as humidity or voltage bias—is subtracted from that of the stressed modules. For better understanding and appropriate application in standardized tests, the method is demonstrated and discussed for potential-induced degradation testing in view of the parallel-occurring but unrelated physical mechanisms that can lead to confounding power changes in the module.**

***Index Terms* — potential-induced degradation, PID, CdTe, thin-film modules, high voltage**

I. Introduction

A frequently sought-after goal when testing thin-film modules is achieving some common comparison point for evaluation. This is usually standard test conditions (STC, 25°C, 1000 W/m^2 irradiance), achieved by a conditioning or "stabilization" step [1]. IEC 61215 ed. 3 Module Quality Test (MQT) 19 describes applying 800 W/m^2 to 1000 W/m^2 with the module temperature at 50 °C ± 10 °C until the module power is deemed not to change within 2% [2]. Electrical characteristics of CIGS and CdTe modules are observed to undergo performance changes known as metastability, which have been associated with charging-discharging of defects states [3,4]. Additionally, power changes due to ion transport based on the stresses applied to the module may occur. Cu at the back contact of the CdTe module can improve the contact with the wide-bandgap p-CdTe layer and it is known to form Cu_{Cd} acceptor-state levels, which increase the carrier density such that higher open-circuit voltage (V_{oc}) is obtained [5]. However, stability or power performance can also degrade as Cu diffuses through grain boundaries to the CdTe/CdS interface [6]. It may be desired to separate such mechanisms when one is trying to study mechanisms specific to the applied stress factors, such as with the effect of damp heat or system voltage stress.

Additionally, it has been shown that the open-circuit condition can accelerate positive Cu^+ ion migration toward the junction, leading to power loss [6,7]. Efficiency loss is less for CdTe cells held at 100°C biased to maximum power (P_{max}) or in short circuit than in open circuit [7]. Similar trends have been reported in fielded modules [6]. Therefore, the state of loading or bias on the module can influence how ions migrate into regions of the absorber layer.

The MQT 19 stabilization process may not sufficiently recover the degradation from the dark heat soaks that accompany many chamber stress tests. Such power changes particular to the specimen and its history make it difficult to measure the effect of the specific environmental stress factor applied. For example, it has been shown that there is degradation of STC power in CIGS modules after placing them unbiased in 85°C dark heat that the MQT 19 stabilization process cannot recover [8]. It was found that the degradation might be mistakenly assigned to the humidity in damp heat testing if the effect of the heat is not specifically controlled and consideration to the junction bias is not given.

Basic experimental procedure involves (1) an *independent variable* that is deliberately changed; (2) a *dependent variable* whose outcome is measured as a function of the independent variable; and (3) *control variables*, which can affect the outcome and need to be kept constant if possible, or else carefully monitored so that their influence on the dependent variable can be quantified [9]. In this vein, MQT 19 performed before and after stress testing presents at least two concerns. First, the MQT 19 temperature of 50°C ± 10°C is insufficient to activate processes that may occur at a subsequent 85°C temperature level occurring in (for example) the following IEC 61215 stress tests. Consequently, any control variables that are activated at 85°C will not be maintained as constant during the stress tests. Second, after potential-induced degradation (PID) stress tests, slow thermal recovery has been observed in some CIGS modules [10]. Application of IEC 61215 MQT 19 to regenerate power loss associated with metastability may also recover losses due to PID to some extent making it difficult to evaluate the PID independently from the metastability.

MQT 19 represents a relatively high insolation and temperate module field condition, omitting real stress factors that exist in fielded modules such as system voltage that drives PID. Many environments can be damp, cold, and have relatively low insolation, not at all represented by MQT 19 conditions. It is of interest to understand the extent of PID

power loss resulting from application of a PID stress test before recovery, as well as the potential to recover. Therefore, deconvolution of PID recovery from metastability recovery during application of MQT 19 requires attention.

In this work, we discuss procedures to address the above concerns for the stress testing of thin-film modules. To better isolate the control variables, unbiased modules as references or controls are placed alongside and compared with high-voltage biased modules for characterizing PID degradation. The extent of PID exhibited and any PID recovery is clearly quantified by separation from other effects in CdTe modules including metastabilities and copper diffusion. The concepts presented here are anticipated to be applicable to standardized testing, including for quantification of PID in thin-film modules.

II. Experiment

A commercial CdTe thin-film module type of double-glass and edge-seal construction was used. Three modules were processed according to the sequence shown in Fig. 1. At the damp heat stage, one module was stressed with -1000 V applied to the shorted modules leads, another with +1000 V, and the third in open circuit without any voltage applied. Stabilization was performed with a light chamber according to IEC 61215-2 MQT 19. Subsequently, dark dry-heat soaks were performed in environmental chambers at 55°C [11] and less than 5% relative humidity (RH). Flash testing was performed at STC conditions. PID stress tests were performed in damp heat at 85°C and 85% RH with an apparatus previously described [12]. Key points in the process indicated in Fig. 1 include L_0, the flash tester-determined power measurement after the initial light-stabilization procedure (MQT 19) with temperature 50°C ± 10°C; D_0, after the 55°C dry dark soak; D_n, post-stress dark-state measurements; D_r, after a thermal-recovery step; and L_n, module power measurement after light stabilization. Flash testing during environmental chamber procedures was performed in stages at about one-week intervals, with some exceptions.

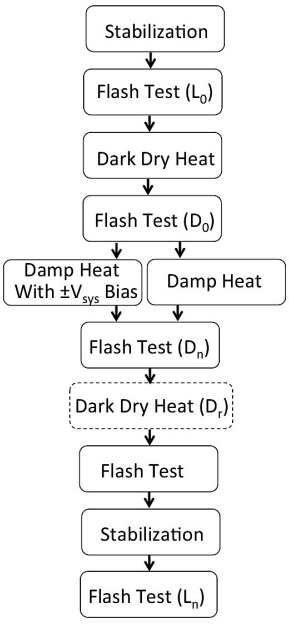

Fig. 1. Process sequence.

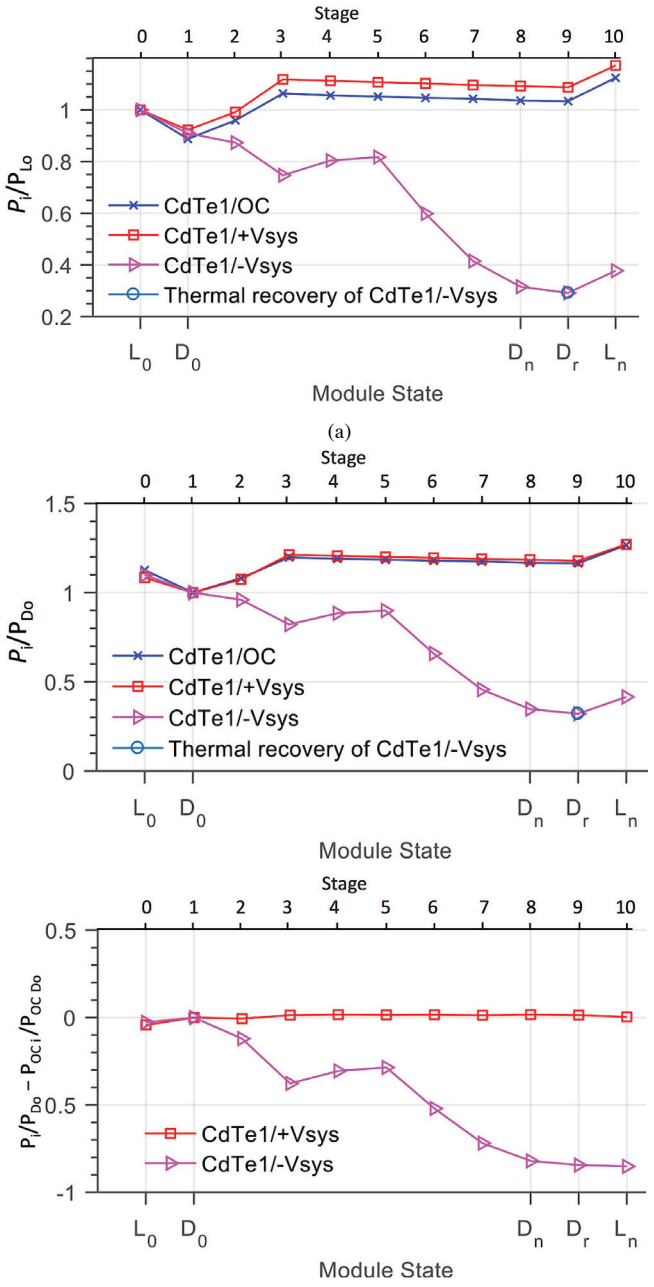

Fig. 2. Two CdTe modules undergoing PID stress testing and one in-chamber unbiased reference module in open circuit at various testing states. The indicated stage numbers represent approximately weekly flash test measurements. The x-axis labels L_0, D_0, D_n, D_r, and L_n correspond to steps in the process as indicated in Fig. 1. System voltage, V_{sys}, (+ or - 1000 V) was applied at D_0 and released at D_n. (a) Module power normalized to their value after initial stabilization L_0, (b) module power normalized to their value after dark dry-heat D_0, and (c) fraction power change of the PID-stressed modules relative to the unbiased in-chamber reference module based the D_0 -normalized data in Fig 2(b).

III. Results and Discussion

Figure 2 shows the results of the sequence in Fig. 1 applied to CdTe modules. The three samples indicated are either in open circuit (OC) or have positive or negative 1000 V bias applied to the module leads, which are respectively labeled as $+V_{sys}$ and $-V_{sys}$. Figure 2(a) shows the results for the module power normalized to their values at L_0, whereas Fig. 2(b) shows the results normalized at D_0. It can be seen in both the OC sample and the sample with $+V_{sys}$ stress applied (a non-PID-sensitive configuration that closely follows the power of the unbiased OC module) that there is an initial decrease in power during the dark dry heat process associated with metastability followed by a net increase in power up to the measurement at stage 3. The extent of the power decrease from L_0 to D_0 due to metastability appears to vary in Fig. 2(a).

To isolate this control variable associated with metastability for the study of the subsequent PID, it is beneficial to view the data normalized to each module's power at point D_0 after the dark dry heat soak as shown in Fig. 2(b). As discussed in the introduction, the initial net increase in power seen in the OC and $+V_{sys}$ samples up to stage 3 in the testing may be attributed to net acceptor formation. V_{oc} was measured to increase about 4% with markedly increased electroluminescence intensity attributable to the increased net carrier density [5]. This is followed in these two samples by a slow, steady decline in power—degradation associated with a fill factor drop of about 2.6% to the D_n point is seen, attributable to Cu diffusion to the junction. After the application of 1000 V to the $+V_{sys}$ and $-V_{sys}$ samples just after D_0, only the $-V_{sys}$ sample appears to degrade by PID.

It is critical to recognize that the V_{oc} increase, attributed to the Cu incorporation to form additional carriers in the p-CdTe layer, was not achieved with the initial light stabilization at the L_0 point, likely due to the insufficient high temperature (50°C ± 10°C). On the other hand, we can see the relative stability in the OC and $+V_{sys}$ samples after stage 3 at 85°C, whereby the copper incorporation to the acceptor state, a control variable in this case, has been isolated. In this experiment, we applied bias before completely maximizing the copper incorporation to the acceptor state. For better isolation of this control variable, application of the bias and placing D_0 at stage 3 would be more appropriate.

After the PID stress testing, attempts for thermal recovery (85°C) of the PID in the $-V_{sys}$ sample between D_n and D_r did not result in increased power; but instead, additional degradation occurred, attributable to continued Cu diffusion to the junction. For the final IEC 61215-2 MQT 19 stabilization step between D_r and L_n it can be seen that the increase in power of the PID-degraded sample under $-V_{sys}$ bias and the non-PID producing conditions, $+V_{sys}$ and OC, are all of about the same magnitude. Also taking into account that thermal PID recovery did not occur between D_n and D_r, it is likely that the power increase with stabilization at L_n is associated with metastability rather than PID recovery in this module type.

A solution for dealing with these unisolated control variables for determining the actual power loss due to PID is to measure the power change relative to the in-chamber reference module undergoing damp heat without applied bias. The change in power of the CdTe modules in the $+V_{sys}$ and $-V_{sys}$ configurations relative to the unbiased modules is shown in Fig. 2(c). The $-V_{sys}$ module data, for example, are calculated at each stage i as $P_{\text{-Vsys},i}/P_{\text{-Vsys, Do}} - P_{\text{OC},i}/P_{\text{OC, Do}}$. Viewing the data in this way, we first see the fractional power loss in the PID-stressed modules devoid of the influence of the control variables, such as the effect of Cu_{Cd} acceptor-state formation and Cu diffusion into the junction. The $+V_{sys}$ biased module, despite the varying power measured over the course of the PID stress test, is absolutely flat in Fig. 2(c) after the D_0 normalization point where the voltage bias was applied. This clarifies that the $+V_{sys}$ polarity does not produce PID. This further gives us confidence that the signal we are seeing in the $-V_{sys}$ biased module is free of effects of control variables and representative of the actual PID. Secondly, we can see that there is no PID recovery in the PID-affected module after the adjustment that was made in Fig. 2(c)—the increase in power we see in Figs. 2(a) and 2(b) at the L_n stage is consistent with the other samples, and therefore, attributable largely to reversible components of metastability.

Based on previously published results [7], isolation of the control variable associated with copper diffusion into the junction over the course of testing leading to fill factor degradation may also be addressed to an extent by applying forward bias voltage or light during the course of the PID stress test. These possibilities are included in the draft standard IEC 62804-2 "Test methods for the detection of potential-induced degradation – Part 2: Thin film." However, these require careful consideration of current and load because placing the cells in forward bias during 85°C tests has been shown to cause additional degradation in some cases; e.g., with the module maintained at maximum power [13] or illuminated and in short circuit [8]. Further, application of light while maintaining the prescribed RH uniformly on the module surface during a damp-heat test may be experimentally challenging because of the required irradiance and temperature uniformity. Further studies on the behavior of light and voltage bias over the junction during PID stress tests are under way.

III Summary and Conclusions

There are multiple factors affecting the power that we measure from thin-film modules over the course of stress tests. To better isolate control variables such as metastability, contact annealing, and Cu migration from an independent variable such as system voltage stress, this paper proposes the following:

1) Insert a dry-heat step at or above the stress temperature before application of the intended stress factor or independent

variable (e.g., humidity, voltage bias) to precipitate beforehand processes that will occur at the eventual stress temperature.

2) Because of unisolated control variables leading to, for example, power increases during testing, use reference modules (*in-situ* controls) that follow the samples through the test process omitting only the key independent variable (e.g., system voltage), so that the effect of the intended stress can be better gauged.

3) As necessary, include light or forward-bias voltage during the stress test to maintain the junction of the cells in a field-representative configuration and to isolate controlled variables such as Cu ion migration to the junction in CdTe modules. However, careful analysis is required so that degradation or enhancement of power is not additionally introduced.

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REFERENCES

[1] C.A. Deline, J.A. del Cueto, D.S. Albin, S.R. Rummel, J. *Photon. Energy* 2(1) 022001 (2012).

[2] Terrestrial photovoltaic (PV) modules – Design qualification and type approval – Part 2: Test procedures, International Electrotechnical Commission, Geneva (2016).

[3] M. Igalson, M. Cwil, M. Edoff, *Thin Solid Films* 515, 6142–6146 (2007).

[4] P. Zabierowski, U. Rau, M. Igalson, *Thin Solid Films* 387, 147–150 (2001).

[5] S.H. Demtsu, D.S. Albin, J.R. Sites, W.K. Metzger, A. Duda, *Thin Solid Films* 516 (8), 2251–2254 (2008).

[6] N. Strevel, L. Trippel, M. Gloeckler, *Photovol. International* 17, 1–6, (2012).

[7] C.R. Corwine, A.O. Pudov, M. Gloeckler, S.H. Demtsu, J.R. Sites, *Solar Energy Materials & Solar Cells* 82(4), 481–489 (2004).

[8] K. Sakurai, K. Ogawa, H. Shibata, A. Masuda, EU PVSEC 2016, 20–24 June 2016, Munich (5DO.10.3)

[9] A. Rubin, *Statistics for Evidence-Based Practice and Evaluation*, Brooks/Cole Cengage Learning, 2013.

[10] S. Yamaguchi, S. Jonai, K. Hara, H. Komaki, Y. Shimizu-Kamikawa, H. Shibata, S. Niki, Y. Kawakami, A. Masuda, *Jap. J. Appl. Physics* 54, 08KC13 (2015).

[11] The 55°C dark heat soak was performed at a lower temperature than the subsequent PID stress temperature of 85°C. As it will be shown, the dark heat soak should have preferably been performed at or above the eventual stress temperature to activate any temperature-dependent processes before the subsequent stress test.

[12] P. Hacke, K. Terwilliger, R. Smith, S. Glick, J. Pankow, M. Kempe, S. Kurtz, 37th IEEE PV Specialists Conference, Seattle, WA, 814–820 (2011).

[13] P. Hacke, K. Terwilliger, S.H. Glick, G. Perrin, J. Wohlgemuth, S. Kurtz, K. Showalter, J. Sherwin, E. Schneller, S. Barkaszi, R. Smith, *J. Photonics Energy* 5, 053083 (2015).