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Three-Phase Phase-Locked Loop Synchronization Algorithms for Grid-Connected Renewable Energy Systems: A Review

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Abstract

The increasing penetration of distributed renewable energy sources (RES) requires appropriate control techniques in order to remain interconnected and contribute in a proper way to the overall grid stability, whenever disturbances occur. In addition, the disconnection of RES due to synchronization problems must be avoided as this may result in penalties and loss of energy generation to RES operators. The control of RES mainly depends on the synchronization algorithm, which should be fast and accurately detect the grid voltage status (e.g., phase, amplitude, and frequency). Typically, phase-locked loop (PLL) synchronization techniques are used for the grid voltage monitoring. The design and performance of PLL directly affect the dynamics of the RES grid side converter (GSC). This paper presents the characteristics, design guidelines and features of advanced state-of-the-art PLL-based synchronization algorithms under normal, abnormal and harmonically-distorted grid conditions. Experimental tests on the selected PLL methods under different grid conditions are presented, followed by a comparative benchmarking and selection guide. Finally, corresponding PLL tuning procedures are discussed.

Keywords: Renewable energy sources (RES), grid side converters (GSC), synchronization, phase-locked loop (PLL), harmonic distortion, unbalanced grid conditions, power converter control, grid codes.

1. Introduction

Renewable energy sources (RES) require power electronic-based grid side converters (GSC) for efficient and reliable integration with the grid [1-5]. The increasing penetration of renewables [6] requires a continuous revision of the grid codes issued by local/national [7-11] and international authorities [12-16]. This is because GSC are continuously enhanced and diversified with new features and functionalities for supporting the grid and improving the power quality. Grid codes are therefore revised so that such systems support the grid when grid disturbances occur. Furthermore, they can be utilized in the future modeling of power systems, smart grids, and micro grids. Several recent grid regulations are given in Fig. 1, where the RES are required to remain grid-connected, injecting reactive power as long as the voltage level at the point of common coupling (PCC) is above the characteristic line for each case [17-21]. In addition, a RES must also have the Fault Ride Through (FRT) capability (i.e., remain connected under grid faults) even under zero grid voltage conditions for approximately 150 ms (i.e., in Germany [18] and Spain [21]), thereby improving the power system stability [22, 23]. Hence, for accurate response and for complying with modern grid regulations, the GSC control algorithms must perform accurately under normal and abnormal grid conditions and be equipped with advanced features and functionalities.

In general, the control of a GSC mainly consists of three modules: the active/reactive power regulation in the outer control loop, the inner current control loop and the synchronization module [24-27]. The power system topology and the corresponding controller diagram for such a three-phase GSC are extensively described in [28-31], and they are also presented in Fig. 2. The *PQ* controller is responsible for generating the current references, which are subsequently tracked by the current controller in order to inject the required active/reactive powers. The synchronization unit

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performs the function of extracting the grid information that is subsequently used in the control loops. Two main design methodologies are adopted for such control algorithms. One design methodology is implemented in the stationary $\alpha\beta$-reference frame with Proportional Resonant (PR) controllers [32] or other periodic controllers [33]. The other design methodology employs Proportional Integral (PI) controllers in the synchronous *dq*-reference frame (SFR) [34-36]. For both cases, the grid voltage information, that is, the phase angle and frequency, is required for the implementation. In general, a PLL is most commonly used to extract the phase angle of the grid voltage at the PCC and hence the frequency. Many PLL algorithms have been proposed and exist in the literature and they are the center of attention in this work. The performance of the PLL under normal and distorted grid conditions directly affects the dynamics of the *PQ* and current controllers. Therefore, the design of PLL systems is critical for the accurate operation of the grid-connected RES.

A review of various three-phase PLLs is presented in [37], however, many of the important state-of-the-art-PLLs such as, the dαβPLL, FPD dαβPLL, adaptive dαβPLL, MSHDC PLL, DNαβPLL, PMAFPLL, αβEPMAFPLL, EPMAFPLL Type 2, LPNPLL, FFTPLL, EPLL, modified PI based PLLs and the MRF PLL are not considered. The review study in [38] considers three-phase PLLs such as the dqPLL, the αβPLL, the DSRFPLL, the EPLL, the 3EPLL and the DSOGIPLL. Both review studies [37, 38] lack experimental benchmarking. The review studies in [39, 40] compare only three PLLs and do not consider many of the other important state-of-the-art PLLs, such as the ones discussed in this work. The work presented in [41, 42] considers four PLLs from the literature. The selected PLLs are dqPLL, modified dqPLL, DSOGIPLL and Multiple SOGI (MSOGI) PLL, neglecting many important ones. A recent review study [43], includes the dqPLL, the EPLL, the Quadrature PLL and the variable sampling rate PLL. However, the study does not provide experimental results comparison and in addition, several advanced PLLs are not considered.

This PLL review study is thorough from all aspects and considers the most important categories and the latest state-of-the-art PLLs that have not been considered in previous review studies. These include filtering based approaches, decoupling network based PLLs, modified loop filter PLLs and other important PLL approaches. Every PLL has been discussed in detail along with its operating principle, mathematical analysis and schematic diagram. In addition, their performance capabilities together with their advantages and disadvantages are provided. Another main contribution of this paper is the experimental benchmarking of the selected three-phase PLLs for the first time in the literature. The work summarizes the benchmarking of the PLLs in a tabular form (Table 7), obtained from experimental analysis. This can be used as a selection guide by engineers and new researchers who want to contribute to the area. Furthermore, it can help engineers to select the appropriate PLL algorithm according to specific application requirements and grid operating conditions. The benchmarking considers various aspects: such as performance accuracy of PLLs under normal and abnormal grid operating conditions, the dynamic response of the PLLs, the computational complexity and frequency/phase overshoot of the PLLs.

The paper is organized as follows: section 2 presents the basic and conventional types of PLLs. Advanced PLL algorithms considering unbalanced and distorted grid conditions are discussed in Section 3. Section 4 presents the experimental verification and comparative study for the selected PLLs, providing a selection guide for choosing the most appropriate PLL algorithm for specific application and under specific grid conditions. Finally, the tuning methods of the PLLs are presented, followed by the conclusion.

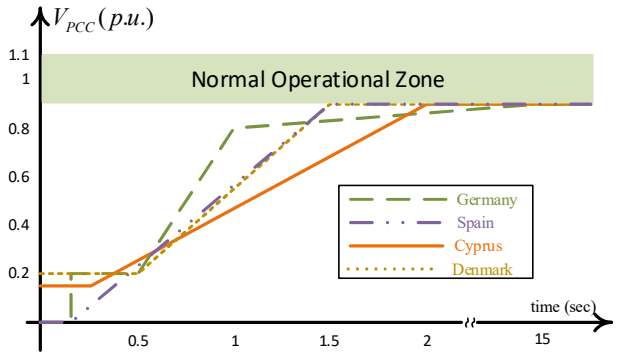

Fig. 1: Fault ride through (FRT) requirement for RES systems under grid faults [44, 45], where V_{PCC} is the voltage at the point of common coupling (PCC).

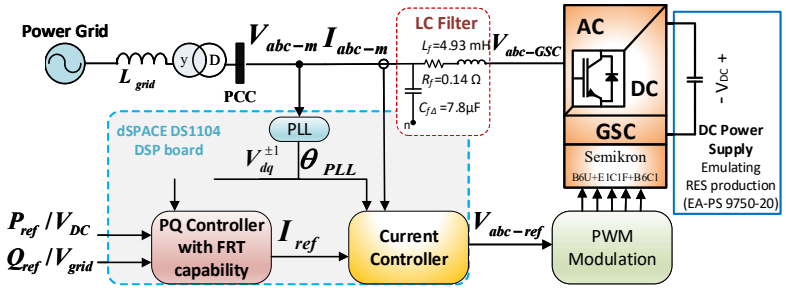

Fig. 2: General structure of a grid-connected renewable energy system.

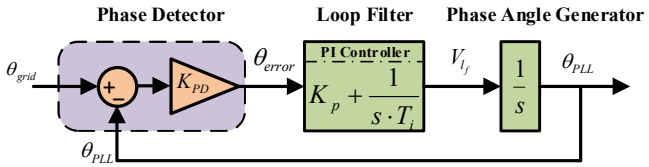

Fig. 3: Block diagram of the fundamental phase-locked loop (PLL) system.

2. Review of Conventional Three-Phase PLL Algorithms

The block diagram of the fundamental PLL consisting of a Phase Detector (PD), a Loop Filter (LF) and a frequency/phase generator (FPG), also called a Voltage-Controlled Oscillator (VCO), is presented in Fig. 3. The simplest PLL algorithms are the conventional dqPLL and the αβPLL.

2.1. The *dqPLL*

The dqPLL [46, 47] is designed according to the Clarke and Park transformation, shown in (1), which converts the natural abc reference frame into the synchronous dq-reference frame. To acquire the phase of the input voltages, the q-component of the positive sequence voltage in (3) tracks a zero reference through a PI controller, the loop filter in Fig. 3. As a result, under ideal voltage conditions, θ_{dqPLL} becomes equal to the phase angle of the three-phase voltage and component v_d perfectly tracks the magnitude of the positive sequence voltage $\mathbf{v}^+$. Since the synchronous frame is rotating with the positive angular speed, the dqPLL works accurately for balanced grid faults. It fails to track the phase angle when an unbalanced fault occurs. This is because of the presence of double-line frequency oscillations induced by the negative sequence components $\mathbf{v}^-$ that disturb the dq-components resulting in the mismatch of v_d from the positive sequence magnitude $|\mathbf{v}^+|$ [34]. In addition, the $dqPLL$ cannot work for harmonically distorted three-phase voltages. The structure of the dqPLL is presented in Fig. 4.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos(\theta_{PLL}) & cos(\theta_{PLL}-120) & cos(\theta_{PLL}+120) \\ -sin(\theta_{PLL}) & -sin(\theta_{PLL}-120) & sin(\theta_{PLL}+120) \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (1)$$

$$v_d = V_m \cos\left(\theta_{grid} - \theta_{dqPLL}\right) \quad (2)$$

$$v_q = V_m \sin\left(\theta_{grid} - \theta_{dqPLL}\right) \quad (3)$$

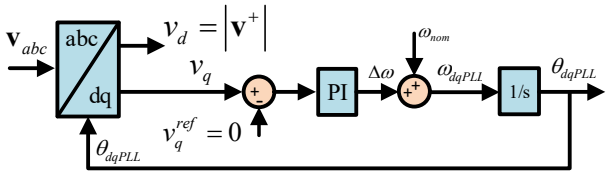

Fig. 4: Conventional $dqPLL$ system.

2.2. $\alpha\beta PLL$

The $\alpha\beta$PLL [48-50] achieves synchronization in the stationary $\alpha\beta$-reference frame that translates the natural abc reference frame into the stationary $\alpha\beta$-reference frame. The transformation can be done by setting $\theta_{PLL} = 0$ in (1). The phase angle $\theta_{\alpha\beta PLL}$ is estimated with the help of the trigonometric equations, as seen in (4), where θ_{grid} is the actual grid voltage phase angle. It is worth mentioning that (4) is valid only for small phase errors θ_{error}. The structure of the $\alpha\beta$PLL, shown in Fig. 5, is used to generate the phase error θ_{error}. Thus, controlling it to track a zero reference through a PI controller leads to the extraction of the phase. The $\alpha\beta$PLL is able to estimate the phase angle for balanced grid conditions. However, it also fails to accurately operate under unbalanced grid faults due to the presence of negative sequence voltage component similar to that of the dqPLL. The inaccuracies due to the unbalanced sequence can be compensated by reducing the bandwidth of the synchronization control loop. Unfortunately, this will result in slower dynamic response of the PLL [51, 52]. The only advantage of the $\alpha\beta$PLL in contrast to the dqPLL is that the frequency overshoot at the time of faults is smaller.

$$\theta_{error} = \theta_{grid} - \theta_{\alpha\beta PLL}$$

$$\Leftrightarrow \theta_{error} \approx sin(\theta_{grid})cos(\theta_{\alpha\beta PLL}) - sin(\theta_{\alpha\beta PLL})cos(\theta_{grid}) \quad (4)$$

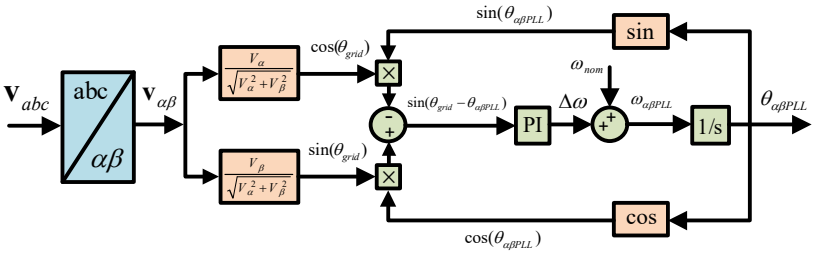

Fig. 5: Structure of the αβPLL system.

3. Review of Advanced Three-Phase PLL Algorithms

The control of the grid-connected RES is very important when disturbances occur on the grid as it may lead to unstable operation. According to recent grid regulations, the RES systems must function as such to support the grid under unbalanced and fault conditions [8, 12]. These abnormal grid conditions introduce undesired oscillations caused by the presence of other frequencies in the voltage vector (negative sequence and/or harmonics) and result in accuracy problems for synchronization techniques [53, 54]. Therefore, the synchronization techniques should be advanced in order to provide accurate angle information under these abnormal conditions with fast dynamics. Various proposals for improving the synchronization under unbalanced grid conditions exist in the literature. They can be divided into two categories. The first one is the Pre-Calculating or Pre-Filtering (PCPF) method and the second one is the Loop Filter Modification (LFM) method. The PCPF method employs a pre-filtering stage in the phase detector unit (PDU)

to compensate the effect of unbalanced grid voltage components. However, in the LFM method, the loop filter stage is modified/re-tuned according to the fault/disturbances in order to improve the dynamics.

3.1. Review of the PCPF-based Techniques

The undesired effects of unbalance and/or harmonics are compensated by the PCPF units before passing it through to the loop-filtering stage. A simple structure modifying the conventional dqPLL is proposed in [55], where two low-pass filters (LPF) are added to the closed-loop control path to compensate the unwanted double-line frequency oscillations. However, adding LPFs in the control path degrades the performance of the PLL. Nevertheless, some advanced PCPF-based techniques are discussed in this section mainly to address issues under unbalanced grid faults.

3.1.1. Decoupled Double Synchronous Reference Frame PLL ($dsrfPLL$)

The performance of the dqPLL and αβPLL is inaccurate under unbalanced grid conditions as discussed previously. This is overcome by the Decoupled Double Synchronous Reference Frame PLL (ddsrfPLL) [56] in which, the coupling effect between the positive and negative sequences of the voltage is decoupled accordingly. The ddsrfPLL is implemented by converting the grid voltage into both positive and negative synchronous reference frames, as shown in Fig. 6. Hence, two SRF frames are employed. One for the positive sequence dq^{+1} and one for the negative sequence dq^{-1} rotating with their corresponding angular speeds. The angular speed for the dq^{+1} SRF frame is $+\omega$ with the corresponding phase angle denoted by θ^{+}. The angular speed for the negative sequence dq^{-1}, is $-\omega$ with the corresponding phase angle represented by θ^{-}. Following the transformation, a decoupling network is used to cancel out the effect of positive and negative sequences from each other. Once the positive and negative sequences are effectively extracted and separated, the algorithm of $dqPLL$ is used to estimate the grid voltage phase angle. The transformed voltage vectors are shown in (5) and (6), consisting of dc and oscillation terms. To determine the positive ($\mathbf{v}^{+}$) and negative ($\mathbf{v}^{-}$) voltage sequences, two Decoupling Cells (DC) are employed, as shown in Fig. 7. The signals from the decoupling cells $\mathbf{v}_{dq}^{+1*}$ and $\mathbf{v}_{dq}^{-1*}$ are almost purely dc terms and can be used to calculate the magnitude of the grid voltage. This is achieved by passing them through an LPF with a cutoff frequency ω_c equal to $2\pi \cdot \left(\frac{50}{0.707}\right) rad/s$ in order to remove any remaining oscillations in the estimated voltage vectors [8, 12]. The q-component of the positive sequence, v_{q}^{+1*}, is then passed to the dqPLL phase extraction algorithm. Due to the decoupling, the ddsrfPLL ensures a satisfactory operation under unbalanced grid faults. Since the ddsrfPLL is using the dqPLL algorithm for the phase extraction, it presents high frequency and phase overshoot at the time of faults. In addition, inaccurate operation due to the presence of voltage harmonics is not considered.

$$\begin{aligned}\mathbf{v}_{dq}^{+1} &= \left[T_{dq}^{+1}\right].\mathbf{v}_{\alpha\beta} \\ &= \underbrace{V^{+}\begin{bmatrix}1\\0\end{bmatrix}}_{DC\ Term} + \underbrace{V^{-}\begin{bmatrix}\cos(-2\omega t)\\ \sin(-2\omega t)\end{bmatrix}}_{Oscillation}\end{aligned} \qquad (5)$$

$$\begin{aligned}\mathbf{v}_{dq}^{-1} &= \left[T_{dq}^{-1}\right].\mathbf{v}_{\alpha\beta} \\ &= \underbrace{V^{-}\begin{bmatrix}1\\0\end{bmatrix}}_{DC\ Term} + \underbrace{V^{+}\begin{bmatrix}\cos(2\omega t)\\ \sin(2\omega t)\end{bmatrix}}_{Oscillation}\end{aligned} \qquad (6)$$

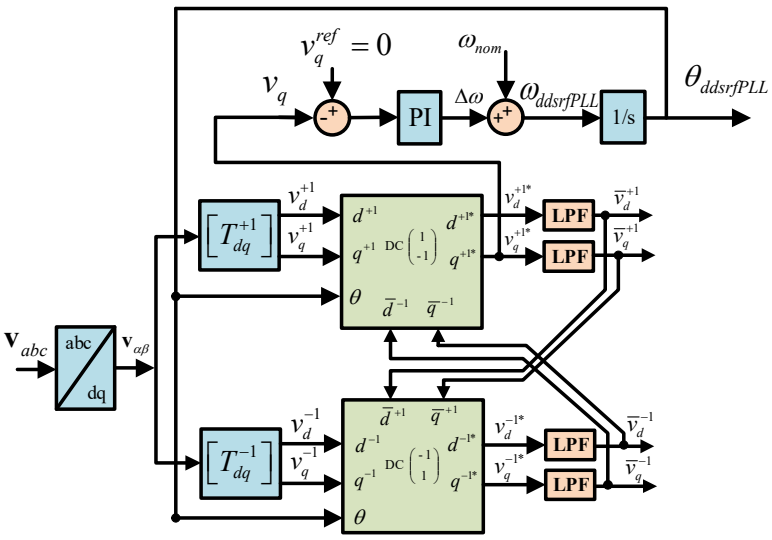

Fig. 6: Block diagram of the decoupled double synchronous reference frame PLL ($ddsrfPLL$).

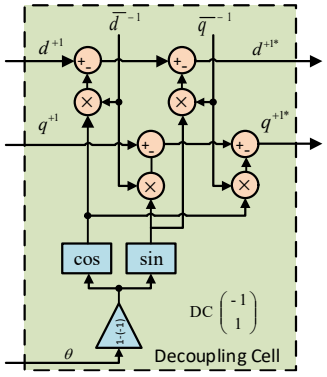

Fig. 7: Structure of a single decoupling cell used in the $ddsrfPLL$ system shown in Fig. 6.

3.1.2. Hybrid $d\alpha\beta PLL$

According to [48-50], the $\alpha\beta$PLL experiences less overshoots under grid faults compared to the dqPLL and the ddsrfPLL. However, the performance of the $\alpha\beta$PLL is affected when an unbalanced fault occurs. On the other hand, ddsrfPLL can operate unaffected under similar grid conditions. This gave way for the development of a new hybrid d$\alpha\beta$PLL [57]-[58] which combines the features of the $\alpha\beta$PLL (small overshoots) and those of the ddsrfPLL under unbalanced faults. The structure of the hybrid d$\alpha\beta$PLL is shown in Fig. 8. The hybrid PLL has an enhanced performance under balanced and unbalanced faults in terms of low overshoots, high accuracy and fast dynamics compared to the ddsrfPLL. The frequency limits provided by grid regulations are therefore not violated with the hybrid d$\alpha\beta$PLL. In [57], a simulation analysis has been performed to show that a lower overshoot can be achieved by the d$\alpha\beta$PLL (compared to the ddsrfPLL) if the tuning parameters are selected to achieve an identical settling time. Similarly, faster dynamics can be achieved by the d$\alpha\beta$PLL, if the tuning is re-adjusted for an identical frequency overshoot with the ddsrfPLL. Like the ddsrfPLL, the accuracy of the d$\alpha\beta$PLL is degraded under grid voltage harmonics.

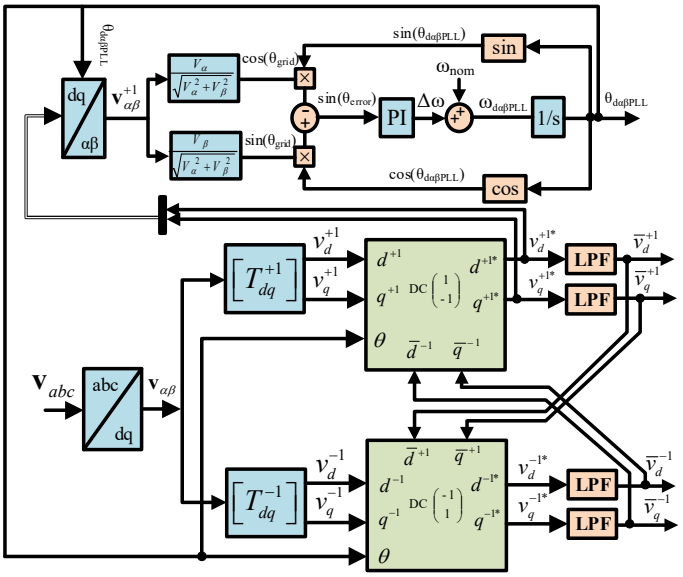

Fig. 8: Structure of the hybrid $d\alpha\beta PLL$ by combining the $dqPLL$ and the $ddsrfPLL$.

3.1.3. Dual Second-Order Generalized Integrator (DSOGI) PLL

The DSOGI-PLL (equivalent to the ddsrfPLL [34]) is designed in the $\alpha\beta$-frame based on the instantaneous symmetrical component (ISC) method [55, 59]. The implementation of the DSOGI-PLL requires the transformed voltage vectors in the $\alpha\beta$ stationary frame, that is, the actual $\mathbf{v}_{\alpha\beta}$ components and the corresponding in-quadrature components $q\mathbf{v'}_{\alpha\beta}$. The transformation is achieved by two second-order generalized integrators (SOGI) based on a Quadrature Generation (QG), which acts as an adaptive band pass filter as shown in Fig. 9. The SOGI-QG has two output vectors, the voltage vector $\mathbf{v'}_{\alpha\beta}$, representing the filtered voltage vector, and the corresponding in-quadrature filtered voltage vector $q\mathbf{v'}_{\alpha\beta}$. Utilizing the output of the SOGI-QG, the positive sequence voltage is calculated using Positive Sequence Calculator (PSC) computations, as illustrated in Fig. 10. When the positive sequence voltage vector is obtained, the q-component is forced to zero. In order to adapt the center frequency of the DSOGI, the estimated frequency is fed back to the SOGI-QG block. The DSOGI-PLL performs an accurate phase angle estimation under unbalanced fault conditions, but results in slow dynamics and large frequency-overshoots, as discussed in [60].

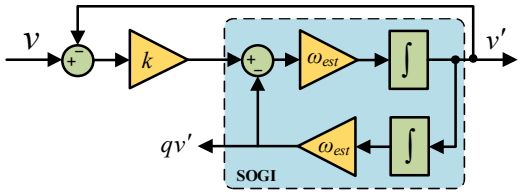

Fig. 9: Second order generalized integrators (SOGI) block diagram.

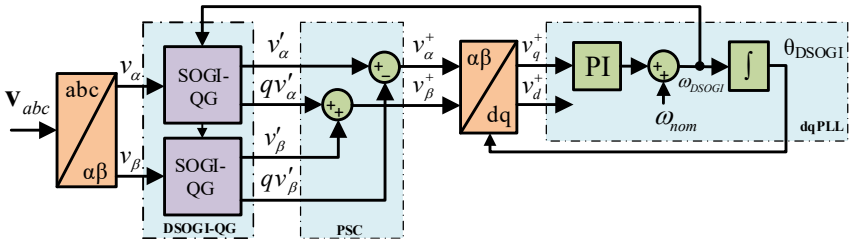

Fig. 10: Block diagram of the quadrature generation (QG) based dual second-order generalized integrator PLL (DSOGI-PLL).

3.1.4. Proportional Integral Derivative (PID)-based PLL

The large frequency overshoots that appear in the $ddsrfPLL$ can be reduced by introducing a Proportional Derivative Integral (PID) controller, instead of the conventional PI, in the loop filtering stage [61]. The extra derivative parameter can efficiently reduce the overshoot in the estimated frequency [62]. However, the low pass filtering characteristics of the PLL are affected due to the presence of extra zeros in the transfer function. Thus, the employment of the PID controller will constitute the PLL less responsive under inaccuracies caused by the higher order harmonics. Therefore, the application of the PID controller is generally avoided for cases where it is necessary to compensate the undesired effect of high-frequency grid voltage harmonics.

3.1.5. Adaptive or Notch Filtering Techniques

The undesired oscillations caused by abnormal and faulty grid conditions can be mitigated using adaptive or notch filters in the PLL algorithm [63-67]. Based on the Schur lattice structure in [64], adaptive notch filters with infinite impulse responses are implemented to improve the performance of the conventional SRF $dqPLL$ under variable frequency and unbalanced grid voltage conditions. The technique in [64] can achieve effective synchronization under unbalanced and harmonic-distorted grid voltages, irrespective of any abrupt variations in the grid frequency. A similar method is proposed in [63], where the conventional SRF $dqPLL$ is modified using a low-pass notch filter (LPN), as shown in Fig. 11. The LPN-PLL is an alternative of the Fast Fourier Transform (FFT) based PLL [68, 69] with improved performance and enables an accurate response under harmonics and grid voltage unbalance. In contrast to the SRF $dqPLL$, the FFT-PLL and LPN-PLL are implemented without PI controllers. The dynamic response is therefore not affected by the tuning of PI controller and they are less complicated and complex. However, the use of adaptive filtering in the estimation path of the PLL causes undesirable slow dynamics and consequently affects the overall performance of grid-connected RES systems.

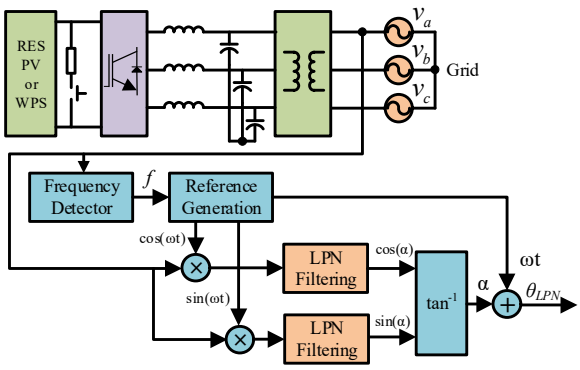

Fig. 11: Phase extraction block diagram of the low-pass filter based (LPN-PLL).

3.1.6. Three-Phase Enhanced PLL (3EPLL)

The three-phase enhanced PLL (3EPLL) proposed in [70] is a three-phase version of the EPLL [71-74] and is developed by utilizing four individual EPLL blocks. The EPLL is actually an adaptive band pass filter that is capable of adjusting the transfer function according to the error signal, as depicted in Fig. 12. In the 3EPLL, each voltage phase is processed by an independent EPLL module, and subsequently, two sinusoidal signals are generated. The two signals are equal in magnitude and frequency but are 90° shifted from each other, the second signal is led by 90°. The output signals from the three EPLLs are then transferred to the Instantaneous Symmetrical Components (ISC) computational block for acquiring the positive voltage sequence, $\mathbf{v}_{abc}^{+}$. The positive voltage sequence is subsequently transferred to the fourth EPLL to extract the phase angle and magnitude of the fundamental component. The structure of the 3EPLL is shown in Fig. 13. A comparison of the 3EPLL with other existing PLL techniques is presented in [60]. It is shown that the 3EPLL performs accurately under unbalanced grid scenarios but has slow dynamics among the benchmarked.

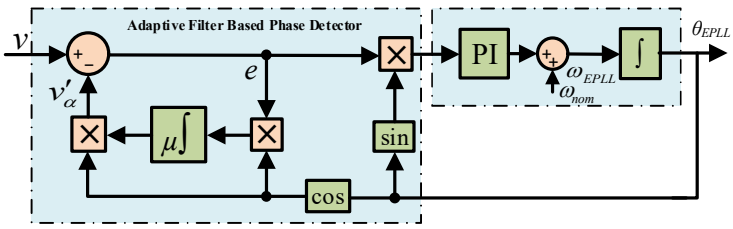

Fig. 12: Adaptive filter based phase detector for a single-phase PLL (i.e., the EPLL).

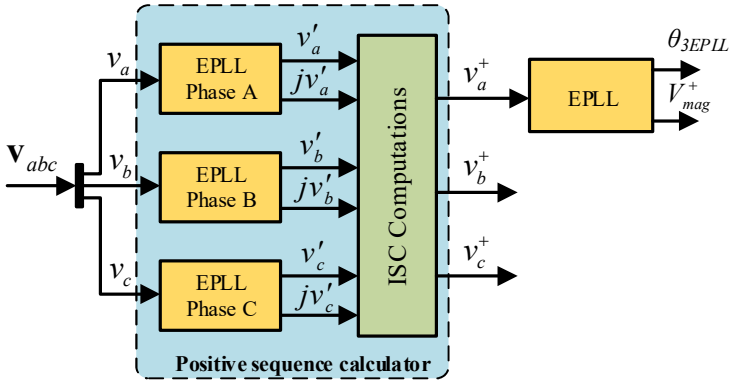

Fig. 13: Three phase enhanced PLL system (3EPLL) consisting of four EPLLs (see Fig. 12) and an instantaneous symmetrical component ISC computation unit.

3.2. Review of PLL Techniques by Modifying the Loop Filter

The PCPF enables the accurate synchronization under asymmetric grid conditions. However, the PCPF-based methods present slow dynamics. By modifying the loop filter (i.e., Loop Filter Modification (LFM) methods), the performance and dynamics under unbalanced faults can be improved. The objectives of the LFM-based techniques are the dynamic cancellation of negative sequence and/or undesired frequency components, a faster response, and a lower overshoot in the estimated frequency/phase. It is worth mentioning that the dynamics of the LFM-based PLL are inversely related to the overshoots in the frequency/phase estimation [56],[75]. Therefore, the response must be improved without violating the frequency limits imposed by grid regulations. This section discusses some LFM-based techniques for further improving the dynamics.

3.2.1. Modified PI Controller

The LFM methods modify the loop filtering stage to improve the performance under distorted and unbalanced grid conditions. In [52, 74, 76, 77] for example, the conventional PI controller is used in the loop filtering stage with an improved adaptive tuning process which adjusts the controller parameters adaptively. Thus, the performance of the PLL is improved. An intelligent method with an elegant adaptive tuning mechanism is proposed in [74], where the integral gain is adaptively adjusted and it is applied to single-phase and three-phase conventional dqPLLs [46, 47]. The method proves to be promising in mitigating the effect of undesired frequency variations under large abrupt disturbances and also enables smooth start-up. To accelerate the performance of the PLL and to reduce the ripples of the estimated frequency, a novel frequency feedback process is introduced in [76]. The feedback term is added to avoid the unnecessary delays caused by the low pass filter. In addition, it is also used to eliminate the second-order harmonic that occurs under the phase-locked condition. However, this method results in increased phase/frequency overshoots. A versatile method is presented in [52] to compensate the effect of harmonic distortions and unbalanced grid faults. The method enables the variable tuning of the PI controller for a slow or fast dynamic response by selecting appropriate PI parameters from a set of two calculated values. The slow-tuned PLL enables the accurate mitigation of harmonics but with slow dynamics. In contrast, a fast-tuned PLL allows the compensation of unbalanced faults with fast dynamics. Furthermore, the transient response of the PLL is improved by using a non-linear PI controller in

the filtering stage [77]. The tuning parameters for the nonlinear PI are updated in accordance with the error in the phase estimation. For all the controllers, the adaptive tuning mechanism can improve the dynamics of the PLL depending on the robustness of the employed adaptive mechanism.

3.2.2. Frequency Phase Decoupling (FPD) d$\alpha\beta$PLL

In [74], the conventional dqPLL algorithm is modified with a feature that decouples the frequency and phase angle estimation loops improving in this way the dynamic response of the PLL. The modification is referred to as Frequency Phase Decoupling (FPD) and is done to avoid the unwanted frequency swings that occur due to variations in the voltage and/or phase angle. In addition, an adaptive tuning mechanism is used to adjust the coefficient of the integral term in order to reduce the effect of disturbances on the frequency overshoot. The tuning mechanism cannot improve the dynamics of the PLL, as indicated by the PLL transfer function in [74]. Instead, it controls the frequency overshoot by adjusting the damping coefficient. Therefore, the response improvement obtained in [74] is mainly due to the FPD. However, the frequency overshoot reduction can also be addressed as time response improvement, since the PLL can be easily tuned for fast dynamics without the risk of large frequency overshoots. Considering the aforementioned advantages, the FPD algorithm in [74] is applied to the d$\alpha\beta$PLL and the new PLL is referred to as the FPD d$\alpha\beta$PLL, Fig. 14 [78]-[79]. The frequency estimation for the conventional and the FPD-based d$\alpha\beta$PLL systems is given in (7) and (8), respectively. As mentioned previously, the FPD performs the decoupling of phase and frequency loops, and this is done without considering the term $(\theta_{error}.k_p)$ in frequency estimation loop, as shown in Fig. 14. In addition, a tuning mechanism similar to that in [74] is used to update the time constant T_i by scaling it with a factor based on the phase error θ_{error} and the positive sequence $\mathbf{v}_{dq}^{*+1}$, as presented in (9). The term λ is set between 50 and 100.

$$f_{est(\mathrm{d}\alpha\beta\mathrm{PL}\ )} = \frac{1}{2\pi}\left[\theta_{error}\left(k_p + \frac{1}{T_i s}\right) + \omega_{norm}\right] \quad (7)$$

$$f_{est(FPD\mathrm{d}\alpha\beta\mathrm{PLL})} = \frac{1}{2\pi}\left[\theta_{error} \cdot \frac{1}{T_i s} + \omega_{norm}\right] \quad (8)$$

$$\left(1 + \lambda \frac{\theta_{error}}{\sqrt{v_d^{*+1} + v_q^{*+1}}}\right) \quad (9)$$

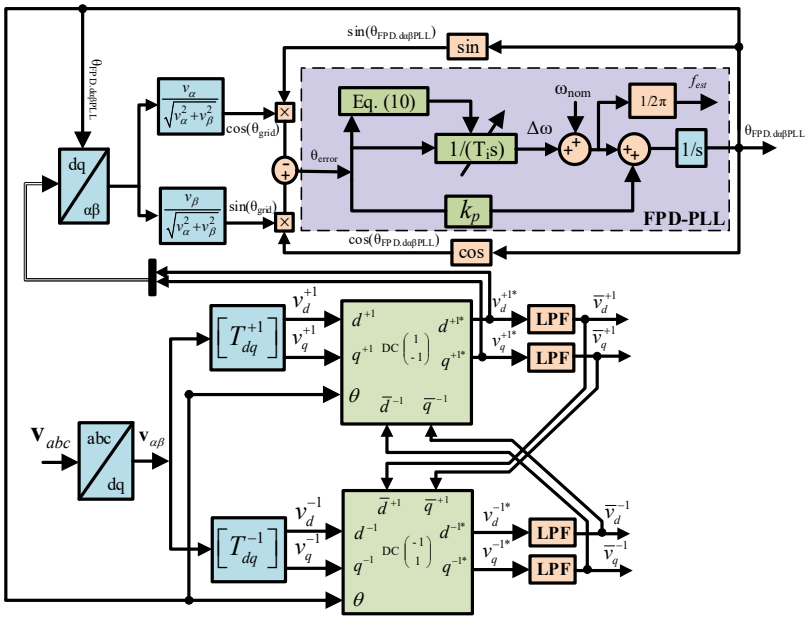

Fig. 14: Block diagram of frequency phase decoupling (FPD) based dαβPLL.

3.2.3. Adaptive Frequency Phase Decoupling (FPD) based dαβPLL

The frequency overshoot is related to the tuning of the PLL (i.e., the time response of the PLL) and the fault type, as discussed in [78, 79]. Consequently, an LFM based adaptive FPD d$\alpha\beta$PLL is proposed in [78]-[79] to improve the dynamics of FPD d$\alpha\beta$PLL under balanced/unbalanced grid faults. The structure of the adaptive FPD d$\alpha\beta$PLL is similar to that of the FPD d$\alpha\beta$PLL shown in Fig. 14 except for the tuning parameters of the PI controller. Unlike the FPD d$\alpha\beta$PLL, the tuning parameters of the adaptive FPD d$\alpha\beta$PLL are adaptive and varies according to the defined adaptation rules. This is enabled by means of a lookup table that is pre-calculated according to the characteristics and type of the grid faults and estimated through a Fault Classification Unit (FCU) in real time environment. The FCU detects for example the voltage dip level d and the fault type (A-G, according to [34],[80]) using space vector analysis [81-84], as shown in Fig. 15. The information from the FCU is subsequently used to improve the dynamics but within the assigned limits of frequency according to the applied grid code requirement (e.g., a frequency window of -2.5 Hz to +1.5 Hz around 50 Hz according to the German grid code [7]-[11]). The inputs required for the operation of FCU are the phase angles and magnitudes of the grid voltage positive and negative sequences, that are, $\theta_p, \theta_n, |\mathbf{v}^+|$ and $|\mathbf{v}^-|$. They are obtained in real time using the adaptive d$\alpha\beta$PLL instead of the FFT in order to ensure a fast online estimation. Based on the space vector analysis in [82], the complex plane representation of the grid voltage results in an ellipse with an inclination angle, a major axis, a shape index (SI) and a minor axis as shown below in (10).

$$r_{maj} = |\mathbf{v}^+| + |\mathbf{v}^-| \ , \quad r_{min} = \big||\mathbf{v}^+| + |\mathbf{v}^-|\big|$$

$$\theta_{incl} = \tfrac{1}{2}\big(\theta_p + \theta_n\big) , \quad SI = \tfrac{r_{min}}{r_{max}} \qquad (10)$$

The grid voltage parameters in (10) are used to characterize the fault type and to calculate the dip level (d) [81-84]. Information about the fault type and dip level is used to tune the PI controller adaptively for fast dynamics. The PI controller parameters are pre-calculated based on simulation analysis for different fault types and dip levels as discussed in [34] [57] [85]-[86]. The adaptive FPD d$\alpha\beta$PLL suggests that the tuning parameters of the PLL should be adaptively adjusted in accordance to the fault type for achieving faster synchronization. Since the dynamic improvement due to the FPD and the tuning mechanism are independent, the overall performance of the adaptive FPD d$\alpha\beta$PLL is better than the corresponding individual performance. One drawback of the adaptive FPD d$\alpha\beta$PLL is that the effect of harmonic distortion is not considered. The structure of the adaptive FPD d$\alpha\beta$PLL is given in Fig. 16.

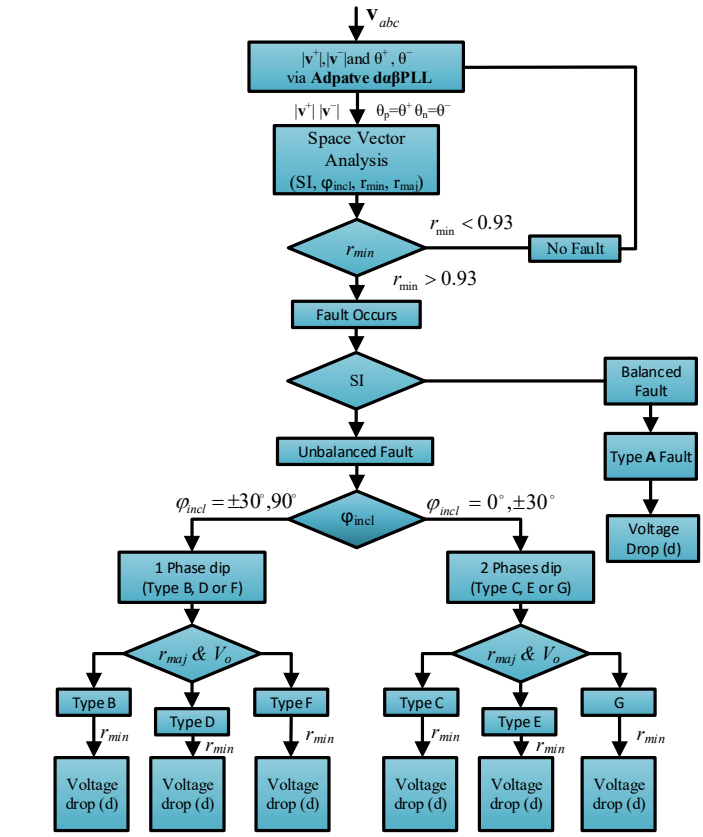

Fig. 15: Algorithm of the fault classification unit followed by a space vector analysis.

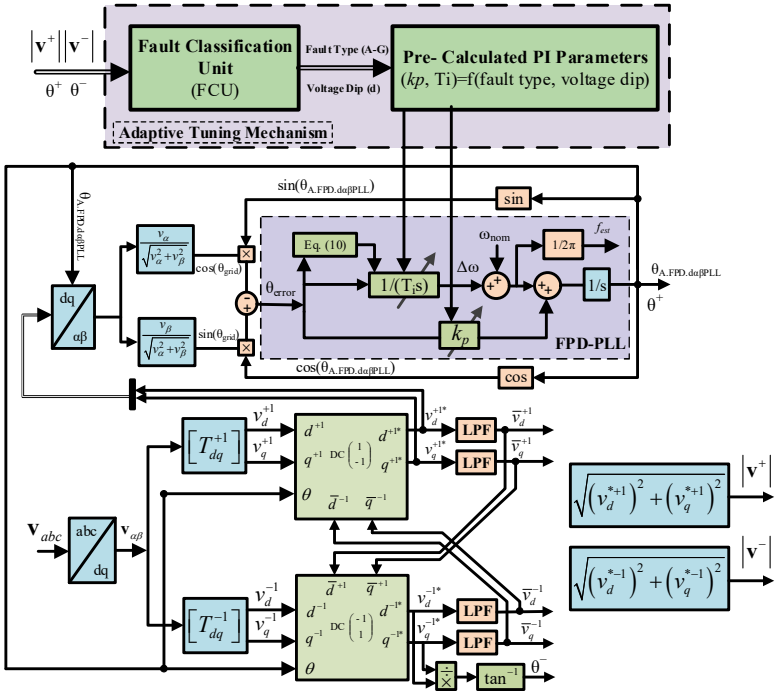

Fig. 16: Block diagram of the adaptive frequency phase decoupling based dαβPLL.

3.3. Review of Harmonic-Immune PCPF Techniques

All the PLLs discussed so far do not explicitly consider the effect of harmonic distortion in the grid voltage. In this section, those PCPF based PLL techniques that consider the effect of grid voltage harmonic distortion are discussed.

3.3.1. Moving Average Filter (MAF)-based Conventional PLL

Moving Average Filter (MAF) based techniques are presented in [87-90] to compensate the effect of harmonics and unbalanced faults. The transfer function of a MAF filter in the z-domain is given in (11) and its discrete implementation is shown in Fig. 17 [88, 91-93].

$$H_{MAF}(z) = \frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}} \qquad (11)$$

The simplest structure for the MAF-based $dqPLL$ and that of the MRFPLL (representing a modified ddsrfPLL) are shown in Fig. 18 and Fig. 19, respectively. The LPF of the ddsrfPLL is replaced by a MAF to mitigate harmonics. Although the MAF provides a good performance in terms of harmonic immunity, the discretized implementation of MAF-based PLL techniques results in an inaccurate estimation when a small variation occurs in the grid frequency. By adjusting the number of samples in accordance to the varying frequency the errors can be minimized but they cannot be removed completely [88]. A possible way is to adapt the MAF window length by operating the PLL under a variable sampling rate [94]-[95]. However, making the sampling rate variable restricts the proper operation and design of the GSC controller and in certain cases it challenges the stability. In [92], a lead compensator is employed to reduce the amount of the phase delay but it is not fully mitigated. Even if the inaccuracies are minimized, MAF-based PLLs have comparatively slow dynamics. A variable sample-rate-based PLL is proposed in [60] with good dynamic responses and with high immunity against harmonics. However, operating the GSC controller under a variable sampling rate may not be always possible. Hence, there is a need for synchronization algorithms that can work under harmonics and balanced/unbalanced faults without compromising the overall performance and dynamic response of the PLL.

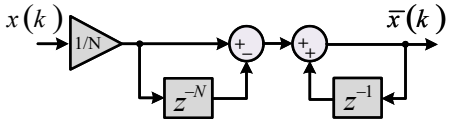

Fig. 17: Discrete implementation of a moving average filter (MAF).

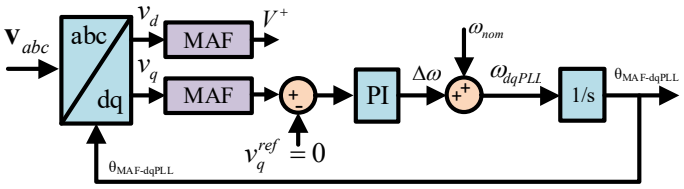

Fig. 18: Conventional $dqPLL$ enhanced by moving average filter (MAF).

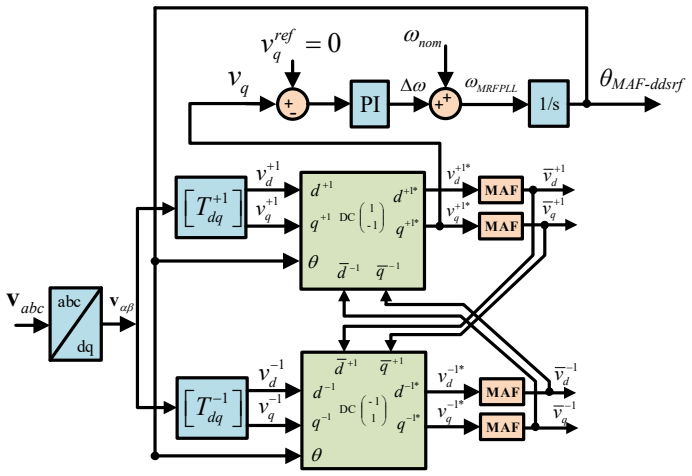

Fig. 19: Block diagram of a modified $ddsrfPLL$ with moving average filters (MRFPLL).

3.3.2. Pre-filtering Moving Average Filter (PMAFPLL)

The Pre-filtering Moving Average Filter (PMAF) PLL [93] overcomes the issue of slow dynamics and allows easy tuning by introducing a pre-filtering stage. The MAF is moved in the pre-filtering stage and the phase detector part contains only the dqPLL. This shifting makes the dynamic response of the PLL faster. The PMAFPLL transfer function is a second-order equation and is easily tuned based on the known parameters such as the settling time and the damping ratio. The structure of the PMAFPLL is shown in Fig. 20. The grid voltage containing the fundamental component and harmonics rotates with a nominal angle and when passed through the MAF, certain harmonics are removed. The filtered signals $\bar{\mathbf{v}}_{dq}$ are then transferred to a conventional dqPLL so that the phase angle is extracted. The offset error in the estimated phase under a non-nominal grid frequency is not considered.

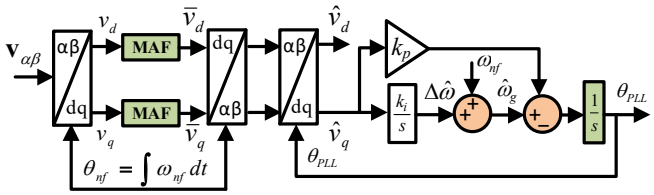

Fig. 20: Schematic diagram of the pre-filtering MAF PLL (PMAFPLL).

3.3.3. Enhanced PMAFPLL (EPMAFPLL)

The offset error under non-nominal grid frequencies is mitigated in an Enhanced PMAFPLL (EPMAFPLL) [93] by introducing a very effective and simple modification to the phase detector part of the PMAFPLL, as shown in Fig. 21. The offset error in the MAF PLL is calculated using mathematical relationships and adjusted by manipulating the rotational angle of the phase detector of the $dqPLL$. The amount of the phase error [93] is given by the phase of the MAF transfer function $\angle H_{MAF}$ as:

$$\angle H_{MAF}\left(z = e^{j\Delta\omega T_{sp}}\right) = -\Delta\omega \underbrace{\left(T_\omega - T_{sp}\right)/2}_{k_\varphi} \quad (12)$$

where, $\Delta\omega = \omega_g - \omega_{nf}$ is the deviation from nominal grid frequency, ω_{nf} and ω_g are the nominal and actual grid frequencies respectively, T_{sp} denotes the sampling period and $T_\omega = NT_{sp}$ represents the MAF window length.

Consequently, the phase error in (12) is added to the output of the PMAFPLL phase detector and the dq-transformation is carried out using the new angle in order to compensate the error, as shown in Fig. 21. The EPMAFPLL performs accurately for phase/frequency variations and harmonic distortions with fast dynamics. However, the EPMAFPLL

presents a poor performance under symmetrical and asymmetrical grid voltage faults since it suffers from high frequency/phase overshoots. Furthermore, when the EPMAFPLL is used to extract the phase angle from a harmonically distorted grid voltage under non-nominal grid frequencies, the estimated phase angle will contain oscillations. Hence, the EPMAFPLL results in an inaccurate estimation under harmonic-distorted grid voltages (for non-nominal frequencies only).

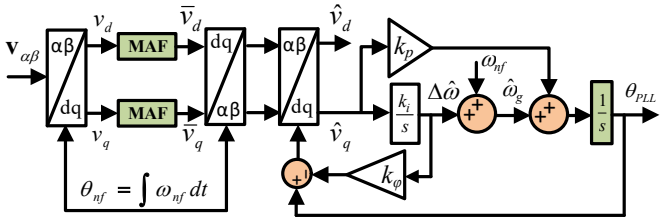

Fig. 21: Block diagram of the enhanced PMAFPLL (EPMAFPLL).

3.3.4. Space Vector Fourier Transform (SVFT) PLL

The Space Vector Fourier Transform (SVFT) synchronization system is a well-known three-phase PLL [96, 97]. The pre-filtering stage of the SVFT PLL is equivalent to that of the PMAFPLL, and hence, the PLLs are similar in terms of performances and mathematical transfer functions. The only difference is that unlike the PMAFPLL (where the MAF is used), the grid voltage fundamental component is extracted with the SVFT in the pre-filtering stage, as shown in Fig. 22. The SVFT is a Discrete Fourier Transform (DFT) applied to complex signals. The z-domain transfer function of the SVFT is shown in (13). As the performance of the SVFT is similar to that of the PMAFPLL, it also does not operate accurately under non-nominal grid frequencies. Consequently, a method similar to that for the EPMAFPLL can be employed to enhance the performance of the SVFT under non-nominal grid frequencies. The SVFTPLL and PMAFPLL are faster than the conventional MAF PLL, but slower compared to the $ddsrfPLL$.

$$G_{SVFTPLL}(z) = \frac{1}{N}\sum_{m=0}^{N-1} e^{j\frac{2\pi m}{N}} z^{-m} \qquad (13)$$

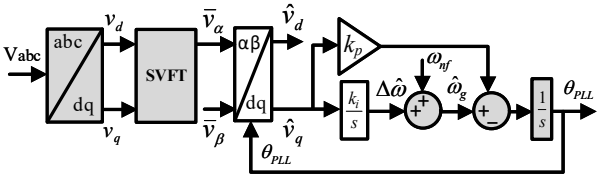

Fig. 22: Block diagram of the space vector Fourier transform (SVFT) based PLL.

3.3.5. Enhanced PMAFPLL (EPMAFPLL) Type 2

The high frequency and phase overshoots under grid faults and the inaccurate phase estimation under a harmonic-distorted grid voltage with non-nominal frequencies are overcome in [98] by modifying the structure of the conventional EPMAFPLL. The resultant modified PLL is referred to as the EPMAFPLL Type 2. The performance of the original EPMAFPLL in [93] is not analyzed under grid faults. However, it is observed that the reason for high overshoots is the presence of $\Delta\omega$ in the compensation term, which goes high under grid faults. Consequently, the high value of $\Delta\omega$ propagates to the resultant frequency/phase estimation because the compensation factor lies in the phase detector part of the EPMAFPLL.

The EPMAFPLL Type 2 eliminates the compensation term in (12) from the phase detector and incorporates it into the pre-filtering stage, as shown in Fig. 23. The modified pre-filtering stage of the EPMAFPLL Type 2 involves two rotating speeds for the input and output of the MAF. The speed at which the output of the MAF is translated back to the $\alpha\beta$-domain is added with the compensation factor. This is mainly because the MAF is responsible for this offset error induced by non-nominal grid frequencies. As a consequence of the compensation, the effect of the increased

frequency error $\Delta\omega$ under grid faults on the phase estimation is decoupled in the Type 2 EPMAFPLL. The result is less frequency overshoots and accurate harmonic mitigation under non-nominal grid frequencies. The improved harmonic attenuation comes from the fact that the reverse transformation is carried out considering the non-nominal error. The voltage translated to the dq frame (i.e., the first $\alpha\beta \rightarrow dq$ transformation) with a nominal frequency is shifted in phase when it is passed through the MAF. Therefore, the reverse transformation will impose the same shift, leading to an effective mitigation of the harmonics due to a non-nominal frequency.

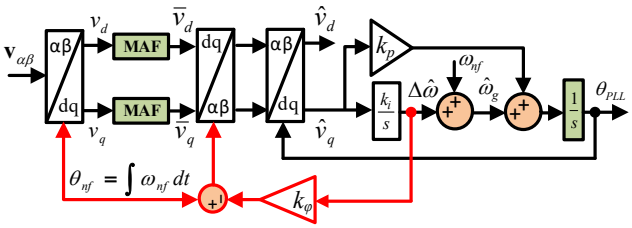

Fig. 23: Block diagram of the enhanced PMAFPLL (EPMAFPLL) Type 2.

3.3.6. αβ-enhanced PMAF (αβEPMAFPLL)

An αβ-enhanced PMAFPLL (αβEPMAFPLL) proposed in [99] aimed in minimizing the frequency overshoot of existing EPMAFPLL [93] in the event of faults. The high frequency overshoot of the EPMAFPLL is due to the dqPLL in the phase detector of the PLL. However, the αβEPMAFPLL is developed by incorporating the αβPLL to the phase detector. For mitigating the phase offset error due to the MAF in case of non-nominal frequency, the conventional αβPLL is modified by adding the phase error mentioned in (12) to the output angle of the αβPLL, as shown in Fig. 24. Consequently, the compensation added angle is fed back for the phase-error $\Delta\theta$ calculations. For the same dynamic response, the frequency overshoot of the αβEPMAFPLL PLL is lower, implying that it can be tuned for even faster response while maintaining the frequency limits. When compared to the EPMAFPLL, the αβEPMAFPLL has enhanced performance under balanced and unbalanced faults in terms of low overshoot and fast dynamics. Consequently, if the αβEPMAFPLL is employed, the frequency limits assigned by grid regulation authorities are not violated. It is worth mentioning that unlike other MAFPLLs, the αβEPMAFPLL is able to compensate any harmonic-order present in the grid with lower computational complexity.

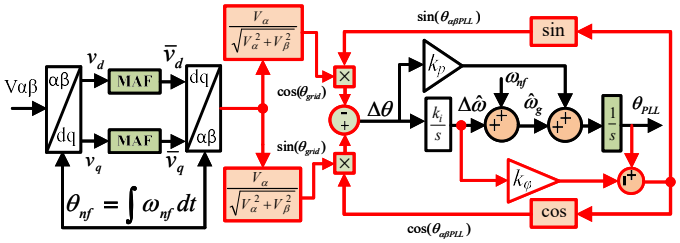

Fig. 24: Block diagram of the enhanced αβ PMAFPLL (αβEPMAFPLL).

3.3.7. Quasi Type 1 PLL

The Quasi Type 1 (QT1) PLL [100] is an extended system of the simple Type 1 PLL [101]. One main feature of the Type 1 PLL, as shown in Fig. 25, is that it accurately tracks step changes in the phase angle but its performance degrades when there is a step change in the frequency [50, 89, 102]. The performance of the Type 1 PLL for phase and frequency changes can be analyzed from (14) and (15) respectively [100], where V_i is the amplitude of the input voltage. According to (15), the tracking error under frequency variations can be mitigated by selecting a large LF gain, i.e., a high K_p. However, the solution is impractical under unbalanced and distorted grid scenarios because the higher the value of K_p, the higher the PLL bandwidth. Consequently, the capability of the PLL to filter noise and negative sequence oscillations becomes poor.

$$K_p V_i \sin(\theta_{error}) = 0 \Longrightarrow \theta_{error} = 0 \qquad (14)$$

$$K_p V_i \sin(\theta_{error}) = \Delta\omega \implies \theta_{error} = \sin^{-1}\left(\frac{\Delta\omega}{K_p V_i}\right) \qquad (15)$$

The QT1 PLL overcomes this problem by modifying the structure of the Type 1 PLL. The block diagram of the QT1 PLL is shown in Fig. 26. Since the MAF is an ideal LPF under certain defined conditions [88], the MAF in QT1 is used as an LPF for a better noise filtering performance. The input voltage amplitude dependency of the Type 1 PLL is removed by normalizing the q-component of the input voltage with the filtered amplitude estimation of the d-component (which corresponds to the input voltage amplitude V_i) [103]. The elimination of the input voltage amplitude dependency makes the PLL more robust against input voltage variations. The nonlinear behavior given by (15) is eliminated by including an arctangent function in the loop. This modification results in a linear relationship between the phase error and frequency change $\Delta\omega$, as given by (16). Consequently, the phase error θ_{error} under frequency variations $\Delta\omega$ is calculated and added to the output angle of the PLL. The term 'quasi' is used because it is similar to the Type 1 PLL but in terms of control systems, it refers to as a Type 2 system. The tuning process of the QT1 is very simple and it is only involved for selecting one parameter K_p in respect to the window length of the MAF. In the design phase, the required settling time under phase jumps should be considered.

$$\theta_{error} = \frac{\Delta\omega}{K_p V_i} \qquad (16)$$

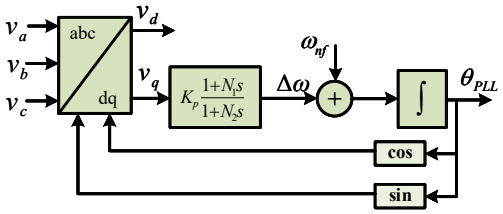

Fig. 25: Block diagram of the Type 1 PLL ($N_1 = 0$ means the lag filter, $N_1 = N_2 = 0$ is the simple gain).

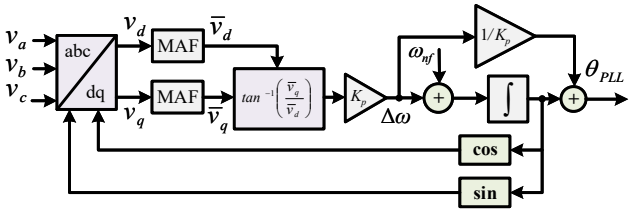

Fig. 26: Block diagram of the Quasi Type 1 (QT1) PLL.

3.3.8. Multi-Sequence /Harmonic Decoupling Cell PLL (MSHDCPLL)

A novel PLL referred to as Multi-Sequence/Harmonic Decoupling Cell (MSHDC) PLL is proposed in [53]. It can perform accurately under balanced/unbalanced grid faults and also harmonic-distorted grid voltages. Since the MSHDCPLL can work for normal and abnormal grid conditions, it can be used for fast and accurate synchronization of the grid-connected RES. The MSHDCPLL is developed using an advanced decoupling network proposed in [56] and [57]. The new decoupling network not only ensures the separation of positive and negative sequences but also performs the decoupling of harmonic components. This results in an oscillation-free positive sequence voltage $\mathbf{V}_{dq}^{*+1}$. Under abnormal grid conditions, the grid voltage consists of more than one voltage vector rotating with different synchronous speeds, that is, $\mathbf{v}_g = \mathbf{v}^{+1} + \mathbf{v}^{-1} + \mathbf{v}^{n}$. The voltage vector under unbalanced and harmonic-distorted grid conditions in each rotating reference is given by (17), where $\mathbf{v}_{dq}^{(n)}$ represents the transformed voltage vector in n^{th} synchronous reference frame (SRF^n) with n being the harmonic order and $\mathbf{V}_{dq}^{(n)}$ representing the DC term in the transformed $\mathbf{v}_{dq}^{(n)}$ voltage vector. The rotating reference frame representation of the grid voltage is used to separate each voltage vector (harmonics and negative sequence), as each component has its own rotating speed. Considering a harmonic-distorted (+5th and -5th) unbalanced grid voltage, an estimation of the voltage vectors is given in (18). The decoupled vectors in (18) lead to the development of a decoupling network as shown in Fig. 27. Once the vectors are

decoupled, the estimated positive sequence $\mathbf{V}_{dq}^{*+1}$ of the voltage is transferred to the phase detection of the $\alpha\beta$PLL and synchronization is achieved. Eq. (18) can be generalized as (19) and the overall structure of the MSHDCPLL is shown in Fig. 28. However, the MSHDCPLL is very complicated for real time implementation in digital signal processors.

$$\begin{bmatrix}\mathbf{v}_{dq}^{+1}\\ \mathbf{v}_{dq}^{-1}\\ \mathbf{v}_{dq}^{+5}\\ \mathbf{v}_{dq}^{-5}\end{bmatrix} = \underbrace{\begin{bmatrix}\mathbf{V}_{dq}^{+1}\\ \mathbf{V}_{dq}^{-1}\\ \mathbf{V}_{dq}^{+5}\\ \mathbf{V}_{dq}^{-5}\end{bmatrix}}_{DC\ terms} + \underbrace{\begin{bmatrix}[0] & T_{dq}^{+1-(-1)} & T_{dq}^{+1-(+5)} & T_{dq}^{+1-(-5)}\\ T_{dq}^{-1-(+1)} & [0] & T_{dq}^{-1-(+5)} & T_{dq}^{-1-(-5)}\\ T_{dq}^{+5-(+1)} & T_{dq}^{+5-(-1)} & [0] & T_{dq}^{+5-(-5)}\\ T_{dq}^{-5-(+1)} & T_{dq}^{-5-(-1)} & T_{dq}^{-5-(+5)} & [0]\end{bmatrix}\begin{bmatrix}\mathbf{V}_{dq}^{+1}\\ \mathbf{V}_{dq}^{-1}\\ \mathbf{V}_{dq}^{+5}\\ \mathbf{V}_{dq}^{-5}\end{bmatrix}}_{Oscillations\ terms} \quad (17)$$

$$\begin{bmatrix}\mathbf{V}_{dq}^{*+1}\\ \mathbf{V}_{dq}^{*-1}\\ \mathbf{V}_{dq}^{*+5}\\ \mathbf{V}_{dq}^{*-5}\end{bmatrix} = \begin{bmatrix}\mathbf{v}_{dq}^{+1}\\ \mathbf{v}_{dq}^{-1}\\ \mathbf{v}_{dq}^{+5}\\ \mathbf{v}_{dq}^{-5}\end{bmatrix} - \begin{bmatrix}[0] & T_{dq}^{+1-(-1)} & T_{dq}^{+1-(+5)} & T_{dq}^{+1-(-5)}\\ T_{dq}^{-1-(+1)} & [0] & T_{dq}^{-1-(+5)} & T_{dq}^{-1-(-5)}\\ T_{dq}^{+5-(+1)} & T_{dq}^{+5-(-1)} & [0] & T_{dq}^{+5-(-5)}\\ T_{dq}^{-5-(+1)} & T_{dq}^{-5-(-1)} & T_{dq}^{-5-(+5)} & [0]\end{bmatrix}\begin{bmatrix}\bar{\mathbf{V}}_{dq}^{*+1}\\ \bar{\mathbf{V}}_{dq}^{*-1}\\ \bar{\mathbf{V}}_{dq}^{*+5}\\ \bar{\mathbf{V}}_{dq}^{*-5}\end{bmatrix} \quad (18)$$

where, LPF $= F(s) = \frac{\omega_f}{s+\omega_f}[I]$ *and* $[0] = \begin{bmatrix}0 & 0\\ 0 & 0\end{bmatrix}$

$$\mathbf{V}_{dq}^{*n} = T_{dq}^{n}\begin{bmatrix}v_\alpha\\ v_\beta\end{bmatrix} - \sum_{m\neq n}\left\{T_{dq}^{(n-m)}\right\}\begin{bmatrix}\bar{\mathbf{V}}_d^m\\ \bar{\mathbf{V}}_q^m\end{bmatrix} \quad (19)$$

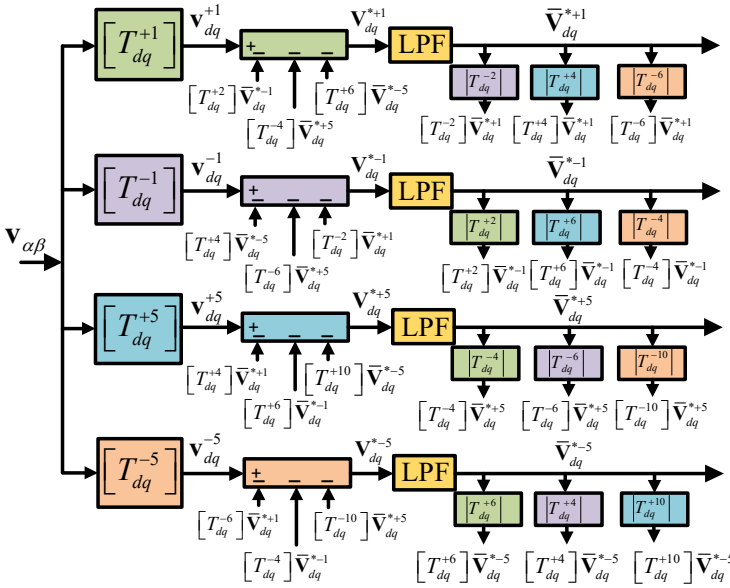

Fig. 27: Multi sequence/harmonic decoupling cell (MSHDC) in the SRF frame.

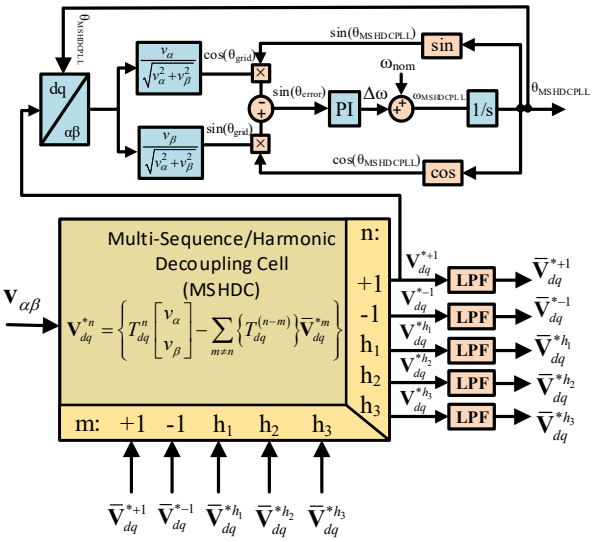

Fig. 28: Block diagram of the multi-sequence/harmonic decoupling cell (see Fig. 27) MSHDCPLL.

3.3.9. DN$\alpha\beta$PLL

The MSHDCPLL provides a fast and accurate grid synchronization under unbalanced faults as well as for distorted grid voltages. The computational complexity, however, of this PLL is high. The MSHDCPLL requires more processing time due to the increased number of Park transformations that are necessary to separate the positive/negative sequence voltages and harmonics. The heavy computational burden motivated a new advanced PLL with a Decoupling Network in the $\alpha\beta$ reference frame (DN$\alpha\beta$) PLL [54]. It provides a fast and accurate synchronization under distorted unbalance grid voltages but with less computations. The decoupling network of [53] is modified for the DN$\alpha\beta$PLL so that it can be implemented in the stationary $\alpha\beta$-reference frame and result is less algebraic calculations. Consequently, space vector transformations are applied to (19) to acquire its equivalent $\alpha\beta$ version. Multiplying both sides of (19) with $\left[\mathrm{T}_{dq}^{-n}\right]$ results in

$$\left[\mathrm{T}_{dq}^{-n}\right]\mathbf{V}_{dq}^{*n} = \left[\mathrm{T}_{dq}^{-n}\right]\left(\mathbf{v}_{dq}^{n} - \sum_{m\neq n}\left[T_{dq}^{(n-m)}\right]\bar{\mathbf{V}}_{dq}^{*m}\right) \quad (20)$$

Which can be further modified with the transformation $\mathbf{v}_{\alpha\beta}^{*n} = \mathrm{T}_{dq}^{-n}\,\mathbf{V}_{dq}^{*n}$ to give

$$\mathbf{v}_{\alpha\beta}^{*n} = \mathbf{v}_{\alpha\beta} - \left[\mathrm{T}_{dq}^{-n}\right]\cdot\sum_{m\neq n}\left[T_{dq}^{(n-m)}\right]\bar{\mathbf{V}}_{dq}^{*m} \quad (21)$$

Substituting the filtered vector estimation $\bar{\mathbf{V}}_{dq}^{*m} = [F(s)]\mathbf{V}_{dq}^{*m}$ into (21), leads to

$$\mathbf{v}_{\alpha\beta}^{*n} = \mathbf{v}_{\alpha\beta} - \left[\mathrm{T}_{dq}^{-n}\right]\cdot\sum_{m\neq n}\left[T_{dq}^{(n-m)}\right][F(s)]\mathbf{V}_{dq}^{*m} \quad (22)$$

The estimated vectors in the m-SRF can also be transformed back into the $\alpha\beta$-frame according to $\mathbf{V}_{dq}^{*m} = \left[\mathrm{T}_{dq}^{m}\right]\mathbf{v}_{\alpha\beta}^{*m}$, and consequently, the final decoupling network in the $\alpha\beta$-frame is given as

$$\mathbf{v}_{\alpha\beta}^{*n} = \mathbf{v}_{\alpha\beta} - \sum_{m\neq n}\left[T_{dq}^{-m}\right][F(s)]\left[\mathrm{T}_{dq}^{m}\right]\mathbf{v}_{\alpha\beta}^{*m} \quad (23)$$

which is shown in Fig. 29. The mathematical model for the desired decoupled voltage vectors in the SRF frame $\mathbf{V}_{dq}^{*n}$ is expressed as

$$\mathbf{V}_{dq}^{*n} = \left[\mathrm{T}_{dq}^{n}\right]\mathbf{v}_{\alpha\beta}^{*n} = \left[\mathrm{T}_{dq}^{n}\right]\left[\mathbf{v}_{\alpha\beta} - \sum_{m\neq n}\left[\mathrm{T}_{dq}^{-m}\right][F(s)]\left[\mathrm{T}_{dq}^{m}\right]\mathbf{v}_{\alpha\beta}^{*m}\right] \quad (24)$$

The estimated vector $\mathbf{v}_{\alpha\beta}^{*n}$, which can be the voltage component of the positive sequence ($n = 1$) or the negative sequence ($n = -1$) or the harmonic order ($n = +5, -5 \ldots$), is first transformed into $\mathbf{V}_{dq}^{*n}$ and then filtered as $\bar{\mathbf{V}}_{dq}^{*n}$. The filtered voltage vector in the $\alpha\beta$-frame is obtained by applying the reverse transformation $\bar{\mathbf{v}}_{\alpha\beta}^{*n} = \left[\mathrm{T}_{dq}^{-n}\right]\bar{\mathbf{V}}_{dq}^{*n}$ and is then subtracted from $\mathbf{v}_{\alpha\beta}$, thereby enabling the decoupling of various frequency components. After the separation of the positive sequence $\mathbf{V}_{dq}^{*+1}$ from harmonics and the negative sequence, the $\alpha\beta$PLL phase detection is used to extract the frequency/phase angle. The Bode diagram of the DN$\alpha\beta$ and the overall structure of the DN$\alpha\beta$PLL are shown in Fig. 30 and Fig. 31, respectively. It is indicated in Fig. 30 that the DN$\alpha\beta$ is able to estimate the positive sequence vector $\mathbf{v}_{\alpha\beta}^{*+1}$ (50 Hz fundamental component) with a unity gain, while it blocks the negative sequence and harmonic components. This efficient extraction of $\mathbf{v}_{\alpha\beta}^{*+1}$ leads to the fast phase angle estimation under highly distorted grid conditions. The modified decoupling network, as shown in Fig. 29, requires considerably less Park transformations, thereby reducing the computational burden. More specifically, the DN$\alpha\beta$PLL requires 76% less execution time when compared to the MSHDCPLL, while maintaining the same performance in terms of tracking accuracy and dynamics for distorted grid voltages. The execution time comparison is based on the mitigation of up to the 11$^{\text{th}}$ order harmonic. The reduced complexity and execution time is an important factor when implementing the algorithm in practice. A complexity analysis is also done in [54], concluding that the MSHDCPLL requires a total of 1040 arithmetic operations in contrast to the DN$\alpha\beta$PLL that requires only 400.

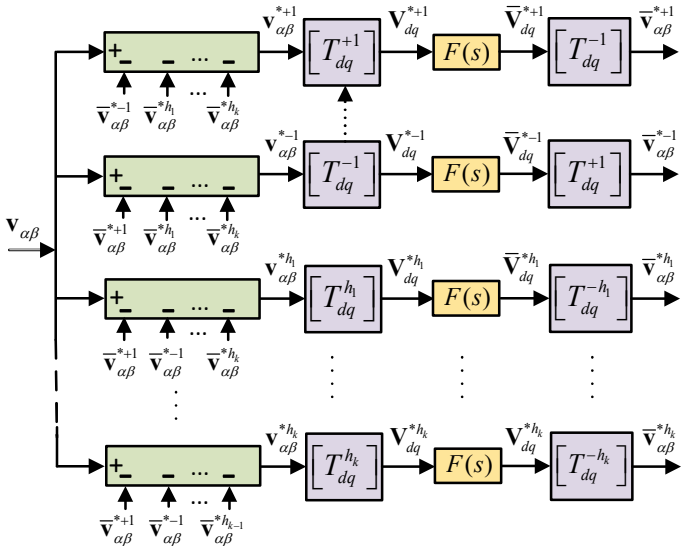

Fig. 29: Multi sequence decoupling network in the stationary αβ-reference frame.

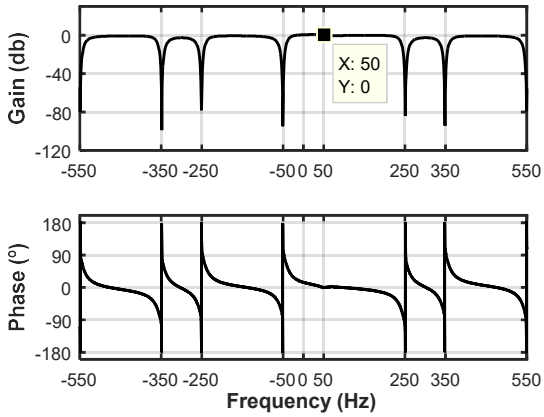

Fig. 30: Bode plots of the decoupling network in the $\alpha\beta$ reference frame ($DN\alpha\beta$).

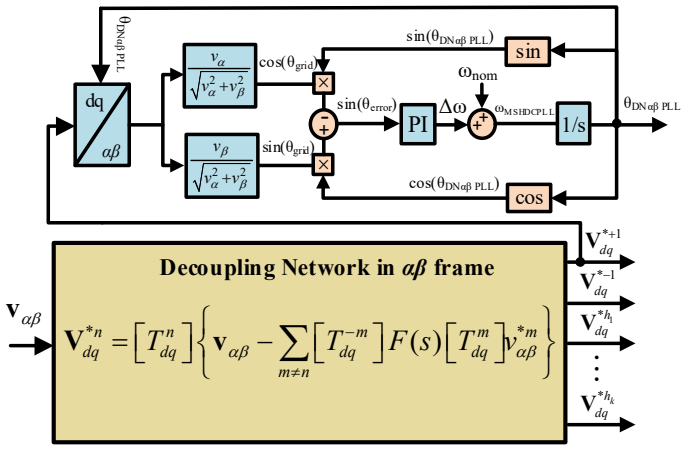

Fig. 31: Block diagram of the $DN\alpha\beta PLL$ system with the decoupling network implemented in the $\alpha\beta$ reference frame.

4. PLL Experimental Comparative Study

The PLLs analyzed above are evaluated experimentally under normal and abnormal grid conditions. A test bench is built up in the laboratory to analyze and compare the performance of various conventional and advanced PLLs in real time conditions. The experimental setup consists of a GSC along with its controller and other peripheral equipment that is used for the RES interconnection, as shown in Fig. 32. This test rig is set up according to the schematic diagram in Fig. 2. The control of the GSC and various PLL algorithms are implemented in a digital signal processing board (dSPACE DS1104) with an integrated real-time platform of the MATLAB/Simulink and the dSPACE Control Desk. A three-phase programmable AC source (California Instrument 2253iX) is used to emulate various grid conditions. An ELEKTRO-AUTOMATIK power supply (EA-PS-9750-20) is used as the dc source to emulate the behaviors of the RES. The GSC is an SEMITEACH inverter (B6U+E1CIF+B6CI). The PLLs under study are the dqPLL, ddsrfPLL, d$\alpha\beta$PLL, DN$\alpha\beta$PLL, MAFPLL, EPMAFPLL, and EPMAFPLL Type 2. Details of the tuning methodologies are given in Appendix I. The tuned parameters are provided in Table 1 and correspond to 100 ms settling time (i.e., the time required to reach and stay within 1% of the steady-state value, when a step change is applied to the phase angle).

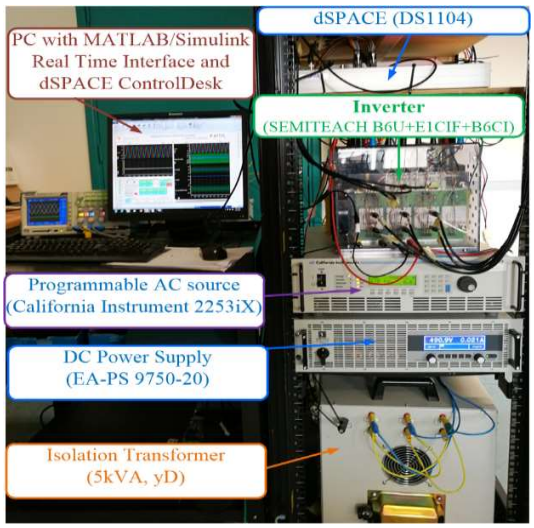

Fig. 32: The experimental setup.

Table 1: Parameters of the PLLs selected for experimental investigation.

Parameters	dqPLL	αβPLL	ddsrfPLL	dαβPLL	MSHDCPLL	DNαβPLL	MAFPLL	PMAFPLL	EPMAFPLL
K_p	92	92	92	92	92	92	41.42	134	134
T_i	0.000235	0.000235	0.000235	0.000235	0.000235	0.000235	0.0014	0.000235	0.000235

Note: Parameter values hold for the grid voltage in p.u. and are calculated using 100 ms settling time with a step-change in phase.

4.3.1. Case I: Response of PLLs to an unbalanced Type A fault with a 50% voltage sag

The first case, case I, analyzes and compares the response of PLLs under a Type A fault (i.e., a single-phase-to-ground fault) with a voltage sag of 50%. Initially, the voltage of all three phases is set to the same as the nominal value of 230 V. All the PLLs respond accurately under balanced and nominal grid conditions. For all experimental plots the disturbance is marked with red arrows. The responses of all PLLs are depicted in Fig. 33 and summarized in Table 2. All the MAF-based PLLs perform accurately, almost with no frequency/phase-overshoots, and zero settling time. The dqPLL and DNαβPLL suffer from higher overshoots in both frequency and phase. The problem with the dqPLL is that it cannot handle unbalanced grid faults and as a result non-decaying oscillations appear in the estimated phase, frequency, and amplitude. When considering the phase error θ_{error} settling time, the DNαβPLL presents the highest, whereas the MAFPLL has the lowest non-zero value. Regarding the estimation of the voltage amplitude V_{amp}, the MAFPLL presents the slowest response (the longest settling time), while the DNαβPLL presents the fastest response.

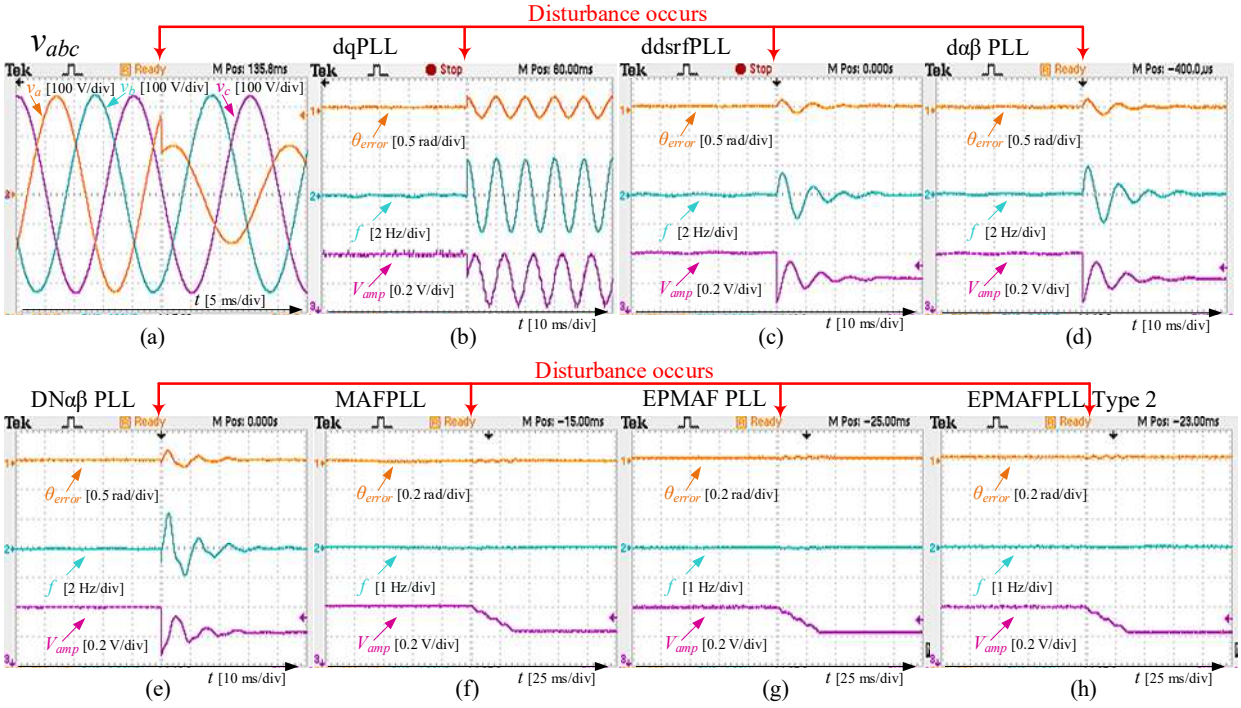

Fig. 33: Experimental results of the selected PLLs under a Type A fault with a voltage sag of 50%.

Table 2: Summary of the Experimental Results presented in Fig. 33.

Type of PLL	**Overshoot/ Maximum Disturbance**		**Settling Time**		
	Frequency (Hz)	**θ_{error} (rad)**	**Frequency (ms)**	**θ_{error} (ms)**	**V_{amp} (ms)**
dqPLL	2.4	0.20	*Inf*	*Inf*	*Inf*
ddsrfPLL	1.6	0.13	36.5	22	32
dαβPLL	2	0.16	36.5	22	32
DNαβPLL	2.4	0.19	30	25	28
MAFPLL	0	0.02	0	0	35
EPMAFPLL	0	0	0	0	35
EPMAFPLL Type 2	0	0	0	0	35

Inf (Infinity): Non-decaying oscillations are observed, and hence settling time is infinite.

4.3.2. Case II: Response of PLLs to a phase fault with a phase change of 20° in phases B and C

The PLL response is investigated under an unbalanced phase change of 20° in phases B and C of the three-phase grid voltage. The response of the PLLs to this phase change is shown in Fig. 34 and further summarized in Table 3.

As expected, the dqPLL does not respond to the unbalanced phase change. The highest overshoot is experienced in the ddsrfPLL, whereas the maximum value of the phase error θ_{error} disturbance is experienced in the dqPLL. The slower response of the MAFPLL can be observed from the frequency and the phase error θ_{error} settling time, which is very high compared to the rest. In the initial review discussion, it was mentioned that the EPMAFPLL and EPMAFPLL Type 2 improve the dynamics of the MAFPLL. This can be verified from the experimental results in Fig. 34 and Table 3. The settling time of the EPMAFPLL and EPMAFPLL Type 2 is less than the conventional MAFPLL. Furthermore, the frequency and phase error θ_{error} overshoots of the EPMAFPLL Type 2 are lower than those of the EPMAFPLL. Moreover, the ddsrfPLL, dαβPLL, and DNαβPLL present a significantly faster response.

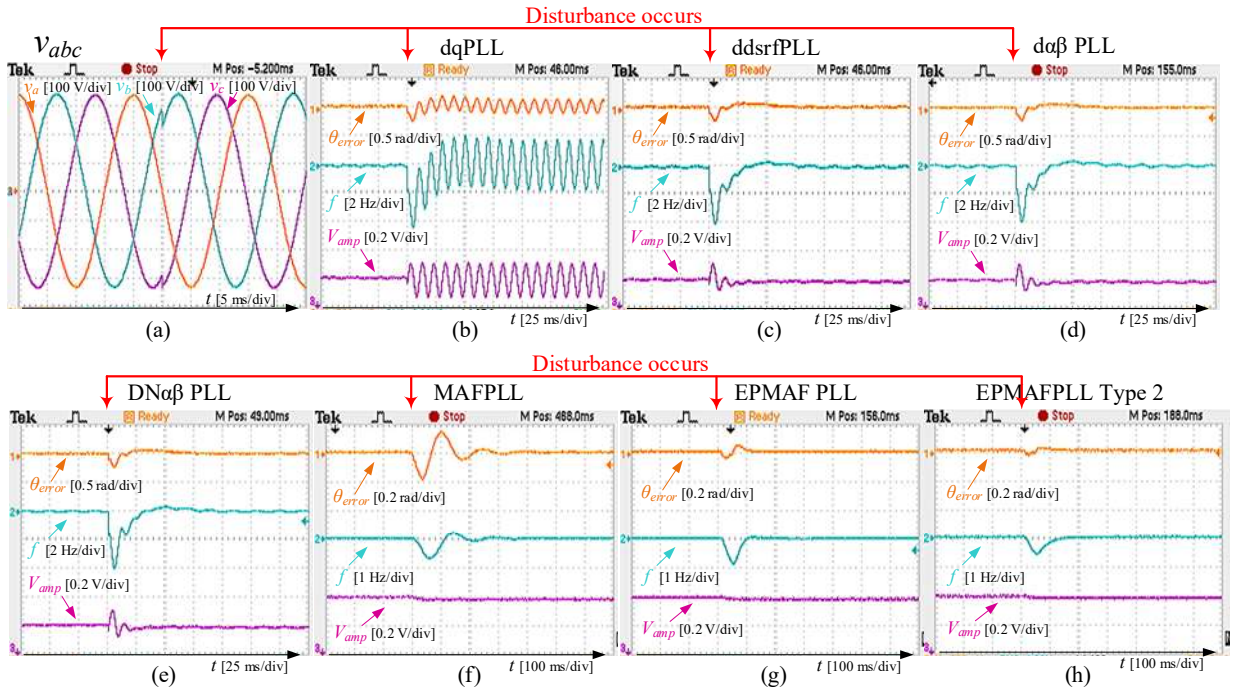

Fig. 34: Experimental results of the selected PLLs under unbalanced phase change of 20°.

Table 3: Summary of the Experimental Results in Fig. 34.

Type of PLL	**Overshoot/ Maximum Disturbance**		**Settling Time**	
	Frequency (Hz)	**θ_{error} (rad)**	**Frequency (ms)**	**θ_{error} (ms)**
dqPLL	4.48	0.285	*Inf*	*Inf*
ddsrfPLL	4.08	0.27	55	50
dαβPLL	4	0.25	75	50
DNαβPLL	4	0.25	75	50
MAFPLL	0.7	0.20	300	300
EPMAFPLL	0.95	0.068	114	120
EPMAFPLL Type 2	0.58	0.12	120	100

Inf (Infinity): Non-decaying oscillations are observed, and hence settling time is infinite.

4.3.3. Case III: Response of PLLs to distorted grid voltages with 5th order harmonic (THD = 10%)

The analysis of PLLs under harmonic distortions is presented in this section. The grid voltage in this case is distorted with +5th order harmonic in all the three phases. This results in a THD of the grid voltage being 10%. The behavior of the PLLs under this condition is depicted in Fig. 35. The frequency/phase-overshoots and settling time durations are given in Table 4. The MAF-based PLLs accurately mitigate the impacts of the harmonic distortion. They perform seamlessly without any explicit oscillations or overshoots. Among the other PLLs, only the DNαβPLL responds accurate and this is because of the extended decoupling network. The dqPLL, ddsrfPLL and dαβPLL cannot compensate for the presence of harmonic distortion and result in undesired oscillations, as shown in Fig. 35.

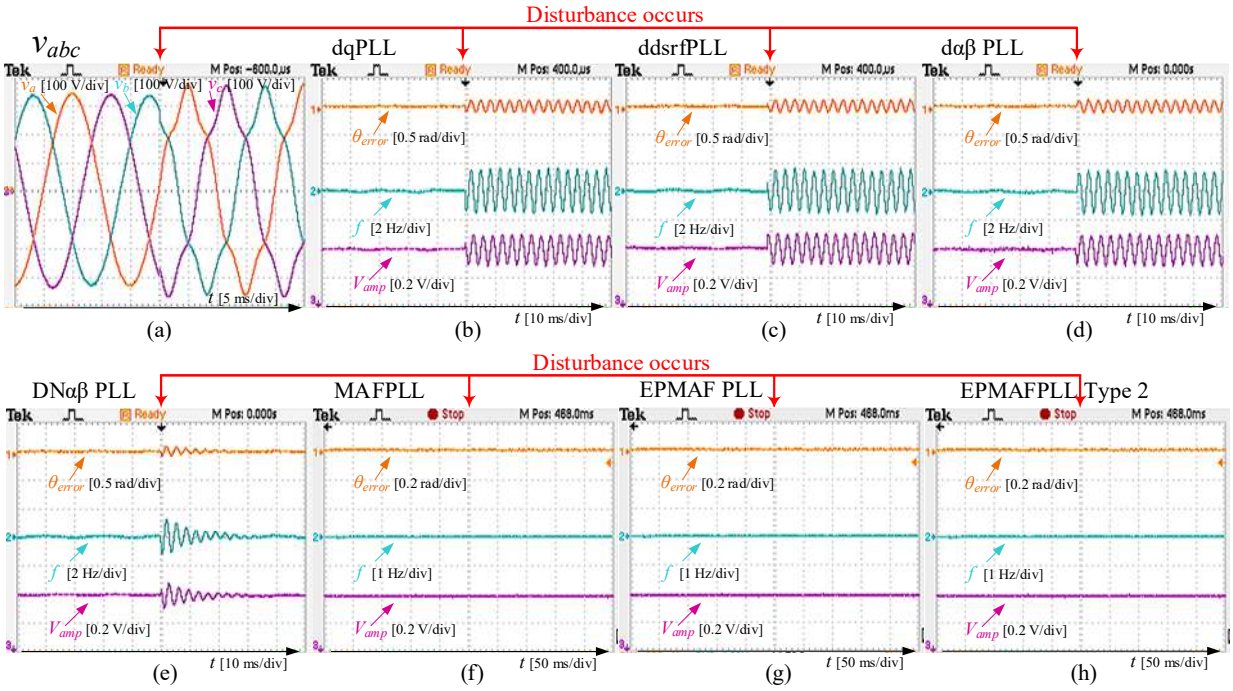

Fig. 35: Experimental results of the selected PLLs in the presence of harmonics in the grid voltage.

Table 4: Summary of the Experimental Results in Fig. 35.

Type of PLL	**Overshoot/ Maximum Disturbance**		**Settling Time**	
	Frequency (Hz)	**θ_{error} (rad)**	**Frequency (ms)**	**θ_{error} (ms)**
dqPLL	1.6	0.1	*Inf*	*Inf*
ddsrfPLL	1.6	0.1	*Inf*	*Inf*
dαβPLL	1.6	0.1	*Inf*	*Inf*
DNαβPLL	1.4	0.1	26	15
MAFPLL	0	0	0	0
EPMAFPLL	0	0	0	0
EPMAFPLL Type 2	0	0	0	0

Inf (Infinity): Non-decaying oscillations are observed, and hence settling time is infinite.

4.3.4. Case IV: Response of PLLs to frequency variation from 50 Hz to 49 Hz

The performance comparison of PLLs is analyzed and compared under a 1 Hz step change in the frequency. The grid frequency is changed from of 50 Hz to 49 Hz. The corresponding responses of the PLLs are presented in Fig. 36 and a result summary is given in Table 5. All the PLLs perform satisfactorily in terms of tracking the new frequency. The slower response of the conventional MAFPLL can be observed in Table 5, as it takes longer time to settle down. Furthermore, the MAFPLL suffers from a fixed offset error of 0.076 rad, as observed in Fig. 36, implying that the MAFPLL cannot perform accurate under non-nominal grid frequency. On the other hand, examining the response of the EPMAFPLL and the EPMAFPLL Type 2, it is seen that that they present very fast dynamics and there exist no offset error. Their settling time is observed to be around four times less than that of the conventional MAFPLL. Furthermore, the phase error θ_{error} settling time of the EPMAFPLL and the EPMAFPLL Type 2 is less than the non-MAF-based PLLs. The phase/frequency settling time for the non-MAF PLLs is however less than the advanced MAF PLLs. Consequently, the dqPLL, ddsrfPLL, dαβPLL, and DNαβPLL enable a faster phase/frequency estimation.

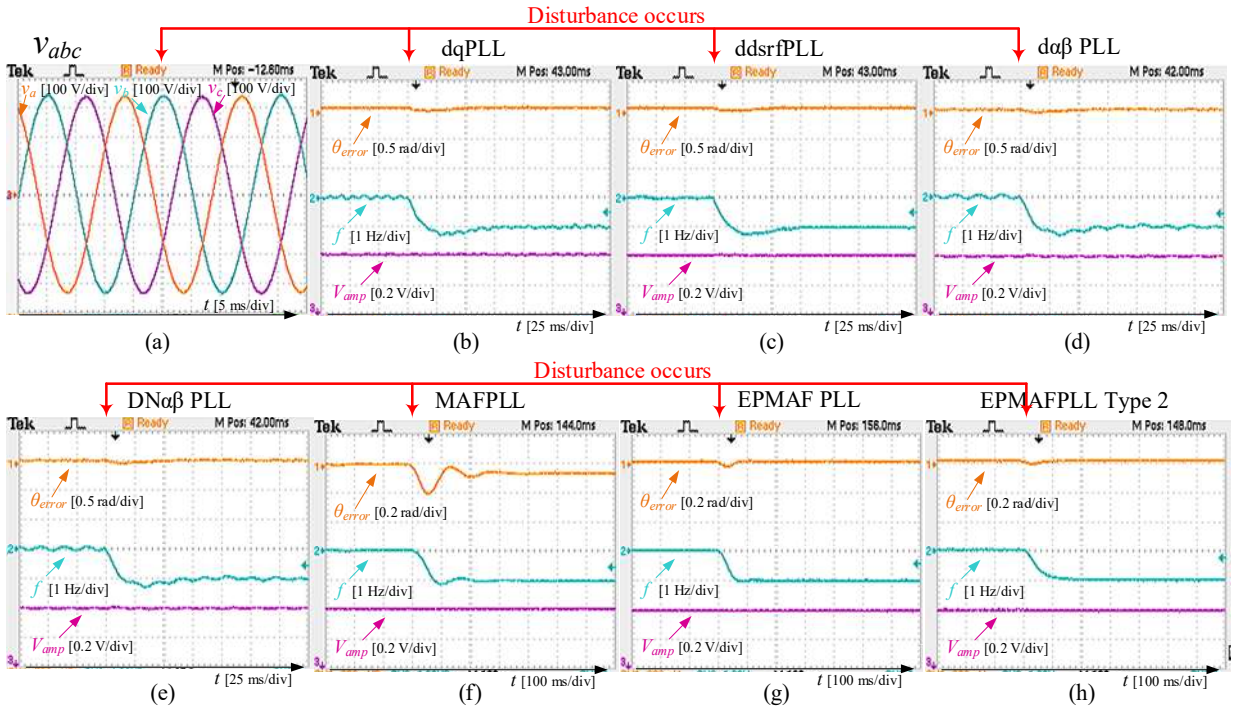

Fig. 36: Experimental results of the selected PLLs under a grid voltage frequency variation.

Table 5: Summary of the Experimental Results in Fig. 36.

Type of PLL	Overshoot/ Maximum Disturbance		Settling Time	
	Frequency (Hz)	θ_{error} (rad)	Frequency (ms)	θ_{error} (ms)
dqPLL	0.34	0.02	75	37.5
ddsrfPLL	0.33	0.02	70	33.75
dαβPLL	0.35	0.09	65	35
DNαβPLL	0.36	0.08	60	35
MAFPLL	0.18	0.206	200	240
EPMAFPLL	0	0.034	60	60
EPMAFPLL Type 2	0	0.01	58	60

4.3.5. Case V: Response of PLLs to a frequency variation from 50 Hz to 49 Hz with distorted grid voltage (THD=10%)

This case study analyzes the response of the PLLs under a frequency variation in the presence of voltage harmonics. The three-phase grid voltage is initially injected with +5th order harmonic of magnitude 10% of the fundamental. A frequency change of -1 Hz follows, as shown in Fig. 37 (a). The response of the PLLs under this disturbance is presented in Fig. 37 and a performance summary is given in Table 6. It can be clearly seen that the dqPLL, ddsrfPLL and dαβPLL are unstable and fail to operate in the presence of harmonics in the grid voltage. The performance of the DNαβPLL is better than the rest, as it takes less time to settle down to the estimated phase and frequency. The slow dynamic response of the conventional MAF is also verified for this case. It is seen that it takes 200 ms and 250 ms for settling time of the estimated phase error and frequency respectively. Between the EPMAFPLL and EPMAFPLL Type 2, the settling time for the phase error θ_{error} is less for the EPMAFPLL Type 2, resulting in a faster phase estimation. The lower harmonic compensation capability of the EPMAFPLL under a non-nominal grid frequency, as discussed in [83], cannot be verified from this experimental comparative study. This is because the PLL is tuned for 100 ms settling time and the oscillations are therefore lower in magnitude. If the PLLs were tuned for 10 ms settling time, the

oscillations observed in the EPMAFPLL would be considerably higher in magnitude as a result of the faster settling time.

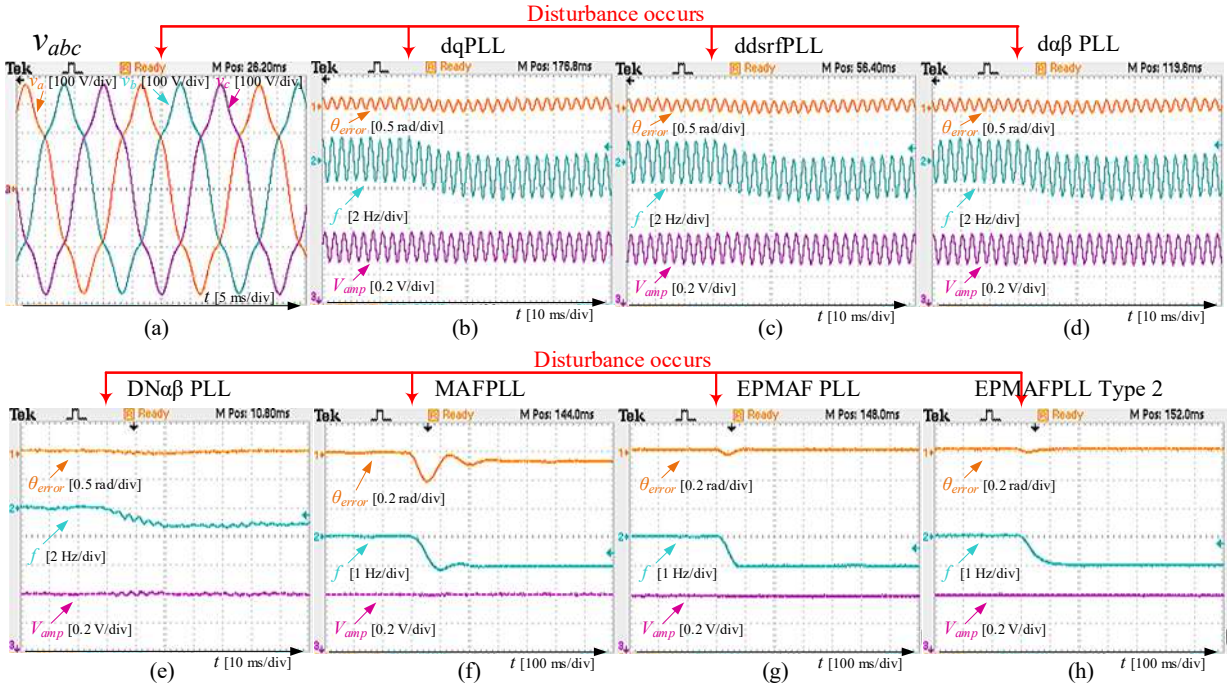

Fig. 37: Experimental comparison for the selected PLLs under grid voltage harmonics and a frequency variation.

Table 6: Summary of the Experimental Results in Fig. 37.

Type of PLL	Overshoot/ Maximum Disturbance		Settling Time	
	Frequency (Hz)	θ_{error} (rad)	Frequency (ms)	θ_{error} (ms)
dqPLL	1.6	0.13	*Inf*	*Inf*
ddsrfPLL	1.6	0.13	*Inf*	*Inf*
dαβPLL	1.6	0.13	*Inf*	*Inf*
DNαβPLL	0	0.09	20	28
MAFPLL	0.2	0.214	200	250
EPMAFPLL	0	0.035	67	60
EPMAFPLL Type 2	0	0.01	100	44

Inf (Infinity): Non-decaying oscillations are observed, and hence settling time is infinite.

4.4. Discussion and comparison summary

A performance comparison has also been carried out among the state-of-the-art PLLs in terms of various performance indices and the results are presented in Table 7. These indices are the frequency/phase overshoot, the computational complexity, the accuracy under unbalanced faults and phase jumps, the immunity against harmonics and inter-harmonics, the dynamic response, the estimation accuracy in the presence of dc offset and response under non-nominal grid frequencies. Initially, the dqPLL, $\alpha\beta$PLL, ddsrfPLL, and the hybrid d$\alpha\beta$PLL are compared. It is found that the hybrid d$\alpha\beta$PLL and ddsrfPLL (or equivalent DSOGIPLL) perform accurately under unbalanced grid faults. Although, the dqPLL and αβPLL present lower complexity, they do not perform accurate under unbalanced faults, as verified from the above experiments. A performance evaluation between the dαβPLL, FPD d$\alpha\beta$PLL and adaptive FPD d$\alpha\beta$PLL shows that the adaptive FPD d$\alpha\beta$PLL significantly enhances the dynamic performance of conventional dαβPLL by accelerating the time response at the cost of a minor increase in the computational complexity. The

experimental verification of the adaptive FPD d$\alpha\beta$PLL is similar to the d$\alpha\beta$PLL with the exception in the tuning of its parameters which are adaptively changed according to the type of faults (hence not included in this paper). The aforementioned PLLs present fast dynamics but they are not immune against harmonic distortions in the grid voltage. For harmonic compensation, a comparative analysis is made amongst the MAFPLL, PMAFPLL, EPMAFPLL, EPMAFPLL Type 2, MSHDCPLL, and DNαβPLL. The results demonstrate that the DNαβPLL and the equivalent MSHDCPLL perform accurate and with improved performance under unbalanced faults and in the presence of harmonics. However, both DNαβPLL and MSHDCPLL are computationally more complicated due to a large number of Park transformations. In addition, they cannot work accurately in the presence of inter-harmonics and dc offset in the grid voltage. Furthermore, although they eliminate selected low-order harmonics, prior knowledge of which harmonics to be compensated is required. Considering that MSHDCPLL and DN$\alpha\beta$PLL are computationally complicated and restricted in compensating harmonics, the MAF-based PLL algorithms present better performances. The MAF-based PLLs achieve very accurate response under grid voltage harmonics compared to all the other PLLs. However, in some cases their performance is poor. For instance, the conventional MAFPLL presents offset errors under non-nominal grid frequencies and has slow dynamics. The EPMAFPLL and EPMAFPLL Type 2 significantly enhance the conventional MAF (as analyzed from experimental results), but compared to other non-MAF PLLs, they are still slower. The MAF-based PLLs can work under dc offset conditions and partially under inter-harmonics. The slower dynamic response of MAF PLLs is however a maor disadvantage and a tradeoff between the accuracy and the dynamic response should be made.

Table 7: Performance Comparison and Guide for State-of-the-art PLLs.

PLL Algorithms	**Frequency/ Phase Overshoot**	**Computational Complexity**	**Dynamic Response under faults**	**Accurate Estimation under**					
				Un-balanced Faults	**Harmonics**	**Phase Jumps**	**Inter-Harmonics**	**dc-offset**	**Off-nominal frequency**
dqPLL	High	Very Low	Fast	No	No	Yes	No	No	Yes
αβPLL	Low	Very Low	Fast	No	No	Yes	No	No	Yes
ddsrfPLL	High	Low	Fast	Yes	No	Yes	No	No	Yes
DSOGIPLL	High	Low	Fast	Yes	No	Yes	No	No	Yes
dαβPLL	Low*	Low	Fast	Yes	No	Yes	No	No	Yes
FPD dαβPLL	Very Low	High	Faster	Yes	No	Yes	No	No	Yes
Adaptive FPD dαβPLL	Very Low	High	Faster	Yes	No	Yes	No	No	Yes
MAFPLL	Low	Very Low	Slow	Yes	Yes	Yes	Partial	Yes**	No
PMAFPLL	Low	Low	Medium	Yes	Yes	Yes	Partial	Yes**	No
EPMAFPLL	High	Low	Medium	Yes	Yes	Yes	Partial	Yes**	Partial
EPMAFPLL Type 2	Low	Low	Medium	Yes	Yes	Yes	Yes	Yes**	Yes
αβEPMAFPLL	Low	Low	Medium	Yes	Yes	Yes	Yes	Yes**	Yes
MSHDC PLL	Low	Very High	Fast	Yes	Yes	Yes	No	No	Yes
DNαβPLL	Low	Very High	Fast	Yes	Yes	Yes	No	No	Yes

*Subjected to the condition of the same settling time. **Compensate the dc-offset only if the MAF window length $T_\omega = 0.02\ s$.

5. Conclusion

This paper enlists a benchmarking on various state-of-the-art PLLs that can be used as guideline for the proper control of grid-connected renewables. A comprehensive implementation analysis containing the details of the schematic diagram, the operating principle, the performance capabilities, and the advantages and disadvantages of each PLL has been discussed. The choice of appropriate PLL depends on the requirements and/or regulations to be fulfilled, as well

as the type of utility grid to be fed by the renewable energy source. The existing state-of-the-art PLLs have many advanced features / capabilities and the computational complexity for the real-time implementation should also play an important role during the selection of appropriate PLL. The comparative study in this work has focused on features critical for the synchronization of grid-connected RES applications. Since the grid synchronization depends on grid parameters and operating conditions, the performance of the PLLs was experimentally investigated under various grid disturbances. The performance indices and capabilities examined are those given above in Table 7. The comparative study has led to a selection guide that may be utilized to aid the selection of the most suitable PLL, which may depend on the specific application, the grid operating conditions, the capabilities required and the criticality of the complexity, speed and accuracy.

Acknowledgment

The authors Zunaib Ali and Nicholas Christofides are highly grateful to the Erasmus Mundus Leaders program for providing PhD fellowship. The authors Lenos Hadjidemetriou and Elias Kyriakides are supported by the Research Promotion Foundation (RPF) of Cyprus under Project KOINA/SOLAR-ERA.NET/1215/06.

Appendix A. Tuning of Three-Phase PLLs

A.1. Tuning for Second-Order PLLs

The tuning of the PI controller is a crucial aspect in the PLL design as it affects the estimation accuracy and time response of the PLLs. Most of the work published in literature [29, 34, 53, 54, 57, 78, 79, 86] used the linearized small signal model (shown in Fig. 3) for calculating the parameters k_p and $k_i = 1/T_i$. The phase detector constant, K_{PD}, is set to 1 for simplicity. The transfer function of the PI controller used in the loop filter stage is given by (A.1). The closed loop transfer function can be represented by (A.2).

$$L_f(s) = \frac{V_{L_f}}{\theta_{error}} = k_p + \frac{1}{T_i s} \qquad (A.1)$$

$$T_\theta(s) = \frac{\theta'}{\theta_{grid}} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{k_p s + \frac{1}{T_i}}{s^2 + k_p s + \frac{1}{T_i}} \qquad (A.2)$$

where θ' is the estimated PLL angle and θ_{grid} is the actual phase angle of the grid voltage. The response of the approximated second-order linearized PLL transfer function is presented in different control system books, including references [34, 86]. The transfer function in (A.2) presents low pass filtering characteristics and the stability of the tuned PLL is ensured. In addition, the inaccuracies caused by higher order frequencies and noise signals are also attenuated. The response of (A.2) can be described by its settling time (T_s), defined as $T_s = 4.6/\zeta\omega_n$, and the damping factor ζ. The settling time actually represents the time needed by the system to reach within 1% of the steady state under a step change in the input signal and is adjusted by varying k_p and T_i. For achieving an optimally-damped response, the value of ζ is set to $1/\sqrt{2}$. Considering the transfer function of (A.2), the natural frequency $\omega_n = 1/T_i$ and the damping factor $\zeta = k_p\sqrt{T_i}/2$. Therefore, the parameters k_p and T_i are calculated according to (A.3) and are valid for the grid voltage in p.u.

$$k_p = \frac{9.2}{T_s} \qquad and \qquad T_i = \frac{\zeta^2 T_s^2}{21.16} \qquad (A.3)$$

A.2. Tuning for the Conventional MAF PLL

For those MAF PLLs for which the filter appears within the closed-loop control path, a 3rd order transfer function exists. The tuning of the 3rd order transfer function is not straightforward and is normally done according to the Symmetrical Optimum Method (SOM) [47, 103-106]. The SOM calculates the PI parameters using the open loop transfer function of the PLL and the resultant parameters are expressed in terms of phase margins (stability index).

The open loop transfer function for such PLLs (a PI controller as the loop filter) is shown in (A.4). The resultant parameters according to the SOM are given by (A.5).

$$T_\theta(s) = \frac{\theta'}{\theta_{grid}} = \frac{\omega_p\left(k_p s + \frac{1}{T_i}\right)}{s^2\left(s+\omega_p\right)} = \frac{\frac{2}{T_\omega}\left(k_p s + \frac{1}{T_i}\right)}{s^2\left(s+\frac{2}{T_\omega}\right)} \qquad (A.4)$$

$$k_p = \omega_c = \frac{\omega_p}{b} = \frac{2}{b \cdot T_\omega} \quad and \quad T_i = \frac{b}{\omega_c^2} = \frac{b}{\left(\omega_p/b\right)^2} = \frac{b^3 T_\omega^2}{4} \qquad (A.5)$$

where, b is a design constant related to the desired Phase Margin (PM) and $\omega_c = \omega_p/b$ is the cross over frequency. The corresponding value of b for the desired phase margin is calculated according to

$$PM = \tan^{-1}\left(\frac{b^2-1}{2b}\right) \qquad (A.6)$$

References

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