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by

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English summary

With the advancements in the past decades on the development of Silicon (Si) based devices, the physical limits of the Si material have been pushed close to the limits, and the researchers have been focused on finding a suitable replacement for the Si semiconductors.

Silicon-Carbide (SiC) materials, due to their physical properties, promise to provide improved performances in terms of breakdown voltages, switching frequency and operating temperatures in semiconductor switching devices. Continuous research in this field has already brought to the market SiC devices with voltages up to 3.3 kV which demonstrated superior performances compared to their Si counterparts in terms of efficiency and operating junction temperature. This also translated to a certain extent in improved reliability when considering the lower operating temperature of the Si devices for a similarly size heatsink.

Due to material properties and continuous research, 10 kV 4H-SiC devices are currently under development as engineering samples. These promise to be a good candidate for replacing Si based IBGTs in the high power high voltage applications where an improved efficiency and higher switching frequency could decrease the converter costs and size while offsetting the semiconductor higher price.

A very important requirement for power electronics devices employed in power converters is their reliability and behavior during transients such as short-circuits. This is highly relevant as the device needs to be able to sustain and safely turn-off such a transient in order for it to be consider as a suitable candidate for high voltage high power converters, where reliability is a key requirement.

Therefore the investigation of the behavior of the 10 kV 4H-SiC device during short-circuit and its degradation mechanism is of high interest. This summarizes both degradation during single event long short-circuit pulses but also during short and repetitive short-circuit events, which initially would not appear as a stress.

The work developed during the Ph.D. studies the 10 kV 4H-SiC DMOSFETs from Wolfspeed/Cree both in terms of device characteristics and short-circuit robustness. Chapter one introduces the challenges and motivation of the research.

Afterwards, in chapter two a theoretical comparison between unipolar SiC and Si devices is presented, together with specific unipolar figures of merit, aimed at

highlighting the superior characteristics of the SiC material, as its limits have yet to be reached by current SiC devices on the market.

Chapter three makes a short introduction into the power MOSFETs, their characteristics and behavior. Afterwards the history and evolution of SiC unipolar devices is presented. In the last part of the chapter a low inductance test setup designed for 10kV 4H-SiC MOSFETs is presented. This, together with a high performance curve tracer is used to characterize the static and dynamic behavior of the first generation 10 kV 4H-SiC MOSFETs from Wolfspeed/Cree.

In chapter four, the short-circuit behavior of the first generation 4H-SiC MOSFETs are investigated. Initially, the maximum short-circuit withstand time capability is estimated using a conservative approach. This was used in order to obtain a benchmark and to observe the behavior of the device during long pulses. Encouraged by the behavior and observed degradation during prolonged short-circuit pulses, a further study aimed at observing and recording the degradation was performed. By periodically recording the degradation in the static measurements thought-out the short-circuit stressing of the device, some observations regarding the degradation could be drawn. A 1D thermal simulation was also set up in order to investigate the temperature evolution inside the device during short-circuit which aided at understanding some of the possible degradations of the device during such transients. Scanning electron microscope images confirmed the very high temperatures achieved in the device during such transients.

Chapter five presents the conclusions and observations of the work and proposes some future investigations which might be performed in order to enhance this work and better understand the novel device.

The main contribution of this project is in the short-circuit investigation process and methods. This allows for a better understanding of the device failure mechanism and steps and future improvements in device robustness during short-circuit transients.

Dansk resume

I takt med udviklingen indenfor silicum-baserede effektkomponenter er man rykket tættere på de fysiske materiale-relaterede begrænsninger for silicium. Som en følge deraf fokuserer en øget del af forskningen på at finde alternative materialer der kan erstatte silicium komponenterne.

Et eksempel på et lovende alternativt material er siliciumkarbid (SiC) der som materiale med et stort båndgåb potentielt har en række interessante fysiske egenskaber såsom større spærrespænding, mulighed for øget switch-frekvens samt evne til at virke ved højere temperaturer. Den fortsatte forskning indenfor dette felt har udmøntet sig i SiC komponenter der kan klare spændinger på op til 3.3kV og som udviser forbedrede egenskaber i forhold til effektivitet såvel som maksimalt tilladt driftstemperatur. Sidstnævnte kan desuden give øget pålidelighed sammenlignet med den lavere driftstemperatur i Si komponenter under samme kølevilkår.

10kV komponenter lavet af SiC typen 4H-SiC er under udvikling og såkaldte ”engineering” komponenter er blevet realiseret af Wolfspeed (Cree). Sådanne komponenter kan være velegnede kandidater til at erstatte Si baserede IGBT komponenter indenfor anvendelsesområder med høj effekt og høj spænding, hvor en forøget effektivitet og muligheden for en øget switching frekvens potentielt kan reducere converteres størrelse og pris og dermed kompensere for den forventeligt højere enhedspris på SiC komponenter i forhold til Si.

En meget vigtig parameter for effektelektroniske komponenter der anvendes i effekt convertere er pålidelighed og robusthed under store transienter som det er tilfældet under kortslutnings hændelser. Det er afgørende at de nye komponenter kan modstå sådanne hændelser og slå fra på en sikker måde hvis de skal tages i betragtning som brugbare alternativer indenfor høj effekt / høj spænding anvendelsesområder, hvor driftssikkerhed og pålidelighed er centralt.

Dette understreger interessen i og vigtigheden af at studere egenskaberne ved 10kV 4H-SiC komponenter under kortslutningshændelser og hvilke nedbrydningsmekanismer sådanne eventuelt måtte udløse. Interessefeltet indebærer både nedbrydning under enkeltforekommende kortslutningshændelser af lang varighed såvel som under korte men gentagne kortslutningshændelser, hvoraf sidstnævnte under enkeltforekomster normalt ikke ville give anledning til nedbrydning men ved gentagne hændelser kan give anledning til nedbrydning over længere tid.

Arbejdet, der er udført under Ph.D. forløbet og som beskrives i nærværende rapport, har været fokuseret på 10kV 4H-SiC DMOSFET's fra Wolfspeed(Cree) både hvad angår komponentkarakterisering såvel som kortslutningstests. I første kapitel introduceres udfordringer og kontekst for arbejdet og motivationen for dette uddybes.

I kapitel to sammenlignes unipolære SiC and Si komponenter suppleret med specifikke "figures of merit" med sigte på at fremhæve de fordelagtige egenskaber ved SiC materialet. De eksisterende kommercielt tilgængelige SiC komponenter har endnu ikke nået til SiC materialets grænser i samme omfang som Si komponenter og en sammenligning udelukkende baseret på tilgængelige komponenter ville dermed undervurdere nogle af de potentielle fremtidige gevinster ved SiC.

Kapitel tre giver en kort indføring I effekt-MOSFET komponenter og deres karakteristiske egenskaber, efterfulgt af udviklingshistorien for unipolære SiC komponenter. Kapitlet afrundes med en beskrivelse af den lav-induktive testopstilling der er blevet designet og udviklet under forløbet. Denne opstilling har i kombination med karakterisering i en avanceret komponent-analysator dannet grundlag for karakteriseringen af 10kV komponenternes statiske såvel som dynamiske egenskaber.

I kapitel fire præsenteres undersøgelserne af kortslutnings-egenskaberne af 4H-SIC komponenterne. Som første trin undersøgtes den maksimale tid som komponenterne kan klare uden nedbrud ved hjælp af en "forsigtigheds" tilgang. Dette blev gjort for at etablere et referencegrundlag og for at etablere kendskab til komponenternes respons under længerevarende kortslutningspulser. Inspireret af observationere fra de første undersøgelser blev et yderligere studie i værksat med sigte på mere systematisk at undersøge nedbrydningsprocesserne. Ved periodisk at observere og registrere nedbrydningstegn mellem forsatte kortslutningstests blev det muligt at identificere delelementer i komponenternes nedbrydning. Eksperimenterne blev suppleret med en numerisk 1D termisk model for at undersøge temperaturudviklingen i komponenterne og dermed opnå mere indsigt i de mulige mekanismer der kan være i spil under de transiente kortslutningshændelser. De høje temperaturestimater fra simuleringerne blev understøttet af undersøgelser foretaget med Scannende Elektron Mikroskopi (SEM) efter kortslutningstestene var afsluttet.

Kapitel fem sammenfatter observationerne og konklusioner på arbejdet og der anvises desuden mulige fremtidige undersøgelser der kunne udspringe af de fundne resultater og som ville udbygge forståelsen af disse nye komponenter.

Det primære bidrag fra arbejdet I dette projekt ligger i den systematiske afdækning af kortslutningshændelserne og metoderne der er anvendt dertil. Dette giver mulighed for en dybere forståelse af fejlmekanismerne og nedbrydningstrin i de nye

komponenter og kan give vigtige bidrag til den videre udvikling af sådanne komponenter i forhold til deres robusthed under kortslutningshændelser.

Acknowledgements

As I am writing this part, I am finishing one of the last tasks in my PhD studies. It has been quite and adventure for me, started more than 3 years ago which challenged me constantly and motivated my hunger to learn. I would like to express my gratitude and appreciation to every person that has helped me grow and evolve throughout this journey.

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Emanuel-Petre Eni
July 2017, Munich

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Nomenclature

μ_0	-	Permeability of free air
μ_e	-	Electron mobility
μ_n	-	Hole mobility
2G	-	Second generation
3G	-	Third generation
A	-	Area
AC	-	Alternating current
Al	-	Aluminum
A_{opt}	-	Optimal area
BFOM	-	Baliga figure of merit
BHFFOM	-	Baliga high frequency figure of merit
BJT	-	Bipolar junction transistor
BV	-	Breakdown voltage
c	-	Velocity of light
C	-	Capacitance
CAD	-	Computer aided design
C_{DC}	-	DC-link capacitance
C_{DS}	-	Drain-source capacitance
C_{GD}	-	Gate-drain capacitance
C_{GS}	-	Gate-source capacitance
C_{ISS}	-	Input capacitance
C_{OSS}	-	Output capacitance
C_{RSS}	-	Reverse transfer capacitance
D_F	-	Freewheeling diode
DMOSFET	-	Double-implanted MOSFET
DPT	-	Double pulse tester
DUT	-	Device under test
E_C	-	Critical electric field
E_{DS}	-	Peak electric field
E_g	-	Bandgap
E_{max}	-	Maximum electric field of the junction
E_{off}	-	Turn-off switching energy
E_{on}	-	Turn-on switching energy
$E_{SC,max}$	-	Maximum short-circuit energy
ε_S	-	Dielectric constant
f	-	Switching frequency
FET	-	Field effect transistor
f_{max}	-	Maximum operating frequency of unipolar device as a function of ratings and dimensions
FOM	-	Figure of merit
GaN	-	Gallium nitrate
GCT	-	Gate-controlled thyristors

g_m	-	Transconductance
g_{m0}	-	Internal transconductance
GTO	-	Gate turn-off transistor
HVDC	-	High voltage direct current
I_0	-	Load current
I_D	-	Drain current
I_{Dsat}	-	Drain saturation current
I_G	-	Gate leakage current
$I_{g,av}$	-	Average gate current
IGBT	-	Insulate gate bipolar transistor
I_L	-	Inductor current
I_{RMS}	-	RMS current
I_{rr}	-	Diode reverse recovery current
JBS	-	Junction barrier Schottky diode
JFET	-	Junction field effect transistor
JFOM	-	Johnson figure of merit
k	-	Ratio of the date-drain overlap vs entire chip size
KFOM	-	Keyes figure of merit
L	-	Inductor
l	-	Length of sleeve and capacitor
LDMOSFET	-	Lateral DMOSFET
MOSFET	-	Metal oxide field effect transistor
N_D	-	Doping concentration in N-region
P_{loss}	-	Total power losses
$P_{loss,min}$	-	Minimum power loss of the unipolar device
PV	-	Photovoltaics
PWM	-	Pulse width modulation
q	-	Electron charge
Q_g	-	Gate charge
Q_{gd}	-	Gate-drain charge
$Q_{gd,sp}$	-	Specific gate-drain charge
R	-	Radius of the sleeve
r	-	External radius of the capacitor
R_{ch}	-	Channel region resistance
R_{Drift}	-	Drift region resistance
$R_{DS,on}$	-	On-state resistance
R_{ext}	-	External gate resistance
R_g	-	Gate resistance
R_{gint}	-	Internal gate resistance
$R_{on,sp}$	-	Ideal specific on-state resistance of the drift regions
R_S	-	Residual resistance
SC	-	Short-circuit
Si	-	Silicon
SiC	-	Silicon carbide
SOA	-	Safe operating area

t	-	Time
τ	-	Time constant
$t_{d(on)}$	-	Turn-on delay time)
t_f	-	Fall time of the drain current
T_j	-	Junction temperature
t_r	-	Rise time of the drain current
t_{rr}	-	Reverse recovery time
UMOSFET	-	Trench MOSFET
V_a	-	Applied reverse bias
V_{DC}	-	DC-link voltage
VDMOSFET	-	Vertical DMOSFET
V_{DS}	-	Drain-source voltage
V_{GG}	-	Applied gate voltage
V_{GS}	-	Gate-source voltage
V_{in}	-	Input voltage terminal
$V_{plateau}$	-	Plateau voltage
v_s	-	Electron saturation velocity
V_{th}	-	Threshold voltage
W	-	Thickness of the depletion region
WBG	-	Wide bandgap
W_D	-	Thickness of the drift layer
ΔV	-	Voltage drop
λ	-	Thermal conductivity

Chapter 1.
Introduction

This chapter discusses the background, motivation and problem formulation of the PhD dissertation. Afterwards it presents the main objectives and in the end a list of selected scientific contributions carried out in this project.

1.1. Limitation of Silicon-based power devices

Nowadays, power electronics devices process over 70% of the electricity either for industrial users, power generating companies or home appliances [2]. Power semiconductor devices have been a key enabling technology in the regulation and distribution of power and energy around the world for the past few decades. Research and breakthrough on modern power electronics started with the invention of the bipolar junction transistor and semiconductor diodes in the 50s and the thyristor in the 60s. These created the foundations of modern power semiconductors as it is known today. Over the next decades, the desire to obtain more control over the power semiconductor devices fueled the research on improvements of the bipolar junction transistor switching speeds and the invention of the power metal-oxide-semiconductor field effect transistors (MOSFETs) and Insulated Gate Bipolar Transistors (IGBTs) [3]. Figure 1-1 summarizes the main industrial applications for power semiconductor devices; with the boxes indicate the current and voltage requirements from the devices. Generally, devices with voltage

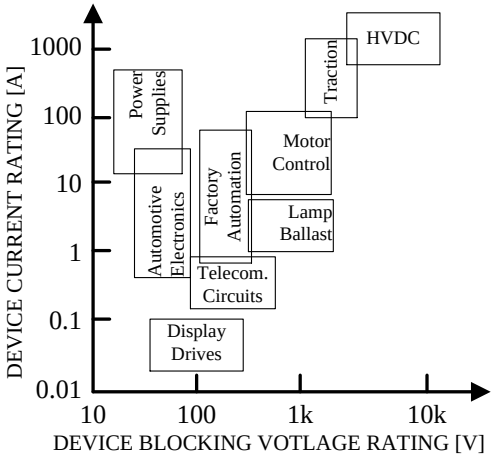

Figure 1-1 Applications of silicon power devices [1]

ratings above 1 kV are mainly used in High Voltage Direct Current (HVDC) and traction applications.

Silicon (Si)-based semiconductor devices have been the main focus of the research and development during the last half-century. Because of this, the material theoretical limits have almost been reached, and most breakthroughs are now related to improving the characteristics and reliability of Si devices; as the manufacturing process has been perfected to obtain a high yield with minimal defects [3].

As the power devices market matured, the demand from the Si semiconductors has increased to the point that further increase in performance are difficult to achieve and complex design solutions have to be selected. The main types of high voltage Si-based devices currently employed in the power systems are thyristors, gate turn-off thyristors (GTOs), gate-controlled thyristors (GCTs), bipolar junction transistors (BJTs), IGBTs and MOSFETs.

Considering the low power applications, like PV-systems and motor drives, the main requirement from the power semiconductor devices, excluding reliability, is the system efficiency. In order to increase the efficiency of such systems, most designers have chosen more complex converter structures like three level converters, which employ series connection of power devices and complex control schemes when compared to the simpler two level half bridge configuration. This switch has allowed them to achieve efficiencies above 96% due to the lower switching losses of 600V Si IGBTs and MOSFETs and a reduction in the output filter losses [4].

Another example are the high voltage applications (e.g. HVDC), in which in order to achieve the high voltage blocking requirements of up to hundreds of kV, lower voltage Si devices like GTOs or Thyristors are stacked in series. As the application voltages increase this becomes a complex design, in order to avoid uneven voltage sharing between the blocking devices, and expensive, from the packaging, cooling and control points of view.

Current power electronics market demands in terms of blocking voltages, switching frequencies, efficiency, power density and reliability are going beyond the material limits of silicon devices and forced device manufacturer to start investigating new materials to replace Si in the power devices over the next years.

1.2. Influence of Silicon-Carbide semiconductors on the high voltage power electronics devices market

In order to surpass the Si material limitations and develop the next generation power semiconductor devices, for the past decades, research has been focusing on

Table 1-1 Material properties of Si and major WBG semiconductors [6]-[9]

Property	Unit	Si	4H-SiC	6H-SiC	GaN	Diamond
Bandgap (E_g)	eV	1.11	3.26	2.9	3.45	5.45
Dielectric constant (ε_s)	-	11.7	9.7	9.7	9	5.5
Critical Electric Field (E_C) (N_D=10^{17}cm^{-3})	MV/cm	0.6	3.5	3.5	3	10000
Electron Mobility (μ_e)	cm^2/Vs	1420	1000	380	1250	2200
Hole Mobility (μ_n)	cm^2/Vs	450	115	95	850	850
Thermal Cond. (λ)	W/cmK	1.5	4.9	4.9	1.3	22
Electron Saturation Velocity (v_s)	10^7cm/s	1.05	2	2	2.2	2.7

wide bandgap semiconductor materials. Among the wide range of such materials, the most promising ones are compared against Si in Table 1-1.

By considering the material properties summarized in Table 1-1, the main advantages of WBG devices compared to Si-based ones are higher operating temperatures, higher breakdown voltage, higher thermal conductivity and higher switching frequency.

From a material point of view, the bandgap of the semiconductor determines the maximum operating temperature. Thus, if a maximum operating temperature for a Si-based device is assumed to be 150 °C, by multiplying this to the bandgap ratios of the WBG, it can be clearly seen that SiC-based and GaN-based devices can operate at temperatures of 400 °C [3], [5]. Therefore, WBG-based devices can operate at higher temperatures when compared to Si, without affecting their electrical properties.

The breakdown voltage of the WBG devices is higher compared to Si-based devices due to the higher critical electric field for a similar doping level. Assuming the case of a diode, for a similar doping level, the theoretical breakdown voltage of a SiC device can be around 50 times higher when compared to a Si one [3]. At the same time, a higher critical electric field allows for a higher doping level to be used, thus the width of the drift region can be reduced. This will result in a thinner drift region for the WBG devices for the same blocking voltage when compared to Si. For a similar breakdown voltage design, SiC and GaN devices drift region can be much thinner than that of Si-based devices. This in terms will result in a small capacitance, fast switching speeds and maximum operation frequency and a small on-state resistance and lower conduction losses for the WBG devices [3], [5]. Considering majority carrier power electronics devices, such as MOSFETs, a 10 fold reduction in blocking layer thickness, combined with a 10 times higher doping concertation for a SiC device will result in a reduction of the on state resistance up to a factor of 100 when compared to Si.

The thermal conductivity of the semiconductor is highly important where the heat generated from the device losses needs to be dissipated and the junction temperature of the junction kept low. Considering high power applications, especially in the case of high ambient temperatures, good heat dissipation is highly desirable as this would result in a lower junction temperature and a higher power density. Considering the SiC-based devices, their thermal conductivity (4.9 W/cm·K) is more than times bigger than that of Si (1.5 W/cm·K), allowing the devices to obtain a greater power density when compared to Si. On the other hand, GaN based devices fail short of this due to the low thermal conductivity, which is even worse than that of Si, making them more suitable for low power devices for high frequency applications [3], [5].

The maximum theoretical switching frequency of the semiconductors is mainly determined by their electron saturation velocity and the device capacitance. The electron saturation velocity defines the time in which the charges in the depletion region can be removed. Since WBG devices have a higher electron saturation velocity, their reverse recovery losses are much smaller, allowing for faster switching times and lower switching losses when compared to Si devices [3], [5]. Also, being thinner makes the device parasitic capacitances smaller, allowing for a faster charging/discharging of those capacitances, and in turn, faster commutation speeds of the devices.

Despite the above mentioned advantages of WBG-based devices, they also present some challenges and disadvantages when compared to Si, which need to be solved in order to take full advantage of their physical properties and adopt them as the default material for power semiconductors.

Cost and reliability are some of the main considerations which make SiC devices unattractive to power electronics systems designer. In order for the devices to be price competitive, low defect density and large diameter wafers are required. Micropipes, dislocations, misoriented blocks, strain, intrinsic point defects and mosaicity reduce the yield of the manufacturing process and are greatly affecting the devices performances while increasing the cost of production. Due to the bulk growth method, SiC bulk crystals have long been plagued in the past by "micropipes", which are the open core of a super screw dislocation which created micron sized holed thought the entire crystal. The density of this type of defect has been currently reduced to less than 0.5 cm^{-2} for all wafer sizes [10]. Due to the device manufacturing process, a high density of interface states is created (10^{13} cm^{-2}), when the semiconductor is oxidized in order to create the gate dielectric [11]. These will affect the device threshold voltage, which might deviate up to 1 V (40% deviation) and will create instability [3]. This type of defect has been reported as largely minimized in [10] and the threshold voltage showed a maximum 280 mV shift after 1000 hours of stressing at high temperature. Another concern is the low channel mobility, as a consequence of the increased surface roughness

scattering (as a consequence of the higher surface fields present in SiC MOSFETs) and coulombic scattering from the interface traps [12]. Similar to the micropipes and high density interface states reductions, all of the other defects can be reduces through improvements of the manufacturing process.

Another disadvantage for the WBG-devices is the necessity of modifying current circuit designs and topologies in order to accommodate these devices. Generally the gate driving circuit requires a low inductive path in order to fully utilize the fast switching capabilities of the devices and a bipolar power supply with large voltage swings. In the case of SiC MOSFETs, the recommended turn-on gate voltages can reach +20 V and -5 V in the case of turn-off. The turn-on requirement is related to the transconductance, which is generally small even at gate voltages under 16 V, even if the threshold voltage is between 2.5 V – 4 V. For the turn-off, due to the smaller thickness of the devices, and the very fast switching events Miller parasitic turn-on can appear if the gate bias voltage is not low enough or the gate power supply can't sink the transient currents [13].

1.3. Evolution of Silicon-Carbide

Silicon-Carbide is one of the oldest semiconductors in the world, and interesting enough, it was first synthesized artificially in 1891 [14] before being discovered in nature in 1905 [15], although all the SiC used today is artificially synthesized. Although as a material it is widely used in industries such as aerospace, furnaces and wear-resistance mechanical parts, its adoption in the power electronics market is still at the beginning. It is composed of equal parts of carbon and silicon, with each atom being bonded to four opposite type atoms in a tetrahedral bonding structure. The bond length between Si and C is 1.89Å and the lattice along the a axis (distance between two atoms of the same type) is 3.08Å as shown in Figure 1-2. The atoms in each layer can be arranged in three positions (A, B and C) and the sequence of stacking determines the SiC polytype, as shown in

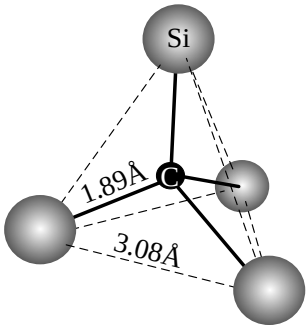

Figure 1-2 Smallest building element of SiC: Thetrahedron of one C atom bonding with four Si neigboring atoms [7]

Figure 1-3. The lattice along the c axis ([1120] plane) is 10.053Å for 4H-SiC and 15.117Å for 6H-SiC. The type of structure of the polytype (cubic, hexagonal and rhombohedral structure) is given by the way the layers stacked on top of each other are oriented, such as lateral translations and rotations. Currently, over 215 SiC polytypes have been discovered, but only the 4H, 6H hexagonal and 3C cubic are of interest. The designators for each polytype comes from the number of layers in sequence, followed by H, R or C which indicates to which class of structure the polytype belongs [8], [16].

SiC-semiconductor has been considered since the 50's as the next generation material in power electronics as a replacement, once Si reaches its material limits [7], [17]. The recent commercialization of such devices is expected to revolutionize the power electronics market. As the technology matured, and the demand increased, it allowed for the wafer size to be increased and cost to be optimized. Figure 1-4 shows the advancements from 75 mm wafers in 2003, to 100 mm in 2008 and, recently, to 150 mm in 2015. Currently, only 4H- and 6H-SiC wafers are available with diameters up to 150mm for research and sample evaluation from different manufacturers [10]. The continuous research on manufacturability allowed for significant decrease in defect densities, which increased yield and decreased costs [10]. Figure 1-4 shows the dramatic price drop since the first generation Schottky SiC diodes when compared to the last generation, due to all the advancements in manufacturing.

The first SiC power MOSFET device was proposed in 1992 by Palmour *et al.*

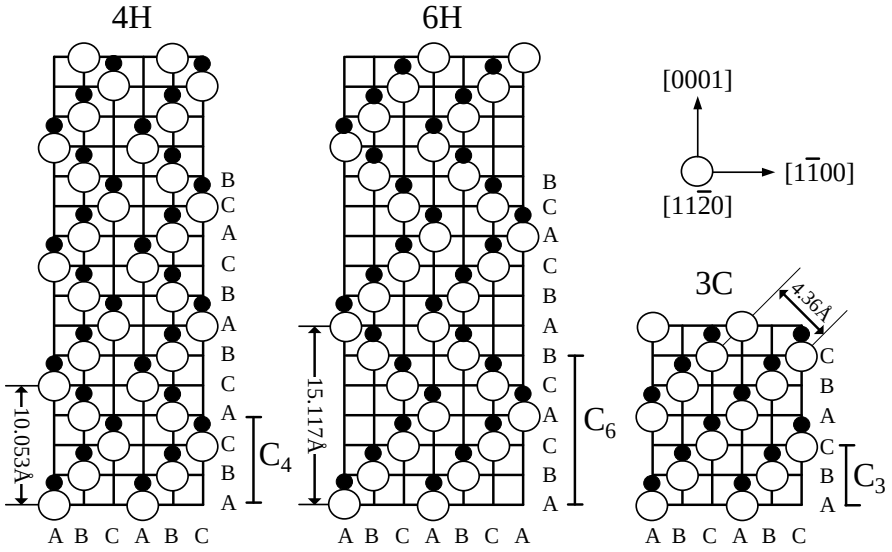

Figure 1-3 Stacking sequence for 4H-, 6H-, and 3C-SiC in the [1120] plane. The white circles represent Si atoms and the black ones represent C atoms [7]

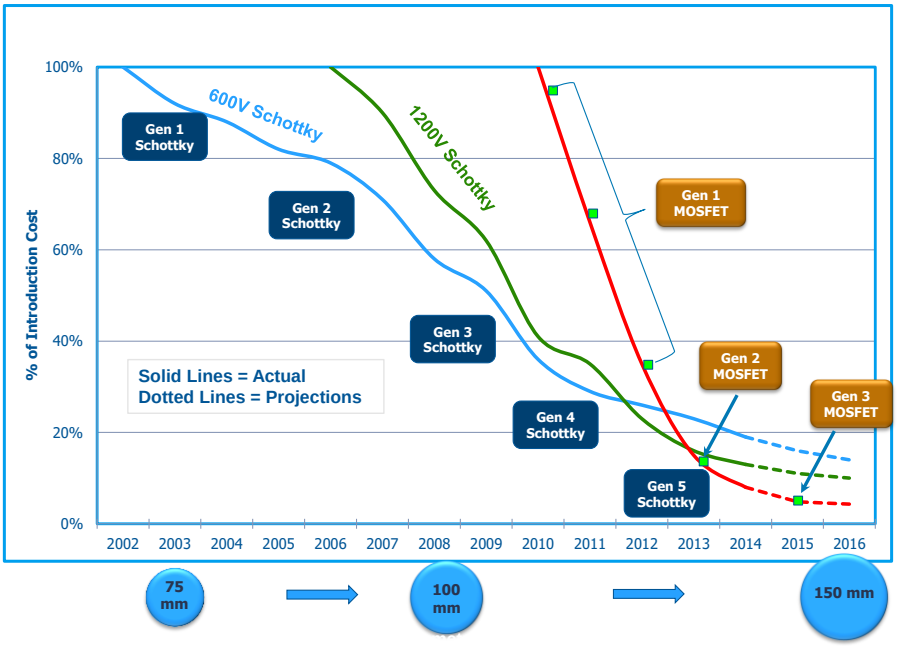

Figure 1-4 Cost reduction curves on a normalized basis of the SiC power device [20]

in 1992 as a UMOSFET structure [18]. Afterwards the SiC DMOSFET structure was presented by Shenoy *et al.* in 1996 [19]. The first commercially available SiC device came to market in 2001. The fifth iteration of the device is currently available on the market with a 5 times lower cost than the first generation, and increased performances [20]. As the technology advanced, more manufacturers started considering SiC as a suitable technology, and currently hundreds of diodes with ratings up to 3.3 kV are commercially available, with engineering samples reaching even 15 kV. The main producers of SiC power devices are Cree, Infineon and Rohm. This paved the way for other devices based on SiC technology, and in 2011 the first commercial SiC MOSFET was presented Cree [21]. Since then, Cree released two more iterations of their SiC MOSFET technology, each one with a lower price and better performances when compared to the previous one [20].

As mentioned earlier, while GaN shows good performances as a WBG material, its low thermal conductivity make it unsuitable for the high power devices market. Comparing the two polytypes of SiC materials available, 4H-SiC has better characteristics due to its higher carrier mobility and lower dopant ionization energy when compared to 6H-SiC, which make it a better semiconductor for use in high power high voltage devices. Because of its maturity on the market and the better performance, only 4H-SiC will be investigated in this work.

As the market matured, more manufacturers started developing unipolar devices (MOSFETs and JFETs) with SiC technology with power ratings similar to those Si-based devices. This encouraged power electronics and systems designer to consider transitioning from Si to SiC based devices in some applications. Initially, this has started as hybrid topologies and devices, where SiC diodes replaced the Si diodes in different application, allowing for an easy way to reduce the system losses. Evolution of the devices ratings, price reduction of the new technology and the better performances play a vital role in the speed of the transition from Si to SiC semiconductors. While current SiC devices have a higher cost when compared to similarly rated Si devices, the lower switching losses, lower threshold voltage, higher switching frequency and better thermal performance of the SiC allow it to offset the higher cost, making it a good solution in certain applications or topologies [4].

Figure 1-5 shows with red the integration of the available SiC devices (including published engineering samples) into the power semiconductor market [3], [10], [22]. Based on the ratings currently reported for SiC devices, the main suitable applications for it range from PV inverters, adjustable speed drives, pumps and hybrid/electric vehicles to high voltage valves, solid state transformers and high power traction. Moreover, commercial products based fully on SiC switching devices have come to the market, such as PV inverters SMA Sunny Tripower 20000TLHE-10 and REFUsol 020K-SCI [23], [24].

Although SiC semiconductors show superior electro-thermal capabilities when compared to their Si counterpart, and the room for improvement up to the theoretical material limits is big, their reliability needs to be asset in order for the market to accelerate the adoption of this new technology. As with any new technology, before being widely adopted and deployed in power electronics systems, the reliability and capability of the technology has to be asserted. Considering grid-connected large power converters where Si IGBTs are predominantly used and which SiC promises to be a competitive replacement, the expectations from power electronics systems designers expect at least a similar robustness and reliability. Failures in this case will have a big financial impact on the owner’s revenue and at the same time, might threaten the power system stability.

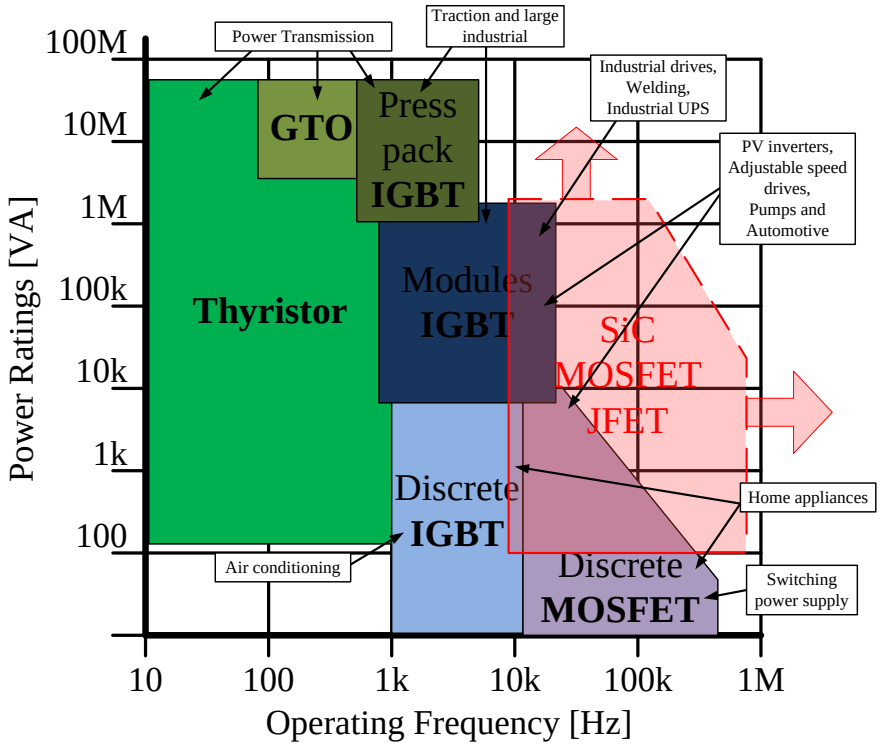

Figure 1-5 Integration of SiC-based devices on the Si-based power devices market [3], [4], [22]

1.4. Challenges of Research

As mentioned earlier, research on the next generation semiconductor material has been ongoing since the 1980's with special focus on SiC, which promises to be a suitable replacement of the Si semiconductor in the power devices as it has reached it material theoretical limits. In order for the new technology to be fully adopted and to increase its adoption rate, the new semiconductor materials have not only to show better electro-thermal capabilities, but also to show similar if not better reliability. In today's power semiconductor market, where power electronics systems and converters are expected to last for a long time, reliability is a key parameter, taken into consideration from the planning stage.

The availability of the power electronics converters is one of the most important aspects and it is mainly dictated by the components reliability and the maintenance schedule [25]. Considering the field of renewable energy, which at the present it is very dynamic and increasing rapidly, the power electronics in a system are responsible for a big part of the failures and unscheduled maintenance [26]-[28].

It was reported in [29] that, over a period of five years, in the case of large scale PV plants 37% of the unscheduled maintenance is due to the power electronics converters and this represented 59% of the total costs associated with the maintenance of a 3.5 MW PV plant.

During the entire lifetime of a power semiconductor device, it will encountered stressing transients, such as short-circuit and avalanche due to unclamped switching which force the device to operate outside its safe operating area (SOA) and might lead to early degradation and failure of the device [30]. Generally, devices meant for critical, grid connected applications are designed with robustness in mind, and should be able to sustain such transients until the control circuit detects it and takes protective actions or triggers the auxiliary protection circuit. It is expected that even though such transients occur, the device should be able to withstand them without any degradation in the device performance. This is highly relevant as it is expected that the SiC based devices should be able to withstand the same short-circuit transients as their Si counterparts, if not outperform them. This becomes challenging because, as mentioned earlier, due to the superior electro-thermal properties of SiC semiconductors, the chip sizes in the power devices for the same ratings are much smaller when compared to Si-based ones. Thus the entire short-circuit energy has to be supported by a much smaller volume, which in turn will result in higher energy per volume and higher temperature in the junction and the heat generated will be dissipated over a smaller area than in the case of Si.

In the 1 kV voltage range, studies have been performed on unipolar SiC devices in order to assess their roughness. This included experiments focusing on high thermal stressing of the devices which are associated with short-circuit events [31]-[34], or evaluation of the device behavior during short-circuit transients [35]-[38].

Single crystal SiC wafers have been fabricates since the early 90’s and with this, different researchers across the world have started focusing on manufacturing low defect density epitaxial materials for high voltage power devices based on SiC. With improvements in the manufacturing process, as a proof of concept for the next generation high voltage power semiconductor device, in 2003, the first 10 kV 4H-SiC power DMOSFET was presented Cree Inc. [39].

Despite the remarkable advancement achieved in the past 15 years in the SiC power devices technology, the development of high voltage SiC devices with ratings above 10 kV is still in an early stage, as most focus is on the lower voltage levels where the devices can directly replace Si power semiconductors. The power switching devices market is mainly defining and shaping the required behavior of the devices, and because devices with ratings over 10 kV are still novel and it is not possible to directly compare their performance with similar Si device which they

might replace. This has less advancements in this field, and the device optimization was not done as well as in the lower voltage range. Thus such devices are mainly optimized for switching performances and low conductions losses but their SOA has not yet been fully defined, and their operation during extreme conditions has not yet been studied or fully understood.

Due to the novelty of the device, and limited researched focused on them, no detailed studies have investigated the full behavior of such devices, or on the test setups which could take advantage of the WBG properties of the semiconductor material. While some studies have investigated the switching behavior of the device, the circuits used for such investigation were not optimized to take advantage of the fast switching capability of the 10 kV 10 A 4H-SiC MOSFET, were only focused on a particular switching characteristics or were done from a theoretical point of view [40]-[44].

At the same time, only the lower voltage SiC 4H-MOSFETs short-circuit capabilities were investigated, with no information regarding the higher voltage devices being available. The lack of these studies makes implementation of such devices into power converters unlikely, as short-circuit capabilities and degradation are key parameters when designing such circuits.

1.5. Objective

The integration of 10 kV 10 A 4H-SiC MOSFETs into the power electronics market, currently dominated by slower Si IGBTs is strongly dependent on their reliability, especially during transients.

Therefore, in order for such device to be considered, and to accelerate their market adoption, the emerging challenges that have to be overcome are summarized as:

1. What is the device behavior over a wide range of temperatures and loading levels?

2. What is the device minimum short-circuit withstand time capability?

3. How and why is the device degrading during short-circuit transients?

Based on the above mentioned research questions, the main objectives of the work have been summarized as:

1. Development of a unified test setup which could test 10 kV 10 A 4H-SiC MOSFETs during all the expected dynamic transients, such as: switching,

short-circuit and unclamped inductive switching, over a wide range of temperatures, drain currents, drain-source voltages and gate voltages.

2. Investigation of device switching behavior and generation of switching losses maps over a wide range of parameters, to allow for an easier study of the device characteristics.

3. Identification of the peak short-circuit current of 10 kV 10 A 4H-SiC MOSFET and the minimum short-circuit withstand time capability.

4. Investigation of the behavior during short-circuit of the 10 kV 10 A 4H-SiC MOSFET and current shaping phenomena.

5. Investigation of the possible degradation mechanisms in 10 kV 10 A 4H-SiC MOSFETs during short-circuit stressing.

1.6. List of publications

The work performed during the PhD period has been presented in the following publications:

Journal paper:

P. I. **E. P. Eni**; S. Beczkowski; S. Munk-Nielsen; T. Kerekes; R. Teodorescu; R. R. Juluri; B. Julsgaard; E. VanBrunt; B. Hull; S. Sabri; D. Grider and C. Uhrenfeldt**,** "Short-Circuit Degradation of 10 kV 10 A SiC MOSFET," in IEEE Transactions on Power Electronics , *[in publication]*

Conference papers:

P. II. C. Sintamarean; **E. P. Eni**; F. Blaabjerg; R. Teodorescu and H. Wang, "Wide-band gap devices in PV systems - opportunities and challenges," in 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), Hiroshima, 2014, pp. 1912-1919.

P. III. **E. P. Eni;** T. Kerekes; C. Uhrenfeldt; R. Teodorescu and S. Munk-Nielsen, "Design of low impedance busbar for 10 kV, 100A 4H-SiC MOSFET short-circuit tester using axial capacitors," in 2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Aachen, 2015, pp. 1-5.

P. IV. **E. P. Eni**; B. I. Incau; T. Kerekes; R. Teodorescu and S. Munk-Nielsen, "Characterisation of 10 kV 10 A SiC MOSFET," in 2015 Intl Aegean Conference on Electrical Machines & Power Electronics (ACEMP), 2015 Intl Conference on Optimization of Electrical & Electronic Equipment

(OPTIM) & 2015 Intl Symposium on Advanced Electromechanical Motion Systems (ELECTROMOTION), Side, 2015, pp. 675-680.

P. V. **E. P. Eni**; S. Bęczkowski; S. Munk-Nielsen; T. Kerekes and R. Teodorescu, "Short-circuit characterization of 10 kV 10A 4H-SiC MOSFET," in 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 974-978

P. VI. S. Bęczkowski; H. Li; C. Uhrenfeldt; **E. P. Eni** and S. Munk-Nielsen, "10kV SiC MOSFET split output power module," in 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), Geneva, 2015, pp. 1-7.

P. VII. H. Li; S. Munk-Nielsen; S. Bęczkowski; X. Wang and **E. P. Eni**, "Effects of auxiliary source connections in multichip power module," in 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 3101-3106.

1.7. Outline of dissertation

Chapter 1 - Introduction – present the background and motivation of the research, highlighting the influence of SiC semiconductor on the power electronics market and evolution of SiC. In the end the main objectives and outline of the thesis are presented.

Chapter 2 - SiC Power Devices – presents a theoretical investigation of SiC and Si unipolar devices. SiC theoretical limits in terms of on-state resistance, switching frequency, dimensions, doping and parameters variation are compared against Si. In the last part, different figures of merits for the two semiconductor materials are compared.

Chapter 3 - Characterization of 10kV 4H-SiC MOSFET – starts with an introduction into power MOSFETs and their characteristics, parasitic components and switching behavior. A state-of-the-art and evolution of 4H-SiC MOSFETs is then presented, up to current times. Afterwards, the design and performance of a custom designed, unified testing, low inductance test setup for 10 kV 4H-SiC MOSFETs are presented. In the last part of the chapter, the static and dynamic characteristics of the 10 kV 10 A 4H-SiC MOSFET are studied over a wide range of temperatures, voltages and currents.

Chapter 4 - Short-Circuit Analysis of 10kV 4H-SiC MOSFETs – investigates the minimum short-circuit withstand time capabilities and behavior of the 10 kV 10 A 4H-SiC MOSFET. As the device has never been studied during such events, a state-of-the-art of short-circuit behavior and degradation of lower voltage 4H-SiC MOSFETs has been gathered. The lower voltage device are based on the same

manufacturing technology and internal structure, and while not necessarily directly scalable, the observation obtained from such devices could be replicable and insightful for the 10 kV 4H-SiC MOSFET. Because of the lack of benchmarks, the minimum short-circuit withstand time capability for the device was obtained in a conservative way, with the device being stressed and degraded long before it failed. Intrigued by the failure, the degradation observed in the short-circuit peak current was also investigated in another study, with the aim to observe variations in the device electrical parameters and structure. 1D thermal simulations were also used to confirm the temperatures during short-circuit experienced by the device.

Chapter 5 - Conclusion and future work – presents the final conclusions of the research done in the thesis and summarized the main contributions of the works, discussing some future possible works which could improve on the findings of the thesis.

Chapter 2.
SiC Power Devices

In this chapter the theoretical capabilities of SiC power devices is compared to that of Si in order to better highlight the advantages of the new WBG semiconductor material and to emphasize the trend and advantages of switching from Si to SiC in power electronics converters.

2.1. Introduction

SiC based power devices are still in the early stage of development when compared to Si semiconductors. Si has been the semiconductor of choice for high power devices for the past decade and the continuous research focused on improving its performance in power semiconductor devices have allowed the power electronics to exploit the material up to its limits, or in case of specific unipolar devices structures, such as super junction MOSFETs, even surpass them. On the other hand, SiC has getting attention for a much shorter period of time, as Si limits were starting to get reached. The research on SiC, being on the beginning has mostly focused on making SiC unipolar devices as reliable and competitive as possible, and the material limits are still not yet fully reached.

Because of this, the most correct way of comparing the two technologies is from a theoretical material point of view, in order to highlight the performances of the two devices from a similar point of view, as research on SiC is still in its infancy, compared to Si.

2.2. Theoretical Specific On-State Resistance

One of the main benefits of WBG based power devices when compared to Si ones comes from lower specific on-state resistance of the drift region for a similar blocking voltage. The voltage limit which can be safely supported across a drift region is decided by the beginning of the impact ionization as the electric field in the region increases. The limit of the electric field at which impact ionization starts to occur is specific to each semiconductor and is termed as the critical electric field (E_C) of the material. The edge termination of the chip plays an important role in influencing the electric field in the device, thus its design can influence the maximum voltage the device can sustain. Although the electric field in a power device is also influenced by the dimensions and geometry of the die, the parallel plane analysis is sufficient to highlight the advantages of WBG semiconductors.

Considering an abrupt asymmetric 4H-SiC device, the critical electric field as a function of doping concertation can be expressed as [3]:

$$E_c(4H-SiC) = 3.3\times10^4 N_D^{1/8} \tag{2.1}$$

where N_D is the doping concertation in the uniformly doped 4H-SiC N-region. The critical field of 4H-SiC with a doping concertation of 1017 cm-3 is 3.5MV/cm, almost 6 times bigger than in Si as show in Table 1-1[6].

Assuming a non-punch through P^+/N junction as shown in Figure 2-1, where the P^+ region is highly doped, the electric field which can be supported by the region is neglectable. If the junction is reversed biased, the depletion region will form in the N-region as the electric field needed to support the bias voltage increases. The maximum electric field of the junction can then be expressed as [3]:

$$E_{max} = \sqrt{\frac{2qN_DV_a}{\varepsilon_s}} \tag{2.2}$$

where ε_s is the semiconductor dielectric constant, q is the electron charge and V_a is the applied reverse bias. Equation (2.2) shows that as the applied bias increases, so does the maximum electric field and at a certain point impact ionization might start to occur and avalanche breakdown might occur. By rearranging equation (2.2) the

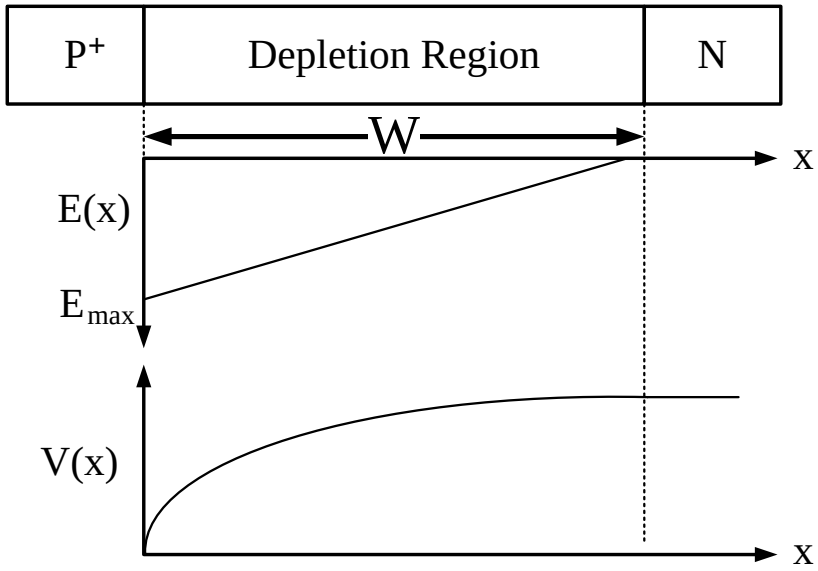

Figure 2-1 Electric field and potential distribution for an abrupt parallel-plane P^+/N junction [3]

breakdown voltage (*BV*) of the structure can be extracted as:

$$BV = \frac{\varepsilon_s E_c^2}{2qN_D} \tag{2.3}$$

Thus, the doping concentration of the N-region required to support this breakdown voltage is given by:

$$N_D = \frac{\varepsilon_s E_c^2}{2qBV} \tag{2.4}$$

The thickness of the depletion region, *W*, can be expressed in relation to the applied reverse bias as [9]:

$$W = \sqrt{\frac{2\varepsilon_s V_a}{qN_D}} \tag{2.5}$$

This represents the minimum thickness required for the drift layer, W_D, in order to support a given avalanche voltage. Inserting equation (2.3) into equation (2.5), the minimum thickness of the drift layer can be expressed as:

$$W_D = \sqrt{\frac{2\varepsilon_s BV}{qN_D}} = \frac{2BV}{E_C} \tag{2.6}$$

The ideal specific on-state resistance of the drift region, if charge coupling is ignored, can be described as [3]:

$$R_{on,sp} = \frac{4BV^2}{\varepsilon_s \mu_n E_c^3} \tag{2.7}$$

where μ_n is the electron mobility in the drift layer.

The breakdown voltage can be written as a function of doping concentration as of the N-region using Baliga's power law [45], as [1]:

$$BV_{pp}(Si) = 4.45 \times 10^{13} N_D^{-3/4} \tag{2.8}$$

for Si, and for SiC as [3]:

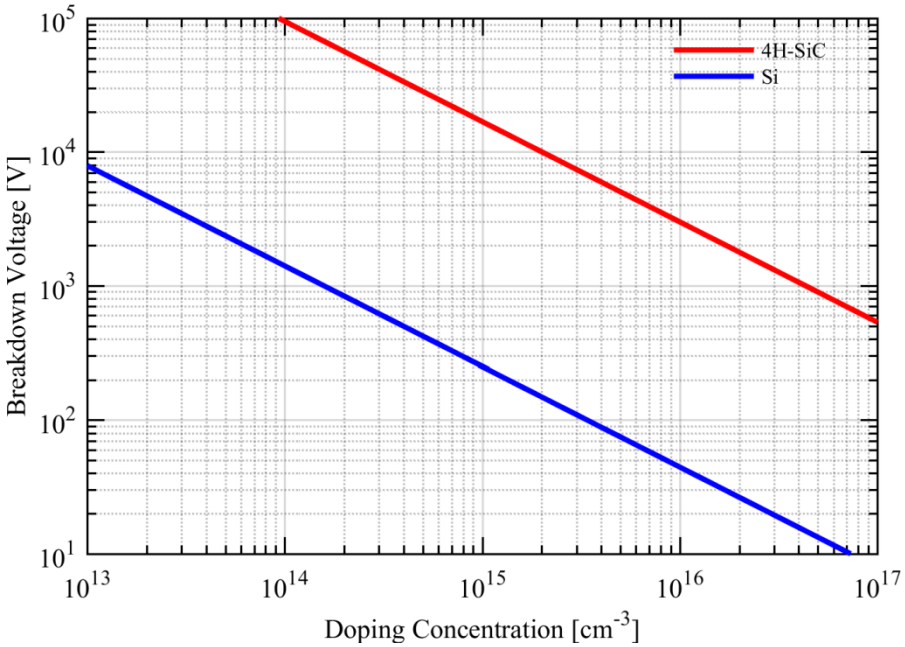

Figure 2-2 Breakdown Voltage for Abrupt Parallel-Plane Junctions in Si and 4H-SiC as a function of doping concentration

$$BV_{pp}(4H-SiC) = 3\times10^{15} N_D^{-3/4} \tag{2.9}$$

The breakdown voltage as a function of doping concentration is plotted in Figure 2-2 for both Si and 4H-SiC. The graph clearly shows that 4H-SiC devices can support a much higher breakdown voltage for the same doping concentration when compared to Si devices. For a similar material doping concentration, 4H-SiC devices have a blocking voltage 60 times higher than that of SiC. Or, a much higher doping concentration can be used for the drift region of the 4H-SiC devices for a given device breakdown voltage when compared to Si. For a similar desired breakdown voltage, the doping concentration of the 4H-SiC devices when compared to Si devices can be 275 times larger.

Using the same power law equation, the width of the depletion layer at breakdown can be extracted for both Si and SiC as a function of doping concentration as [1], [3]:

$$W_{pp}(Si) = 2.404\times10^{10} N_D^{-7/8} \tag{2.10}$$

$$W_{pp}(4H-SiC) = 1.82\times10^{11} N_D^{-7/8} \tag{2.11}$$

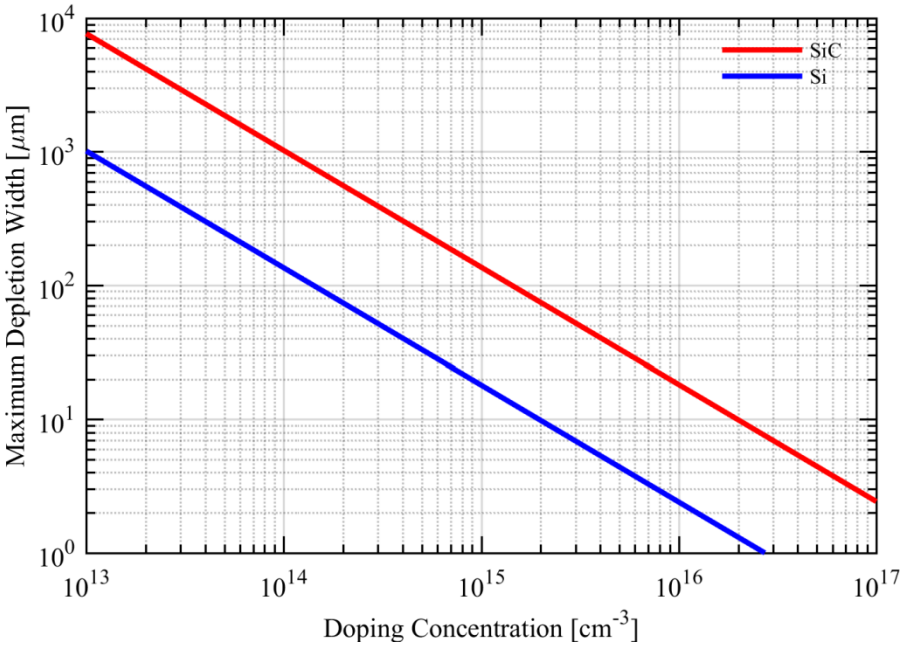

Figure 2-3 Maximum Depletion Width at Breakdown in Si and 4H-SiC

Figure 2-3 shows depletion layer width at breakdown voltage of SiC and Si for as a function of doping concentration. 4H-SiC maximum depletion width in the N-region is 7.6 times bigger than that of the Si material for a similar doping concentration. This would allow 4H-SiC to support a larger electric field when compared to Si. The main advantage which can be observed here is that the depletion width of the 4H-SiC devices is much smaller than for Si-based devices for a given breakdown voltage. The smaller depletion layer and much higher doping levels used in 4H-SiC devices will give a big reduction in the device specific on-state resistance of the drift region compared to Si-based devices.

In order to compute the specific on-state resistance, it is required to consider the variation of the mobility and electric field with the doping concentration. Since the doping varies with the breakdown voltage. An approach to this would to calculate the doping concentration required for a certain breakdown voltage and, based on that, to calculate afterwards the mobility and depletion width. Afterwards, the specific on-resistance, $R_{on,sp}$, of the ideal non-punch through drift region is described as [3]:

$$R_{on,sp} = \frac{W_D}{q\mu_n N_D} \tag{2.12}$$

The theoretical specific on-resistance at room temperature of unipolar Si-based devices (which follows the results from the equation above) can also be written as [46]:

$$R_{on,sp}(Si) = 5.93 \times 10^{-9} BV^{2.5} \tag{2.13}$$

The theoretical on-state resistance of the drift regions for 4H-SiC and Si is calculated using equation (2.12) and compared in Figure 2-4. The ratio between the theoretical on-state resistance of 4H-SiC based devices to that of Si based devices is around 1000 at 100V and goes up to 2600 for breakdown voltages of 10kV.

2.3. Theoretical Maximum Switching Frequency of Unipolar Devices

One of the main key features of 4H-SiC, inherited from its wide bandgap properties are the material capabilities for fast switching. This is highly attractive because, generally, increasing the switching frequency allows for a decrease in size and weight of the power converters and an increase in power density. This is mainly related to a reduction in the converter output filters, reduction in converter complexity by reducing the number of level and furthermore a reduction in cost,

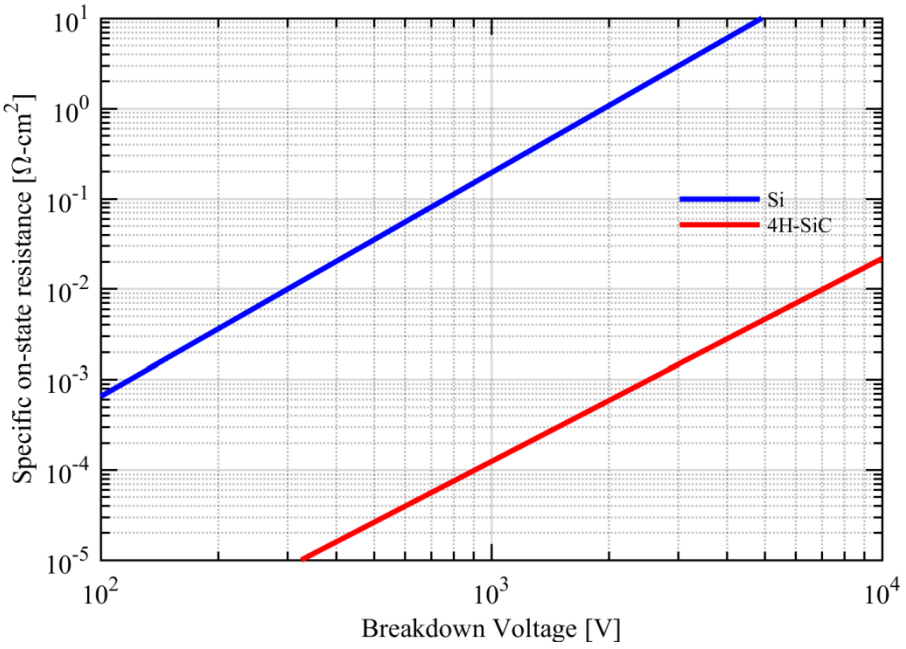

Figure 2-4 Specific On-State Resistance of the Drift Region as a Function of Voltage on 4H-SiC and Si

depending on the parameters of the converter which are optimized [4].

The switching losses of unipolar devices can be described by observing their gate charge characteristics, and is similar for all unipolar devices, independent of their structure (MOSFET, JFET etc.) [47].

The total power losses of a unipolar power device can be described as [47]:

$$P_{loss} = I_{rms}^2 R_{DS,on} + V_{DS} I_D f \left(t_r + t_f\right) \frac{1 + E_{on}/E_{off}}{2} \tag{2.14}$$

where I_{rms} is the RMS current of the converter, $R_{DS,on}$ is the on-state resistance of the device, V_{DS} is the applied drain-source voltage, f is the swithicng frequency, t_r is the drain current rise time, t_f is the drain-source voltage fall time and E_{on} and E_{off} are the turn-on and turn-off energies. The first part of equation (2.14) describes the unipolar device conduction losses, while the second term describes the switching losses.

t_f can be expressed as [47]:

$$t_f = \frac{Q_{gd}}{i_{g,av}} \tag{2.15}$$

where Q_{gd} is the charge of the gate-drain capacitance, C_{GD}, integrated over the voltage supported by the device during its transition from V_{DS} to the small voltage drop during conduction as the devices shifts from blocking to conduction state, or vice versa [47]. $i_{g,av}$ is the average gate current of the device. Q_{gd} is mainly defined by the depletion layer charge under the gate which is formed in order to support V_{DS}. Based on Gauss's law, the specific gate-drain charge, $Q_{gd,sp}$ can be expressed as [47]:

$$Q_{gd,sp} = k\varepsilon_s E_{DS} = k\sqrt{\frac{V_{DS}}{BV}}\varepsilon_s E_c \tag{2.16}$$

where E_{DS} is the peak electric field required for the device to support V_{DS} and k (<1) represents a device design parameter which defines the ratio of the gate-drain overlap area compared to the entire chip area.

The assumption made in [47] by *Huang et all.* that the turn-on and turn-off losses are equal, thus the last part of the switching losses can be assumed to be one is not correct, as it was already observed in [48] where the turn-on losses are up to 6

times higher than the turn-off losses, even when a low gate-source voltage bias is used.

Considering that the switching losses are dominated by the charging and discharging of the Miller charge, and the losses accumulated during the t_r period are neglectable compared to the ones in the t_f period, equation (2.14) can be simplified and expressed as a function of the area:

$$P_{loss} = \frac{I_{rms}^2 R_{on,sp}}{A} + \frac{V_{DS} I_D f Q_{GD,sp} A}{i_{g,av}} \frac{1 + E_{on}/E_{off}}{2} \tag{2.17}$$

From equation (2.17) it can be observed that the losses are dependent on the device dimensions. As expected, if the device area is increased, the current and $R_{on,sp}$ will be distributed over a larger area, thus decreasing the conduction losses, but on the other hand, the $Q_{gd,sp}$ is directly proportional to the device area, thus increasing the switching losses. The minimum power losses can be obtained when $dP_{loss}/dA=0$. Equation (2.17) can be rearranged then in order to obtain to satisfy the minimum power losses criteria:

$$\frac{V_{DS} I_D f Q_{gd,sp}}{i_{g,av}} = \frac{I_{rms}^2 R_{on,sp}}{A^2} \tag{2.18}$$

Thus the optimal area of the device, A_{opt}, in order to obtain the minimum power losses is described as:

$$A_{opt} = \frac{I_{rms}}{\sqrt{\frac{1 + E_{on}/E_{off}}{2} \frac{V_{DS} I_D f}{i_{g,av}}}} \sqrt{\frac{R_{on,sp}}{Q_{gd,sp}}} \tag{2.19}$$

Substituting equation (2.19) into equation (2.17), the minimum power losses can be obtained as:

$$P_{loss,min} = 2 I_{rms} \sqrt{\frac{1 + E_{on}/E_{off}}{2} \frac{V_{DS} I_D f}{i_{g,av}} R_{on,sp} Q_{gd,sp}} \tag{2.20}$$

Combining equation (2.7) and equation (2.16), one can obtain:

$$R_{on,sp} Q_{gd,sp} = \frac{4kBV\sqrt{BV \cdot V_{DS}}}{\mu_n E_c^3} \tag{2.21}$$

Thus, introduction equation (2.21) into equation (2.20) the minimum power loss of the unipolar device becomes:

$$P_{loss,min} = \frac{4I_{rms}\left(V_{DS}BV\right)^{\frac{3}{4}}\sqrt{k\frac{1+E_{on}/E_{off}}{2}\frac{I_D f}{i_{g,av}}}}{E_c\sqrt{\mu_n}} \tag{2.22}$$

From equation (2.22), the maximum operating frequency of unipolar devices as a function of device ratings and dimensions can be extracted as:

$$f_{max} = \frac{P_{loss}^2 E_c^2 i_{g,av}\mu_n}{16I_{rms}I_D^2\left(V_{DS}BV\right)^{3/2}k\frac{1+E_{on}/E_{off}}{2}} \tag{2.23}$$

where P_{loss} is the total losses the packaging of the device allows to be dissipated. As it can be seen, the maximum frequency is directly proportional to P_{loss}^2, which means that any improvement in the power density of the packages will allow for a higher operating frequency.

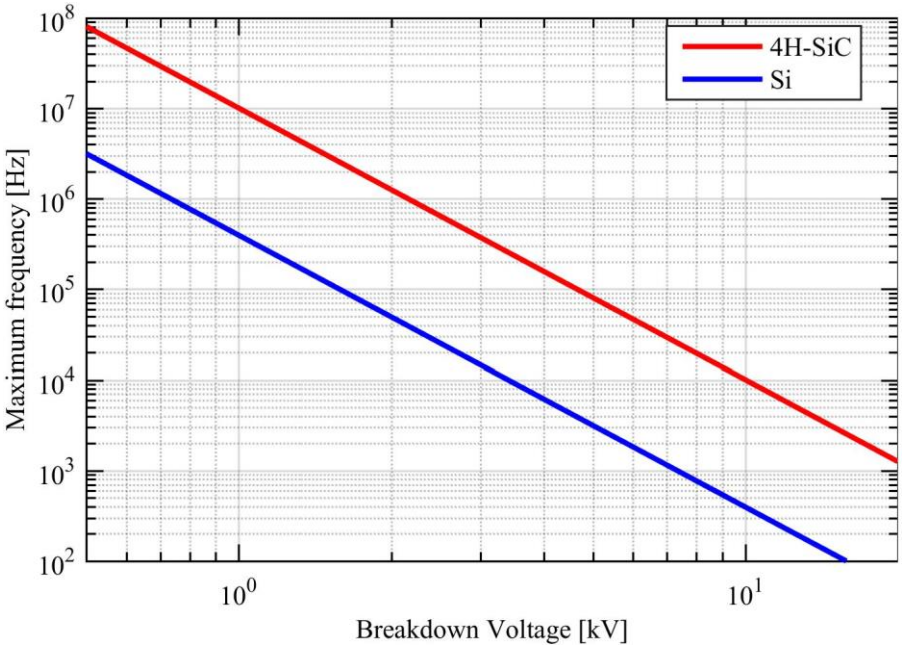

Figure 2-5 Maximum theoretical swithcing frequency of unipolar Si and 4H-SiC devices as a function of the blocking voltage assuming usage in identical circuits

As an example, assuming a Si and a 4H-SiC MOSFETs with a chip active area size of 100mm^2, k=0.5, a turn-on losses to turn-off losses ratio of 4, that operate in a converter with a V_{DS} nominal voltage of half of the BV, a nominal current I_D=10A, an average gate current $i_{g,av}$=1A with a total power losses of 300W and a junction temperature of 175°C, their maximum frequency as a function of their blocking voltage is plotted in Figure 2-5. Based on the above assumption, the a 4H-SiC unipolar, device can have a maximum theoretical switching frequency more than 25 times higher than a Si unipolar device with an identical breakdown voltage used in a similar circuit with identical power ratings. This is related only to the better material properties of the WBG material. For a 10kV 4H-SiC unipolar device, the maximum theoretical switching frequency is approximately 10 kHz.

2.4. Figure of Merits

Figure of merits (FOMs) have been developed over the years in order to quantify the performance of semiconductor power device based on the semiconductor material properties. For power unipolar devices, there are two main categories of FOMs, the first category uses only the material properties in order to highlight the impact of better material properties of the device, while the second category take into consideration different device specific characteristics and behavior. The first category is the most used one as it allows for the semiconductor material to be directly compared, thus giving a theoretical comparison. Because research on most WBG materials has not been as intensive as on Si devices, the challenges of developing WBG devices with those materials have not been fully overpassed and solved when compared to Si based device. The evolution of the power semiconductor market and the reach of Si theoretical limit is speeding the research in those fields, allowing for large improvements in the WBG based devices manufacturing and closing the gap between the commercially available devices and the theoretical limits at a high pace [22], [49]. The second category takes into consideration device specific parameters thus also showing the limitations of the design and manufacturing process. While they might be more relevant to a certain extent, they require a lot of knowledge regarding the device manufacturing process and the physical dimensions of the semiconductor chip which are not easily available. Also WBG devices are still in their early stages, thus research on their manufacturability can yield larger improvements on WBG devices performance, when compared to Si which has been the main research topic in the power semiconductor industry for the past decades.

In 1965, Johnson derived a figure of merits for semiconductor materials used in high frequency field-effect transistors where the product of the electron saturation velocity and the electric breakdown field is assumed to be the limiting factor [50]:

Table 2-1 FOMs for semiconductor materials [53]-[55]

Material	Si	4H-SiC	GaN
JFOM	$9.09 \cdot 10^{23}$	$3.64 \cdot 10^{26}$	$6.87 \cdot 10^{26}$
KFOM	$1.39 \cdot 10^{3}$	$6.46 \cdot 10^{3}$	$3.85 \cdot 10^{3}$
BFOM	$4.26 \cdot 10^{20}$	$1.83 \cdot 10^{23}$	$2.88 \cdot 10^{23}$
BHFFOM	$1.22 \cdot 10^{14}$	$6.3 \cdot 10^{15}$	$9.8 \cdot 10^{15}$

$$\mathrm{JFOM} = \frac{E_c v_s}{2\pi} \tag{2.24}$$

In 1972, Keyes proposed a figure of merit aimed at defining a thermal limitation to the switching behavior of transistors [51]:

$$\mathrm{KFOM} = \lambda \left[\frac{c \cdot v_s}{4\pi\varepsilon_s} \right]^{1/2} \tag{2.25}$$

where c is the velocity of light.

Both JFOM and KFOM are not relevant for high power switching application as they are limited to specific conditions. JFOM is only applicable in the case of low voltage transistors while KFOM is mainly usable in the case of integrated transistor. Despite this, they can still be used when comparing different materials as they take into consideration only the material properties of unipolar devices.

In 1982, Baliga derived a figure of merit as [52]:

$$\mathrm{BFOM} = \varepsilon \mu E_G^3 \tag{2.26}$$

which quantifies the material parameters mobility and bandgap in order to minimize power unipolar devices conduction losses. This assumes that almost all the device losses are associated with the large current passing through the device on-state resistance during conduction, making it suitable only for devices operating at low switching frequencies.

In 1989, Baliga presented another figure of merit aimed to consider the switching losses of power unipolar devices resulted from the charging and discharging of the device's input capacitance during each switching cycle [53]:

$$\mathrm{BHFFOM} = \mu E_c^2 \left(\frac{V_{GS}^{1/2}}{2} BV^{1.5} \right) \tag{2.27}$$

In order to keep BHFFOM only related to the material properties and not device dependent, the part of the equation in the parentheses is generally dropped when using BHFFOM to compare different semiconductor materials for unipolar power devices.

Table 2-1 shows the FOMs for different semiconductor materials. It can be observed that from a theoretical point of view, due to its superior material properties, 4H-SiC devices promises to offer vast improvement when compared to Si ones. In order to highlight the advantages better and help the reader, the values in Table 2-1 have been normalized to Si and are shown in Table 2-2.

Table 2-2 Normalized values of FOMs for semiconductor materials [53]-[55]

Material	Si	4H-SiC	GaN
JFOM	1	400	756.25
KFOM	1	4.66	2.78
BFOM	1	429.88	674.98
BHFFOM	1	51.85	80.67

2.5. Summary

In this chapter, several theoretical material limits of Si and SiC based unipolar devices, such as theoretical specific on-state resistance, have been investigated and compared among the two semiconductor materials. It was showed that for a similar breakdown voltage a SiC based unipolar power device can have a 275 times larger doping concentration than a Si based unipolar device. This higher doping concentration would allow for a up to 7.5 times smaller drift layer thickness in the SiC based unipolar device when compared to Si counterpart with a similar voltage rating. The theoretical on-state resistance of SiC based unipolar devices was shown to be up to 2000 times smaller than that of Si based ones if the same breakdown voltage is desired.

The theoretical maximum frequency of a SiC power MOSFET was also compared against a Si based power MOSFET with similar voltage ratings in an identical circuit and assuming similar power losses. The SiC based device outperformed the Si one, showing a theoretical switching capability more than 25 times larger than the Si based device.

The two semiconductor materials were also compared using different figures of merits, proving that as a semiconductor SiC is a better material for unipolar power devices.

Due to all of the above mentioned advantages make SiC based unipolar devices the best candidate to replace Si based power devices for voltage ratings above 1kV. At the same time it allows unipolar devices to achieve voltage rating which were previously suitable only for Si bipolar transistors and even exceeding them.

Chapter 3.
Characterization of 10kV 4H-SiC MOSFET

This chapter discusses the power MOSFET and history of SiC power MOSFETs and then makes an analysis of the first generation 10kV 10A 4H-SiC MOSFET from both the dynamic and static perspective. The switching losses of the device are investigated in order to get a clear understanding of its behaviour during operation.

3.1. Introduction to Power MOSFETs

The power MOSFET was developed in the 1970's and was the first commercially viable Si-based unipolar switching device [56]. It revolutionized the market, which at that time was dominated by slow, generally current driven power semiconductors. It had an innovative design which gave several advantages. Its high input impedance gate structure allowed for a cheaper and simplified driving circuit while maintaining good control of the device. Since it was a unipolar, majority carrier device, it allowed for much faster switching frequencies compared to bipolar minority carrier devices. The device allowed for a large SOA, compared to bipolar devices of the time, where larger currents and voltages could be supported for short periods of time without destruction.

The initial structure design has been improved and modified depending on the feature which needed to be enhanced, giving birth to different structures such as: CoolMOS HEXMOS, UMOSFET, etc [3]. The purpose of this chapter is to only focus on the basic power MOSFET structure which is also termed DMOSET, as a consequence of the cost-effective way of constructing the channel in these devices: by the double diffusion process.

Figure 3-1 shows the cross section view of a simplified n-channel power MOSFET cell. The source regions, P-base and N^+, are formed by ion implantations though a common slot given by the edge of the gate polysilicon electrode. After each implantation cycle, a drive-in process moves the P-N junction laterally under the gate. The P-base region is pushed deeper under the gate than the N^+ region. The area under the gate electrode between the N^+/P-base junction and the P-base/N^--drift junction defines the source channel region [3]. This allows for the channel length to be controlled up to μm dimensions without complicated and expensive, high resolution lithography.

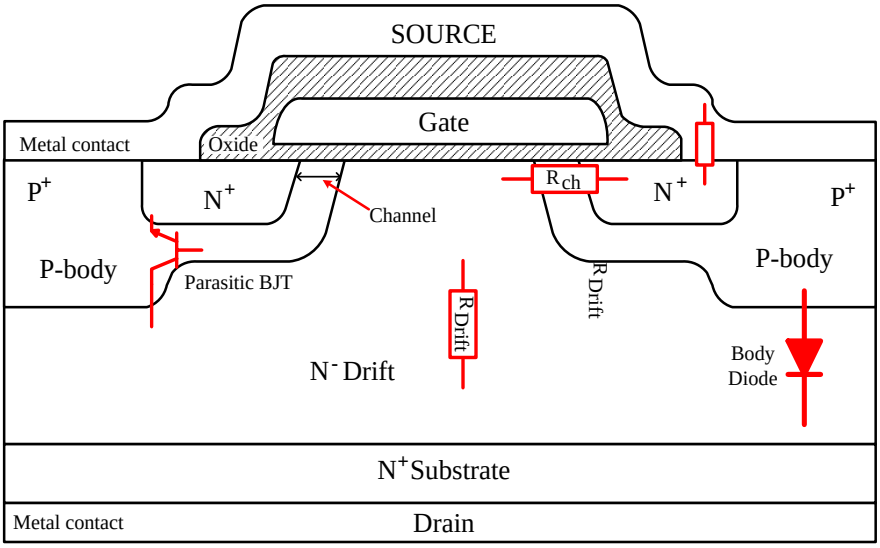

Figure 3-1 Cross section view of simplified n-channel power MOSFET cell structure [9]

When employed in high voltage application, the drift region resistance becomes dominant in Si-based MOSFETs, leading to large voltage drops for high current applications. For devices with large breakdown voltage ratings, this resistance is in the range of 10^{-2} $\Omega \cdot cm^2$, as shown in Figure 2-4. This has discouraged the usage of MOSFETs in applications above 200 V, instead being replaced by Insulated Gate Bipolar Transistors (IGBTs) in higher voltage power applications. The new Si MOSFETs technologies (UMOSFET, CoolMOS, etc) have allowed for Si MOSFETs to be used in application with device ratings up to 900V [57], but their drift region resistance is still considerably large leading to higher conduction losses when compared to Si IBGTs, thus making them suitable only for applications requiring high frequency switching.

3.1.1. STATIC CHARACTERISTICS

Considering the simplified n-channel power MOSFET from Figure 3-1, it has three main operation modes: linear or ohmic mode, saturation mode and cutoff or blocking mode as shown in Figure 3-2.

Ignoring sub-threshold conduction and the weak-inversion current, under ideal circumstances, when the gate-source bias voltage, V_{GS}, is smaller than the MOSFET threshold voltage, V_{th}, the device is assumed to be turned off and can support a large drain-source voltage, V_{DS}, across the junction formed by the P-body/N^- drift region. The maximum drain-source voltage has to be within the device design limits, thus

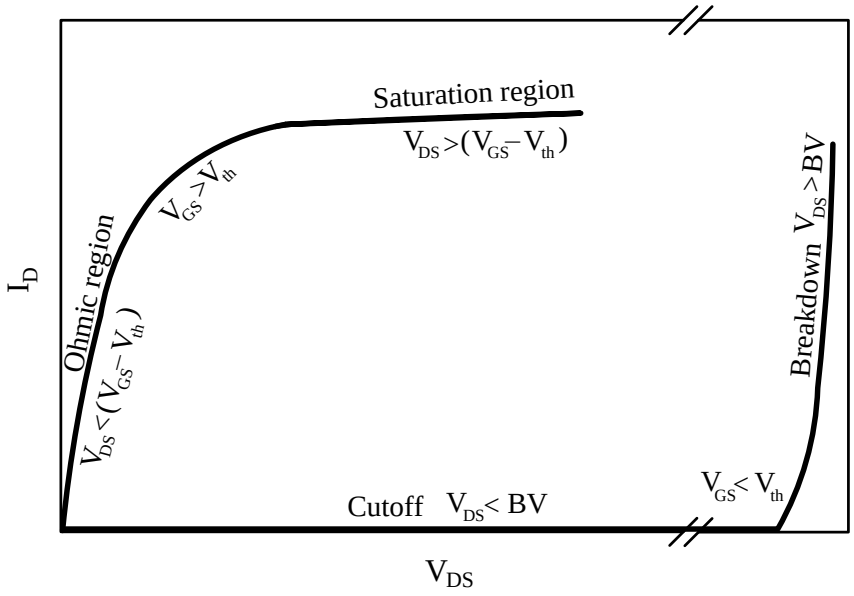

Figure 3-2 Typical output characteristic of basic n-channel Si MOSFET(based on [9])

smaller than the breakdown voltage of the junction formed by the P-body/N^- drift region, or the device will go into avalanche breakdown and the device could get destroyed. The lowest curve in Figure 3-2 shows the cutoff operation mode.

As a gate-source voltage larger than the threshold voltage is applied, an inversion layer channel appears under the gate oxide of the power MOSFET, at the interface between the p-body and the oxide, and currents starts flowing between the drain and the source of the device. The device will enter the ohmic regime while the drain-source voltage is smaller than the applied gate-source voltage minus the device threshold voltage. In the linear region the device behaves as a resistor, and the drain current is controlled by the applied gate-source and drain-source voltages. This resistance dictates the losses of the device during conduction and as a consequence, the junction temperature. The resistance mainly varies with the channel resistance, drift region resistance and JFET resistance. If the drain-source voltage is increased above the applied gate-source voltage minus the device threshold voltage, the device will go into saturation mode. During this mode the device on-state resistance will increase as a consequence of the channel getting pinched off and an increase in drain-source voltage will have almost no influence on the drain current.

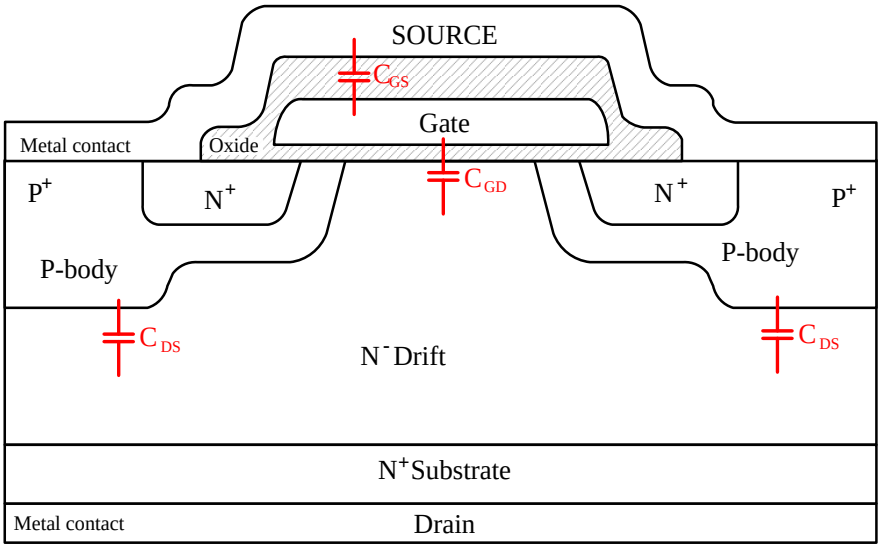

Figure 3-3 Parasitic capacitances of a simplified n-channel power MOSFET cell [9]

3.1.2. PARASITIC CAPACITANCES

Figure 3-3 shows the internal parasitic capacitances present in a power MOSFET. The gate-source capacitance, C_{GS}, is formed by the region of the polysilicon gate which overlaps the source and the metal source contact. This capacitance is mainly considered constant as the N^+ and P body regions are highly doped. As the gate polysilicon overlaps the drift region (from which it is separated by the gate oxide) it forms with the silicon underneath (in the JFET region) a part of the gate-drain capacitance, C_{GD}. The other part of C_{GD} is dependent on the space-charge zone which forms when the device in not conducting. Therefore it shows a non-linear behavior, being influenced by the applied drain-source voltage. The last internal parasitic capacitance is the drain-source capacitance, C_{DS}, which is attributed to the body drift diode and varies inversely with the square root of the applied drain-source bias.

The equivalent electrical circuit of an n-channel power MOSFET with the parasitic components is shown in Figure 3-5. These parasitic components have a high impact on the device switching performance, dictating the shape and slopes of the MOSFETs current and voltage switching waveforms. During switching the external gate driving circuit has to charge and discharge the input capacitance, C_{iss}, formed by C_{GS} and C_{GD}, while considering the internal gate resistance, R_{Gint}. These devices mainly dictate the switching speeds the device can achieve, the switching losses and the required gate driving power. C_{DS}, in conjunction with the drain current, also dictates the shape of the voltage waveforms during switching, influencing the device switching losses.

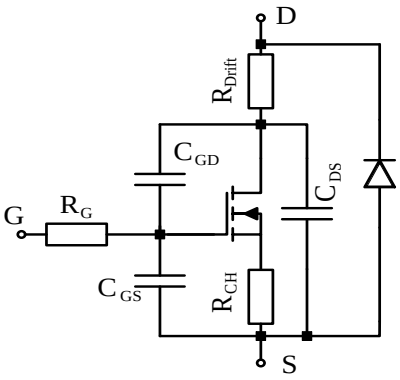

Figure 3-5 Electrical equivalent circuit of MOSFET with parasitic components [9]

3.2. Switching performances

In order to evaluate the turn-on and turn-off performances of a power MOSFET, a clamped inductive test circuit is used, as an inductive load is usually existent in the application where such devices are used, especially in DC-DC converters. A simplified schematic of the typical test circuit is shown in Figure 3-4 and is normally referred to as a Double Pulse Tester (DPT).

In order to simplify this analysis the parasitic inductance of the circuit is going to be ignored (no overshoot of the drain-source voltage) and the current through the inductor is going to be considered constant. Despite this, the analysis will not differ

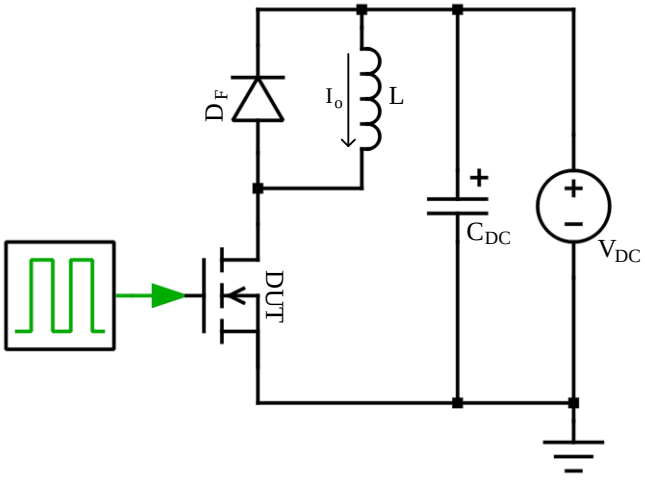

Figure 3-4 Test circuit for clamped inductive switching characterisation of Power MOSFETs

too much from what a power MOSFET behaves in real life, as it is general desirable and achievable to obtain a low parasitic inductance in the circuit through careful consideration and design of the circuit.

The turn-on time for a power MOSFET is influenced by the internal parasitic components of the device, if maximum power dissipation is ignored, limits the transition period to:

$$\tau_{co} = \frac{1}{2\pi C_{iss} R_G} \tag{3.1}$$

where R_G is the gate resistance and is equal to:

$$R_G = R_{Gext} + R_{Gint} \tag{3.2}$$

with R_{Gint} being the device internal parasitic gate resistance and R_{Gext} is the resistance added in the gate circuit in order to control the switching behavior of the device.

The turn-on waveforms for the power MOSFET are shown in Figure 3-6, where at time t=0 the voltage applied to the gate is stepped from zero to V_{GG}, with V_{GG} larger than the V_{th}. During the first interval, $t_{d(on)}$ (turn-on delay time, V_{GS} will rise from zero to V_{th}. This delay is given by the charging of C_{GS} and C_{GD} by the current flowing through the gate resistor R_G, as shown in Figure 3-7a. The voltage rises almost linearly and is defined by the time constant $\tau_1=R_G(C_{GS}+C_{GD})$.

Afterward, in the following interval, V_{GS} continues to rise with the same slope as before. An inversion channel start forming under the gate and drain current, I_D, starts flowing though the device with a linear slope. The device will operate in the saturation region. This is associated with the equivalent circuit shown in Figure 3-7b. The drain-source voltage, V_{DS}, stays constant until I_D reaches I_o, which is the same current running through the inductor, I_L. t_{ri} is the current rise time, representing the time interval needed for I_D to ramp from zero to I_o.

Since the freewheeling diode, D_F, is not ideal, it has a reverse recovery current I_{rr}, I_D increases beyond I_o to I_o+I_{rr}. This will also force V_{GS} to temporarily increase beyond $V_{GS,Io}$, until I_{rr} goes to zero and the diode turn off. When this happens, V_{GS} will decrease to $V_{GS,Io}$ and the gate current, I_{GS}, flowing though C_{GD} will temporarily increase as shown in Figure 3-7c. This current will also cause a rapid decrease in V_{DS}. $V_{GS,Io}$ is the gate-source voltage required to clamp I_D to I_o while the device is the active region.

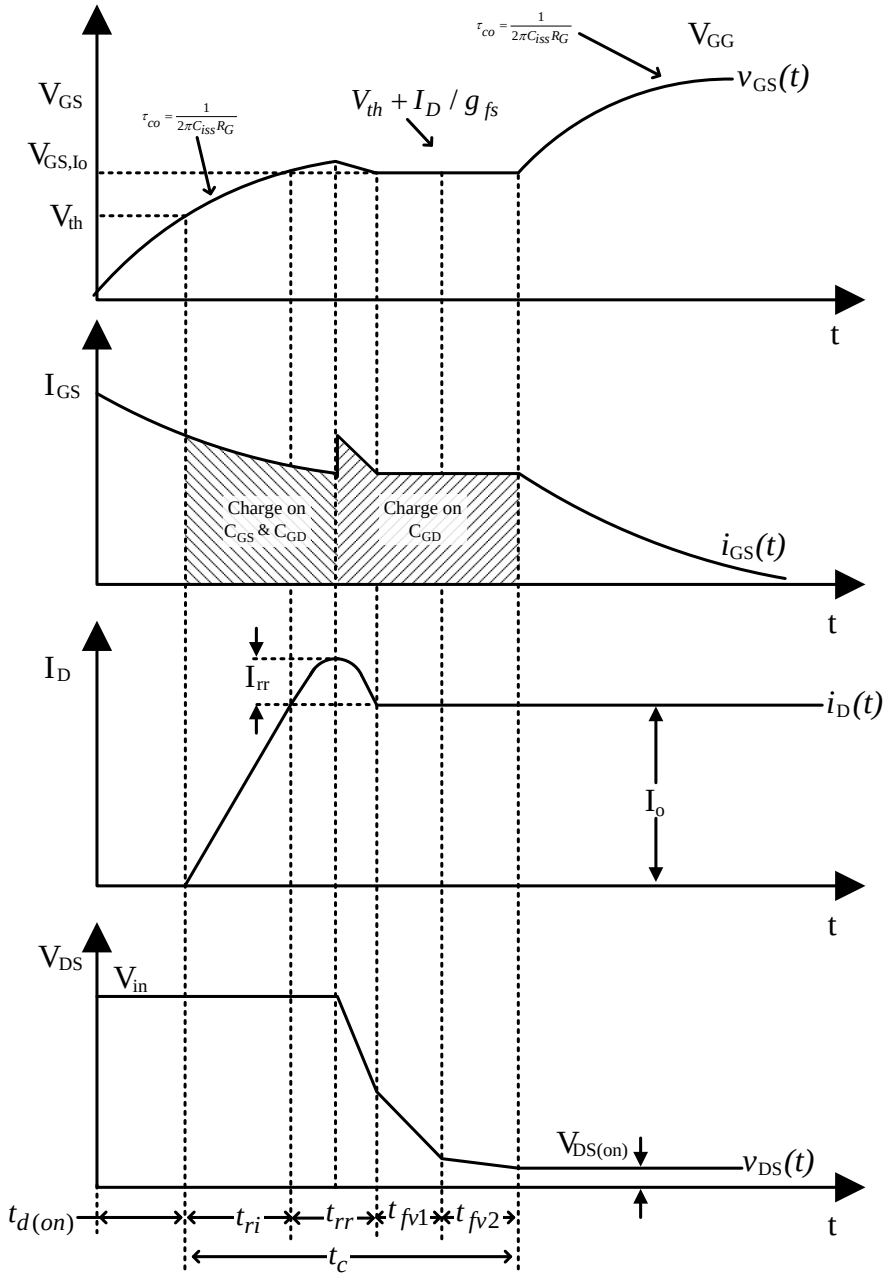

Figure 3-6 Turn-on waveforms of the MOSFET with inductive load (based on [9])

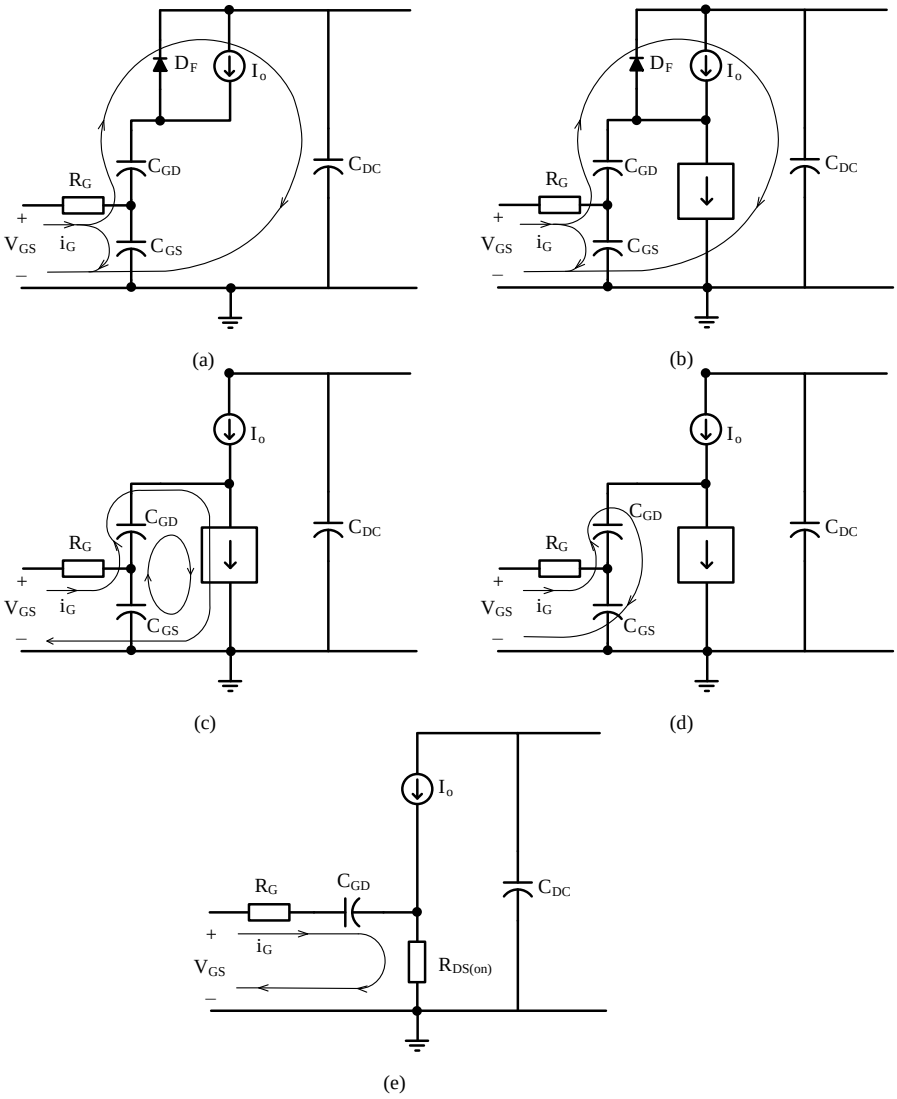

Figure 3-7 Equivalents circuits used to estimate the turn-on voltage and currents waveforms for a power MOSFET used in a clamped inductive double pulse tester: (a) equivalent circuit during turn-on delay time ($t_{d(on)}$) (b) equivalent circuit during the rise time (t_{ri}); (c) equivalent circuit during free-wheeling diode reverse recovery (t_{rr}); (d) equivalent circuit during the drain voltage decrease while the device is in the active region (t_{fv1}); (e) equivalent circuit during the drain voltage decrease as the device swithces to the ohmic region (t_{fv2}) (based on [9])

After the reverse recovery period of the diode is over and the device carries to full load current I_o, the gate-source voltage is clamped at while still in the active region. During this time I_{GS} is given by the voltage drop over R_G due to the difference between the applied gate-source voltage and the voltage at which the gate is clamped. This current will flow though C_{GD} as shown in Figure 3-7d. V_{DS} will decrease in the time interval t_{fv1} as the device crosses though the active region toward the ohmic region.

In second time interval that V_{DS} decreases, t_{fv2}, the devices passes into the ohmic region and the associated circuit is shown in Figure 3-7e. When the drain-source voltage becomes smaller than the gate-source voltage, in this case $V_{GS,Io}$, the device leaves the saturation region and goes into linear operation. This coincides with the collapse of the depletion region which will increase C_{GD} as the device enters the ohmic region ($V_{DS}<V_{GS}-V_{th}$). V_{DS} will have a slower decrease rate because of the increased capacitance of C_{GD}. This time interval will end once the drain-source voltage will reach its on-state value, given by $I_o \cdot R_{DS(on)}$. At this point V_{GS} is unclamped and continues to grow exponentially until it reaches the applied gate-source voltage V_{GG}.

The turn-off waveforms are shown in Figure 3-8 and it involves the same steps as during turn-on, but in a reverse sequence. At time zero the device is turned off by applying zero volts to the gate. If the device permits, negative voltage can also be applied to turn off the device, as this will give a higher gate current and will speed up the turn-off transient. Also, different values for R_G can be used for turn-on and turn-off in order to speed up or slow down the device, depending on the application requirements.

The switching losses resulting from the turn-on/turn-off transients are mainly concentrated in the time interval t_c in Figure 3-6 and Figure 3-8. The instantaneous power losses $p(t)=v_{DS}i_D$ is very high during this transition time. While the on-state resistance of the device varies with temperature which will result in conduction losses varying with the junction temperature of the device, the MOSFETs' internal parasitic capacitances variation with temperature is negligible. Thus, the switching losses are marginally influenced by the actual junction temperature of the device. On the other hand, the gate resistance used for turn-on/turn-off of the device, limits the current which flows though the parasitic capacitances and can have a large impact on the devices' switching losses and can be selected as a function of device controllability, desired switching waveforms and switching losses.

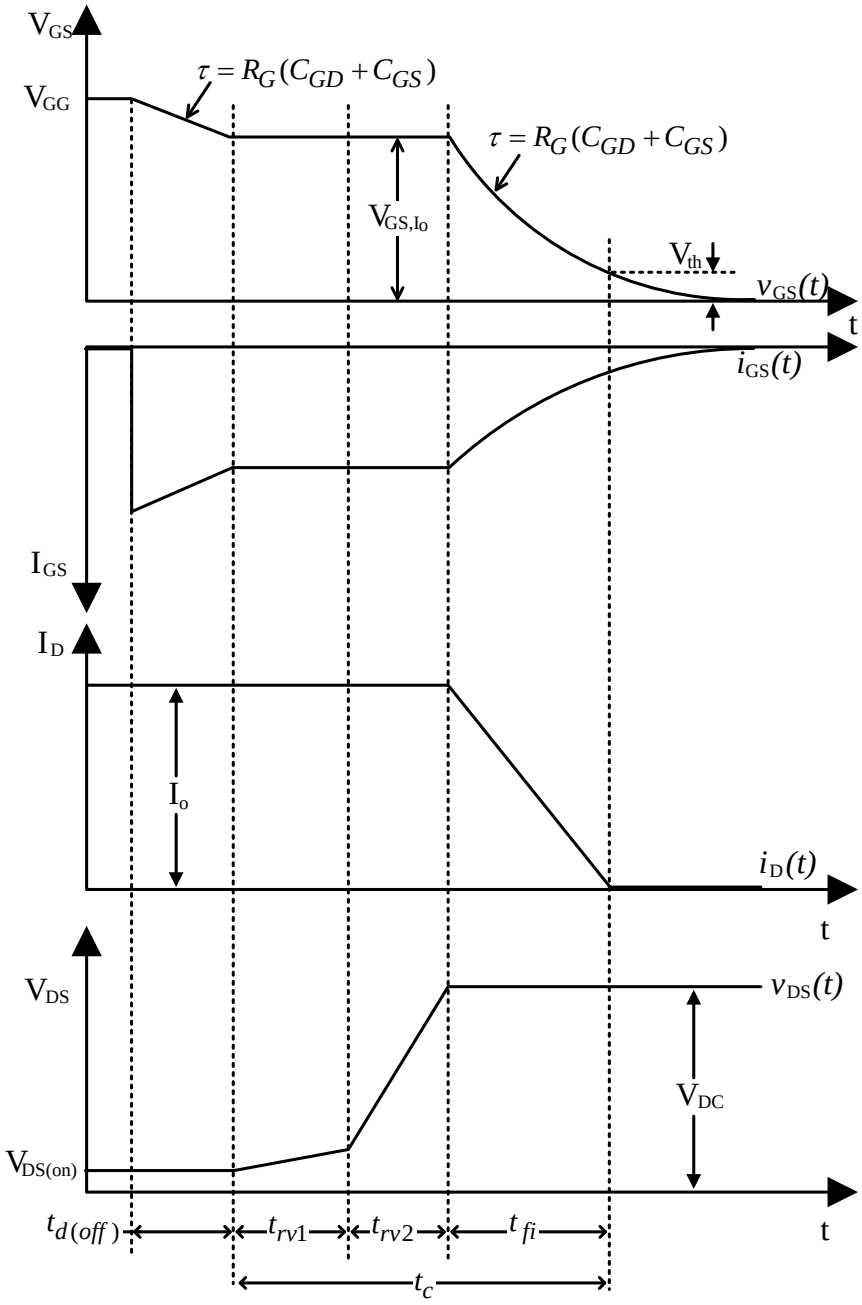

Figure 3-8 Turn-off waveforms of the MOSFET with inductive load and ideal free-wheeling diode (based on [9])

3.3. SiC MOSFETs history and status

As mentioned before, only being on the market for less than two decades, SiC based devices are still in their infancy when compared to Si ones. Despite this, research efforts focused on 4H-SiC and the knowhow acquired from Si based devices gave large progresses and improvements. Most if not all current commercially available SiC MOSFETs are based on the DMOSFET structure and use 4H-SiC material as the semiconductor.

In the early stage of development different attempts were made to create a suitable power device based on SiC which would accelerate the transition from Si to WBG semiconductors with higher breakdown field, with special focus on SiC for voltage levels above 600V. For a vertical unipolar power device, the theoretical minimum value of specific on-state resistance, defined as resistance-area product, under optimal punchthrough conditions can be expressed as [49]:

$$R_{on,sp} = \left(\frac{3}{2}\right)^3 \frac{BV^2}{\mu_n \varepsilon_s E_c^3} = \frac{3.375 BV^2}{\mu_n \varepsilon_s E_c^3} \tag{3.3}$$

The first SiC based MOSFETs were reported in the late 1980s [58]-[60] but the first power MOSFET based on SiC was presented by Palmour *et al.* only in 1994 as a vertical trench MOSFET (UMOSFET) [61]. The device showed a specific on-state resistance of $33 m\Omega \cdot cm^2$ and a blocking voltage of only 150V. This was improved afterwards in 1996 to a specific on-state resistance of 18 $m\Omega \cdot cm^2$ for a blocking voltage of 260 V [62]. In 1997, Agarwal *et al.* presented a 1.1kV SiC UMOSFET with a specific on-state resistance of $87 m\Omega \cdot cm^2$ [63]. SiC semiconductor, being a highly thermal and chemical material creates challenges during manufacturing, and solution used in the fabrication of Si based devices are not practical for SiC. UMOSFET structure was initially selected to develop a power SiC MOSFET based on it manufacturability. The base and source regions in the UMOSFET can be formed epitaxially, instead of ion implantation which requires annealing temperatures between 1000 °C and 1700 °C. The channel in a UMOSFET structure is formed in the trench created with reactive ion etching, as chemical etching is not a viable solution. Despite its easier way to manufacture, the SiC UMOSFET structure comes with some disadvantages. Due to the way the gate in designed, the channel mobility was as low as $1.5 cm^2/V \cdot s$ [63]. Another disadvantage of the UMOSFET structure was related to the high electric fields which are developed in the device. Due to the high critical field of SiC semiconductor, the electric field at the p-n junction is 10 times higher when compared to Si semiconductor, leading to very high fields in the gate oxide, close to the oxide breakdown field [49]. Combined with the sharp corners of the trench structure which will lead to field concentration, it will result in oxide failure and

reliability problems. In order to surpass the disadvantages of the UMOSFET structure and avoid reliability problems related to the gate oxide breakdown due to the sharp trench corners, the double-implanted DMOSFET [19] structure was proposed in 1996 and the accumulation-channel UMOSFET [64] structures where proposed in 1997.

The accumulation-channel UMOSFET proposed in 1997 was designed to avoid the sharp corners field concentration in the classical UMOSFET by rounding the trench corners and adding an n-type epilayer on the side of the etched trench [64]. A blocking voltage of 450V and a specific on-state resistance of 10.9 $m\Omega \cdot cm^2$ were reported for the device. Purdue University improved on this design by adding a grounded, shielding p-type ion implanted region in the trench structure [65]. This shielded the oxide from the high electric fields when device was in blocking state. The device also had a thin n-type epilayer inserted between the n-type drift region and the p-type base region. This helped reduce the current crowding phenomenon around the trench corners by allowing better lateral distribution of the current during conduction. The device showed a blocking voltage of 1.4 kV and a specific on-state resistance of 15.7 $m\Omega \cdot cm^2$.

As mentioned earlier, the DMOSFET structure was proposed as an alternative to avoid the UMOSFET disadvantages due to field concentration in the corners of the trench structure. This was first proposed with a 6H-SiC semiconductor material in 1996 [19]. Due to its material properties, impurity diffusion is unfeasible in SiC, hence the base and source regions are successively created by ion implantation. Since p-type implant annealing is done at temperatures in excess of 1600 °C, challenges arise in the manufacturing process as self-aligning of the implant is not feasible and larger tolerance for realignment of the different regions (base, gate, source) have to be taken into consideration [49]. Despite these, the device presented manage to show a blocking voltage of 760 V with a specific on-state resistance of 125 $m\Omega \cdot cm^2$. Compared to previous SiC UMOSFETs presented before, this device blocking voltage was almost three times larger than the ones presented before. The DMOSFET structure also presents some drawback due to arrangements. The resistance of the JFET region formed between the p-base regions of the devices adds up to the device specific on-state resistance and creates challenges when designing the devices. If the JFET region is reduced, by increasing the distance between the two p-based regions in the cell, the area of the cell is also increased, thus increasing the rest of the components parasitic resistances. At the same time, this increase in the spacing between the p-bases will result in a higher electric field in the gate oxide and diminishing the voltage blocking capability. Despite these drawbacks, the remarkable result obtained with the new DMOSFET structure determined others to try and improve on the structure. Most notable here are: the accumulation-channel DMOSFET in 1997 [66], with a rated voltage of 350 V and a specific on-state resistance of only 18 $m\Omega \cdot cm^2$, the triple implanted DMOSFET in 1998 [67], with a rating of 1.8 kV and a specific on-state resistance

of 82 $m\Omega \cdot cm^2$ and in 2000 [68] a static induction channel accumulation FET with rated voltage of approximately 2 kV, 4.1 kV and 4.6 kV and specific on-state resistances of 172 $m\Omega \cdot cm^2$, 324 $m\Omega \cdot cm^2$ and 387 $m\Omega \cdot cm^2$.

In order to terminate the edges and problems arising from the high electric fields associated, floating guard were used to create a 2.4kV 4H-SiC DMOSFET in 2001 by Cree [69]. As a world first, in 2003, Cree presented a 10 kV 4H-SiC DMOSFET with a specific on-state resistance of 236 $m\Omega \cdot cm^2$ [39]. The effective channel mobility was still small, at 14.5 $cm^2/V \cdot s$. This was followed in 2004 by another 10 kV 4H-SiC DMOSFET with an improved specific on-state resistance of 123 $m\Omega \cdot cm^2$ [70] and in 2006 a specific on-state resistance of only 111 $m\Omega \cdot cm^2$ was achieved for a 10 kV device [71]. The first commercial SiC device was brought to market as a DMOSFET structure in 2011 by Cree [21], also referred to as first generation Cree device, as a reference to the manufacturing process. At the same time, using the same manufacturing process, a 10 kV 10 A 4H-SiC DMOSFET was presented [72]. At that time it was the largest SiC chip even built with a 8.11mm by 8.11 mm dimensions. Devices manufactured as generation 1 showed reliability problems regarding their body diode due to recombination induced stacking faults in the p-n diode [73]. This effect was more evident in the case of 10kV devices, but it applied also to the lower voltage devices, and it was recommended to use a JBS diode in parallel with the body diode. The initial problems of the 4H-SiC DMOSFETs related to the gate oxide and threshold voltage instability and drift [74], [75] have been largely reported as solved or diminished through improvement and optimization of the manufacturing process [76]. In 2013 Cree launch its second generation of 4H-SiC DMOSFETs as they improved and optimized their manufacturing processes. This devices where mainly designed for the PV market and where rated for 1.2 kV with a specific on-state resistance of approximately 5 $m\Omega \cdot cm^2$. No 10 kV DMOSFET was presented for the second generation of manufacturing. In 2014, after improvements in the manufacturing processes, the third generation 4H-SiC MOSFETs where presented by Cree with voltage ratings ranging from 900 V up to 15 kV and specific on-state resistances ranging from 2.3 $m\Omega \cdot cm^2$ for the 900 V unipolar device up to 123 $m\Omega \cdot cm^2$ for the 10 kV and 15 kV devices [22].

Figure 3-9 summarizes the most relevant devices with SiC MOSFETs since their first introduction in 1994 until present times. The blue and red lines shows the theoretical limits of Si and SiC semiconductors as defined by equation (3.3). The pink line shows the current SiC state-of-the-art for unipolar devices. The data is presented as the a mark with the year and company/institute that presented it, based on references [19], [21], [22], [39], [49], [61]-[73].

While the main focus has been on unipolar devices, proof-of-concept bipolar devices have been demonstrated With IGBTs with voltage ratings of 12 kV and

15 kV in 2012 and specific on-state resistances of 24 $m\Omega \cdot cm^2$ and 5.3 $m\Omega \cdot cm^2$ [77], Gate Turn-off Thyristors (GTOs) with voltage rating of 12 kV [78] and 20 kV and 11 $m\Omega \cdot cm^2$ specific on-state resistance and Emitter Turn-off Thyristors (ETOs) with a rating of 22 kV and a specific on-state resistance of 7.7 $m\Omega cm^2$ [79]. To the authors knowledge this are the higher rated voltages for power semiconductor devices achieved until the time of writing.

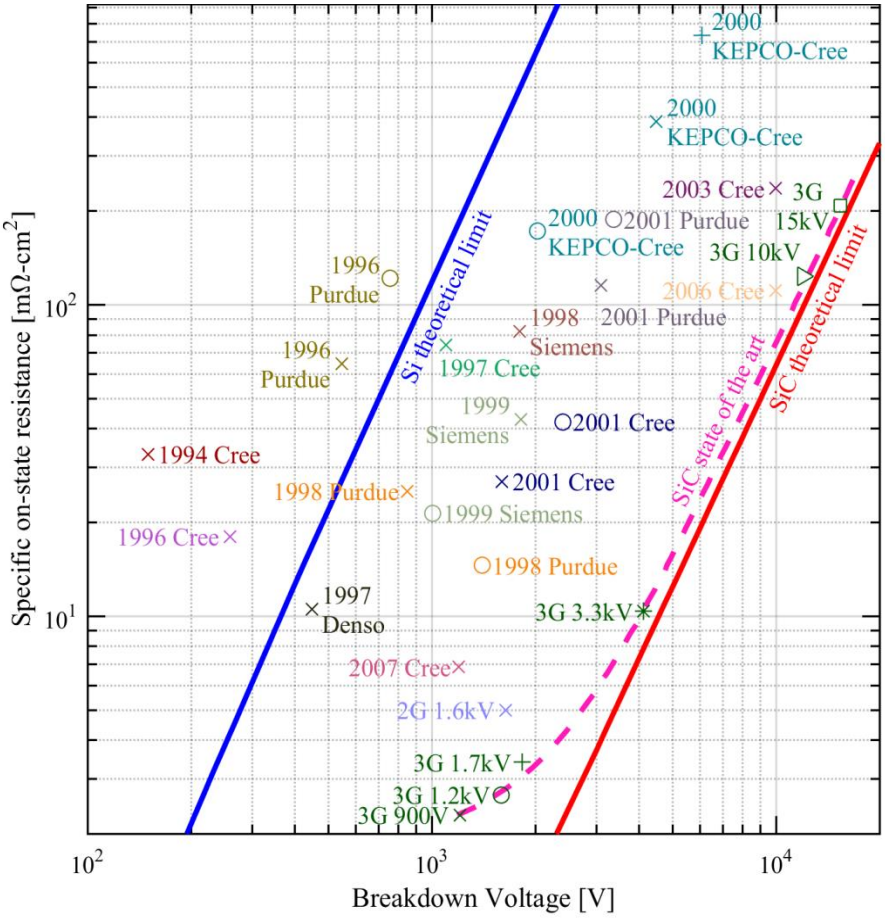

Figure 3-9 Specific on-state resistance and breakdown voltage of representative SiC MOSFETs fabricated since 1994 until the present. Solid lines represent the theoretical material limits of Si and SiC as given by equation (3.3) and the dash line represents the current state of the art in SiC MOSFETs. The plot is not complete, and only presents the devices and manufacturer for which the specific on-state resistance and breakdown voltage were given or could be derived .3G and 2G data represents second and third generation of devices from Cree Inc. [19], [21], [22], [39], [49], [61]-[73]

Despite the higher blocking voltages, SiC bipolar devices are not highly desirable due to their increased conduction losses, slow switching times and specific tail currents. At the same time SiC unipolar devices allow for fast switching times, are new on the market and their limits have yet to be explored, making SiC bipolar devices.

SiC-based MOSFETs, having a much lower on-state resistance than their Si-based counterparts allow for the development of power MOSFETs with very high voltage ratings. This would permit SiC MOSFETs to replace Si IGBTs in high power high voltage applications while at the same time reduce the conduction and switching losses and increase the switching frequency of those applications and further limiting the power electronics converter losses and dimensions by allowing a decrease in the size and dimension of the passive components [80].

To the authors knowledge five technologically different 10 kV SiC devices have been manufactured until the time of the writing. The first two devices [39], [70], could be considered proof of concept, as to their very low current capability (<200A) would make them unsuitable for power applications. The third device [71] was an improvement of the previous technology managing to achieve a current capability of 5A. This device has been extensively studied in [40], [44], [81]-[83] and showed surprising results when compared against Si IGBTs in high power high voltage converters. The fourth iteration of the 10 kV 4H-SiC DMOSFET was based on the manufacturing processes for generation one, which defines the manufacturing process for the commercially available devices with lower voltage ratings and showed a current carrying capability of 10 A and a breakdown voltage in excess of 12 kV[72]. The fifth variation of the 10 kV was presented based on the manufacturing process of the third commercial generation from Cree, alongside 15 kV SiC DMOSFETs, which to the authors knowledge until the time of the writing is still the highest rating achieved by any power unipolar device.

Despite the fact that 10 kV SiC DMOSFETs have been presented as since 2003, and available as engineering samples since 2011 in the form of 10 kV 10 A device, due to the scarce availability of such devices, they have not been measured and studied as extensively as the lower voltage devices, especially in the 1 kV range, which have been commercially available to the research and academic world.

In this work the first generation 10 kV SiC DMOSFET (designed as a 10 kV 10 A device) is going to be thoroughly investigated in order to observe the device static and dynamic behavior and highlight the performance and drawbacks of such a device.

3.4. Design of low inductance test setup for discrete packaged 10kV 4H-SiC MOSFETs

In order to evaluate the generation one 10 kV 10 A SiC MOSFET, custom test setups need to be constructed in order to evaluate the dynamic behavior of the device during different transients, such as: clamped and unclamped inductive switching, short-circuit and avalanche breakdown. Ideally, such a test setup would add no parasitic inductance in the test circuit, but since this is impossible, as it is highly desirable for the circuit parasitic inductance to be minimal, and initially the aim was for a maximum parasitic inductance of 10 nH. Designing and constructing such test circuit can be time and resource consuming, it was decided to developed a unified test setup which would enable easy testing of all of the above mentioned transients.

Different test solution for high power devices, and especially SiC unipolar devices have been published in the literature [35], [84], [85]. These solutions allowed fulfilled the versatility requirement by allowing testing the device under all the above mentioned circumstances. They allowed a good control over the test, integrating also protections which gave a big flexibility, such as: ramping the current up in the inductive tests with a separate device in order to avoid heating the device under test (DUT) or disconnecting the DUT at different intervals in order to avoid destruction during testing or different biasing and configuration of the circuit in order to minimize the parasitic capacitances of the circuit which might affect the behavior of the DUT during testing. Despite their versatility, such tests setups which required multiple power sources and auxiliary devices were not suitable designs for such high voltage (>10 kV). For the test setups presented in literature, the devices required to charge the inductor, bypass the DUT as a protection or disconnect it would most of the times be Si IGBTs with higher voltage and current ratings than the device under test. At the time when the test setup was designed devices with ratings above 10 kV which would be able to conduct and switch short-circuit currents where bulky and expensive and were mainly designed with little consideration for their parasitic components, and would add large inductive and capacitive parasitic components. Another disadvantage for such test setups was the increase complexity and length of the circuit which would in itself add a lot of parasitic inductance to the switching path, influencing the device switching waveforms. This could also be observed in the literature when the setups where presented.

Based on the above, it was opted for a simplified solution, as shown in Figure 3-10, which although would not offer the versatility of device protection during destructive tests, it would allow for a low inductance in the switching path, which was more desirable. At the same time the self-heating of the device during inductor charging was not considered a critical design criteria, as the switching current was small compared to the chip size and with a properly designed charging inductor, the

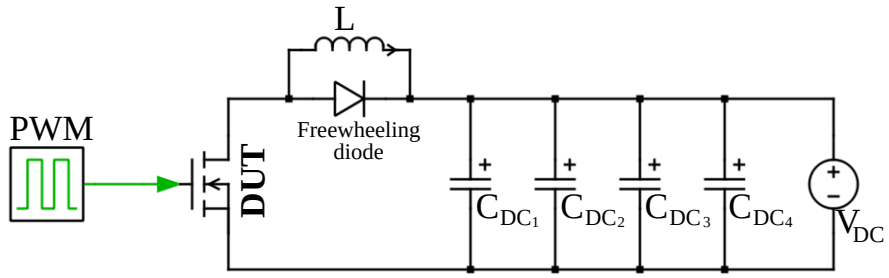

Figure 3-10 Simplified test circuit diagram

current ramp up time could be minimized in order to minimize its impact on the device junction temperature.

Since the device that was going to be tested was packaged in a custom discrete package by Cree with long clearance distances, it was decided to build the test setup around it in order to try and keep the parasitic inductance as low as possible. The packed device is shown in Figure 3-11b). The device drain is soldered directly to the baseplate, which acts also as the drain terminal, making it a challenge when it comes to cooling/heating the device. The gate and source terminals are on the same plane, on opposite sides of the device, 10 mm above the drain terminal in order to ensure sufficient clearance distance during high voltage operation. The source terminal is connected to the source pads on the die via four 250 µm aluminum bond wires, while the gate terminal is serviced by only one 250 µm bond wires. While the bond wires are rather long, the inductance added by them seems negligible [86]. The distance between the interconnection hole on the drain terminal and between the connection holes of the gate and source is 42 mm.

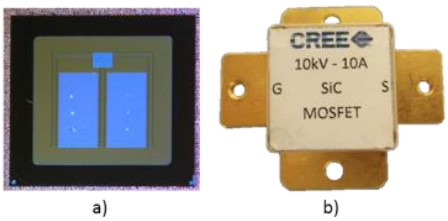

Figure 3-11 10 kV 10 A 4H-SiC MOSFET: a) Bare die; b) custom packaged device [48]

The test setup was designed so that the freewheeling diode and the inductor could be inserter and in the circuit easily, in order to be able to make the transition from one test configuration to the other straightforward. Different planar busbar designs for various applications which might apply also for this versatile test setup, together with their model have been investigated in order to obtain guidance on the design [87], [88].

When designing such a circuit, the storage capacitance of the setup DC-link, C_{DC}, is dependent on the maximum energy which is expected to be sourced, $E_{SC,max}$, the DC-link voltage during short-circuit, V_{DC}, and the maximum allowable voltage drop during short-circuit, ΔV, if it is assumed that $E_{SC,max}$is going to be drawn out of the storage capacitors. The required total DC-link capacitance can be expressed as [35]:

$$C = \frac{2 \cdot E_{SC,\max}}{V_{DC}^2 - \left(V_{DC} - \Delta V\right)^2} \tag{3.4}$$

In general, for power electronics used in converters which are exposed to inductive switching, it is recommended to operate the devices at 60% of their nominal voltage ratings. This is done in order to avoid situations where during turn-off, due to the inductive load and the current in the switching path, the turn-off voltage would overshoot and exceed the devices breakdown ratings. Since the circuit would also be used for short-circuit investigation, the same operating voltage would be assumed. Thus the DC-link voltage for the design was chosen as $V_{DC} =$ 6kV. During short-circuit transients, the MOSFET behaves as a resistor, and in order to obtain proper results it is necessary to ensure that the energy stored in the DC-link capacitor is sufficiently high in order to avoid large voltage variations of the V_{DS} during the transient. For the lower voltage (1.1kV) DMOSFETs the maximum withstand short-circuit energy fount in literature was around 3000 mJ [35], [84]. Since the 10 kV device is large, and in theory should be able to dissipate a larger energy during short-circuit before failing, the storage energy was chosen at 6000 mJ and the maximum voltage drop during short-circuit was selected at 1% of the 6kV DC-link (60V). Based on these requirements, the minimum DC-link capacitance can be calculated using equation (3.4):

$$C = \frac{2 \cdot 6000 \cdot 10^{-3}}{6000^2 - \left(6000 - 60\right)^2} = 16.75\ \mu F \tag{3.5}$$

In order to minimize the parasitic inductance of the test circuit and provide symmetry for the current path from the storage capacitors to the DUT, four identical 6 µF film capacitors with a rating of 15 kV DC are connected in parallel and arrange around the DUT as shown in Figure 3-12. At the time of the design, capacitors with voltage ratings above 5 kV where only designed axially, due to cost and manufacturing limitations. The arrangement of the terminals would require series and parallel connection of capacitors in order to bring the DC-link planes close and reduce the parasitic inductance which might be added otherwise. This would make the DC-link large and unpractical. In order to avoid this, the aluminum capacitors are placed in aluminum sleeves in order to bring both terminals to the same plane. The negative terminal, sitting on the bottom is connected through a

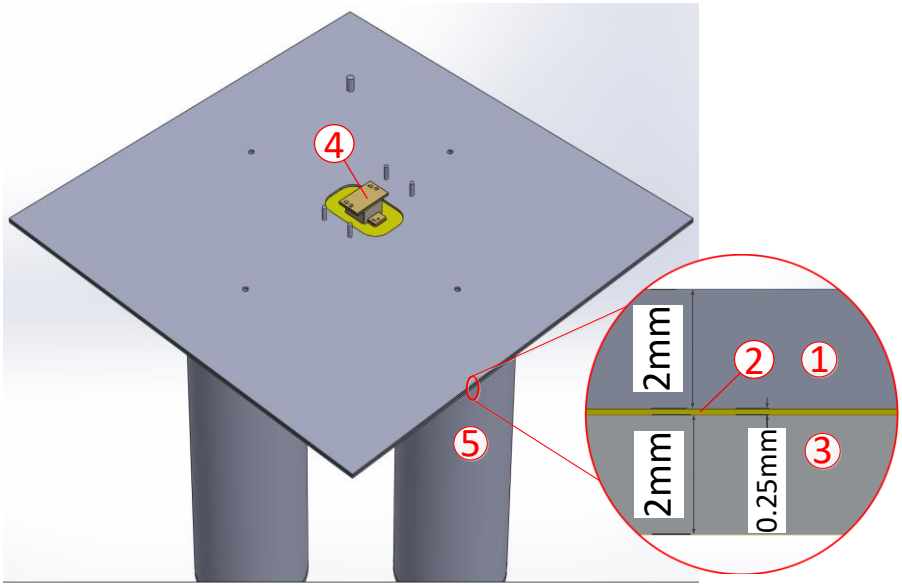

Figure 3-12 Busbar CAD design 1) Positive busbar side 2) Insulation Mylar 3) Negative busbar side 4) MOSFET under test 5) DC-Link capacitors [86]

plate to the slave and at the top of the sleeve a flange connects to the bottom negative plate of the DC-link. Thus the bottom plate of the DC-link is the negative terminal which was designed to be at ground potential and the top is the positive terminal. Since the capacitors where rated to support the 15 kV across the two terminals at opposite ends, they might not be rated to support it when the negative terminal is brought to the same plane. In order to avoid the destruction of the capacitors due to internal dielectric breakdown, it was decided to line the inside of the sleeves with 0.05 µm Mylar film, which has a breakdown rating of 9 kV. In order to ensure even higher breakdown voltage, after the capacitors where inserted in the sleeves, the same silicone gel used in power modules was used to pot the capacitors.

Assuming the capacitors as a single solid conductor and the external sleeve as a hollow cylinder with a known radius, the inductance of each capacitor could be approximated as:

$$L = \frac{\mu_0 l}{2\pi} \ln\left(\frac{R}{r}\right) = \frac{1.26 \cdot 10^{-6} T - m / At \cdot 0.3m}{2 \cdot 3.14} \cdot \ln\left(\frac{0.057m}{0.055m}\right) = 31.86nH \qquad (3.6)$$

where μ_0 is the permeability of free air, l is the length of the sleeve and capacitor, R is the radius of the sleeve and r is the external radius of the capacitor, with all

length measurement in meters. It was also assumed that the current is evenly distributed inside the sleeve and the capacitor. Based on the results from equation (3.6), the inductance of the four capacitors can be calculated as 7.9 nH. The DC-link positive and negative terminals are cut from a 2mm aluminum plate. Mylar foil with a thickness of 0.25 mm and a insulation rating of 20 kV is used in-between the plates in order to support the large voltages. As mentioned earlier the DC-link if formed by two plates on top of each other. This would force the current on each plate to flow in close proximity and in opposite directions, reducing their impact on the circuit parasitic inductance. Also precautions were taken in order to reduce the number of holes in the plates. Thus, screws were welded on the bottom DC-link plate to allow a secure connection with the negative terminal of the capacitors and at the same time to avoid having the large holes in the top plate which would otherwise be needed in order to ensure proper clearance. The DUT is connected to the two DC-link plates directly through cutouts in both plates as shown in Figure 3-13. The gate driver is connected from the bottom side.

In order to validate the calculations, the setup inductance was measured to be 8.09 nH using a E4990A impedance analyzer from Agilent. The test setup was also

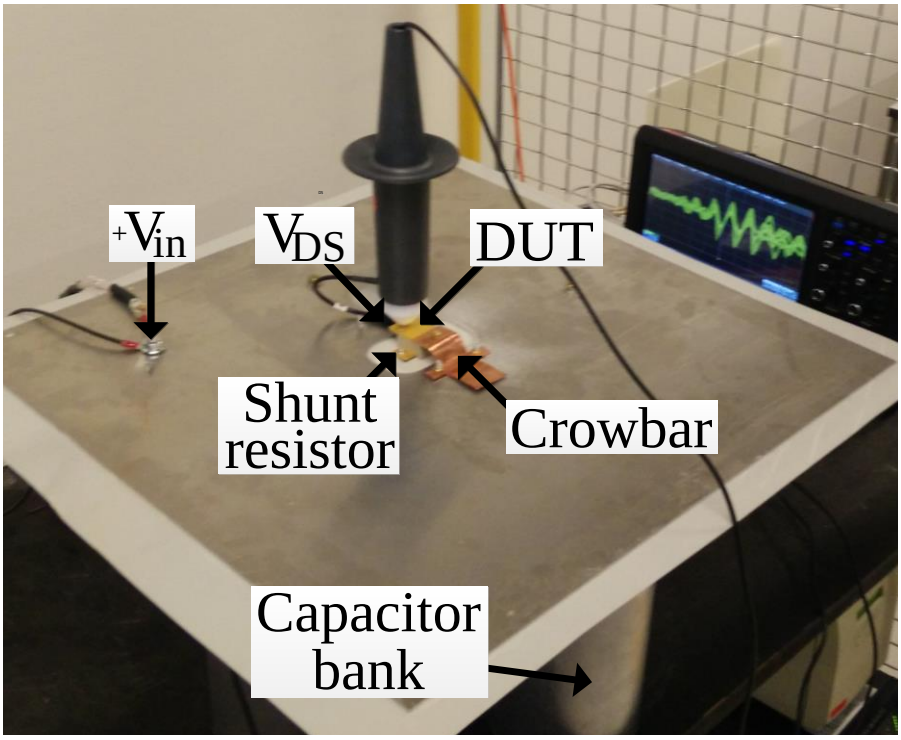

Figure 3-13 Versatile test setup for characterisation of 10kV 10A SiC MOSFETs, configured for short-circuit testing [89]

simulated in Ansys Q3D and analyzed using AC inductance estimation with a mesh of 10^6 triangles. The inductance resulted from the simulation was 8.4 nH.

In order to confirm the results, an inductor and diode where inserted into the circuit and a double pulse test was performed in order to observe the over-voltage experienced by the device during turn-off.

A custom built 20 mH, low capacitance (<5 pF) 10kV inductor was used for current charging. The freewheeling diode was a 10kV 10A JBS diode from Cree in a package identical to the one of the MOSFET [90]. The DC-link was charged to 6 kV and the device was double pulsed at room temperature. The current was measured with a SSDN-001 low inductance shunt resistor from T&M research. The voltage waveforms are acquired with a PHV4002-3, 100Mhz, 20kV passive voltage probe from PMK. All the measurements are recorded with a 12bit oscilloscope from Lecroy. The pulses length were adjusted to obtain a turn-off current of 10 A. The results of the measurement are shown in Figure 3-14. The measured current at turn-off was 9.77A with a fall rate of di/dt=18.27kA/μs by using a gate driver with a −5V/+20V power supply. The over-voltage at turn-off, ΔV, is given by the equation:

$$\Delta V = L\frac{di}{dt} \tag{3.7}$$

V_{DS} rises to 6105V and then settles at 5939V after turn-off. Based on the measured current di/dt and the voltage overshoot the parasitic inductance of the circuit was calculated to be 9.08 nH. This is a bit larger than the one simulated and measured due to the internal parasitic inductance of the 10 kV 4H-SiC DMOSFET and the screws and nuts which are used to connect the DUT to the test setup.

Since the test setup has already been imported into Ansys Q3D for inductance analysis, the current distribution on the plates was also analyzed and is shown in Figure 3-15. For the analysis only one connection point (con. 1) was used. The current is sourced from the four positive terminals of the setup capacitors, marked

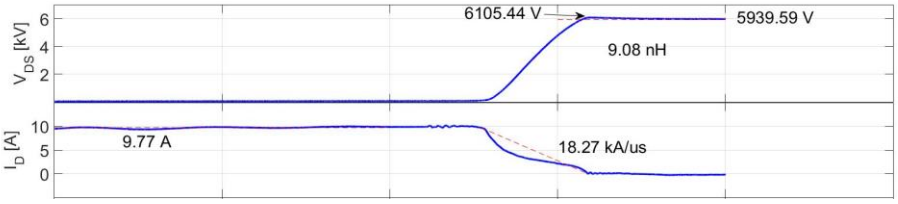

Figure 3-14 Turn-off waveforms at 6 kV and 10 A for 10 kV 4H-SiC MOSFET at room temperature with V_{GS}=−5V/+18V [86]

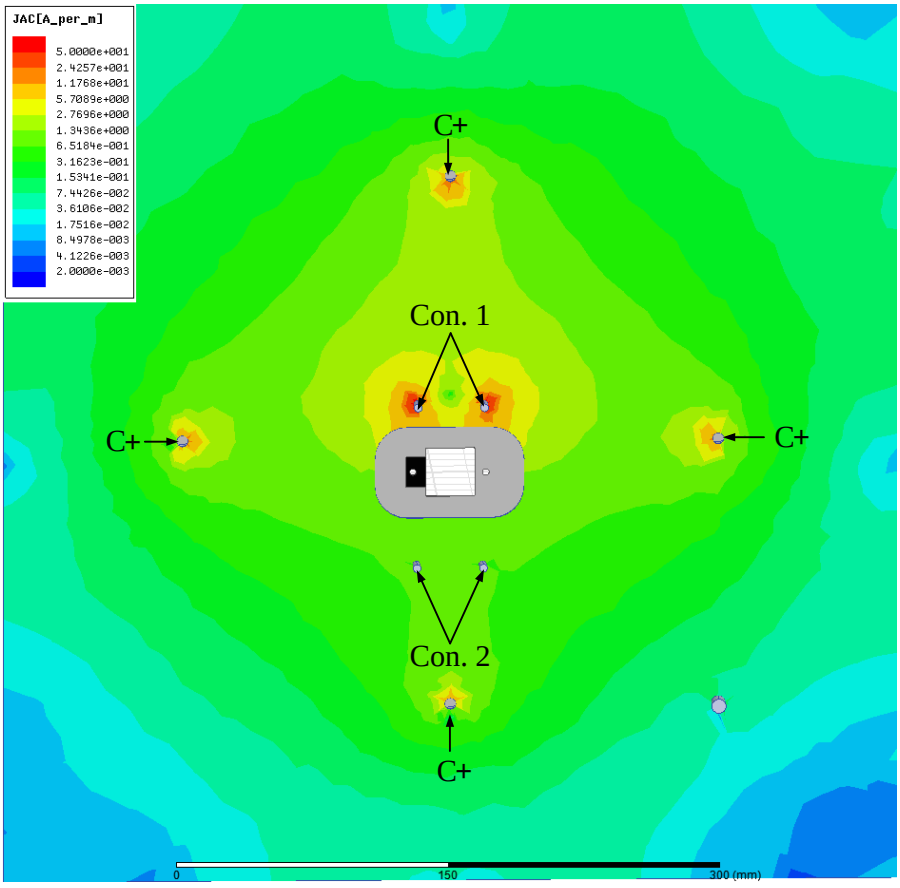

Figure 3-15 Surface current distribution of the busbars of loop 1 at 1 MHz frequency asuming only one connection point for the DUT. C+ shows the positive terminal of the capcitors throw which the current is sourced on the top plate. Con.1 and Con. 2 are the connection points of the DUT during testing.[86]

with C+ and is sinked into the two terminals of the connection point Con. 1. It can be observed that overall the current distribution is even among the four capacitors, and the symmetrical arrangement around the DUT would allow for a good current distribution, especially if Con. 2 is used during large currents.

This test setup is going to be used to characterize the 10 kV 4H-SiC MOSFET as it showed high energy storage and low inductance which should not affect the measurements or behavior of the device.

3.5. Characteristics of 10kV SiC MOSFET

The 10 kV 10 A first generation SiC MOSFET from Cree has been fully investigated in the literature. This is highly relevant and required before deploying such a device in a converter, in order to assess the different requirements of the device in terms of EMI, cooling etc.

Figure 3-16 shows a simplified cross section of the device under test [22] and the bare die is shown in Figure 3-11a). The chip size is 8.11mm by 8.11 mm.

3.5.1. DC-CHARACTERISTICS

The DC characteristics of the device were measured using a Keysight B1506A curve tracer and a Thermostream ATS-515. The characterization setup is shown in Figure 3-17. A custom measurement program was set up to acquire the specific DC-characteristics of the device. The setup was automated to perform all the

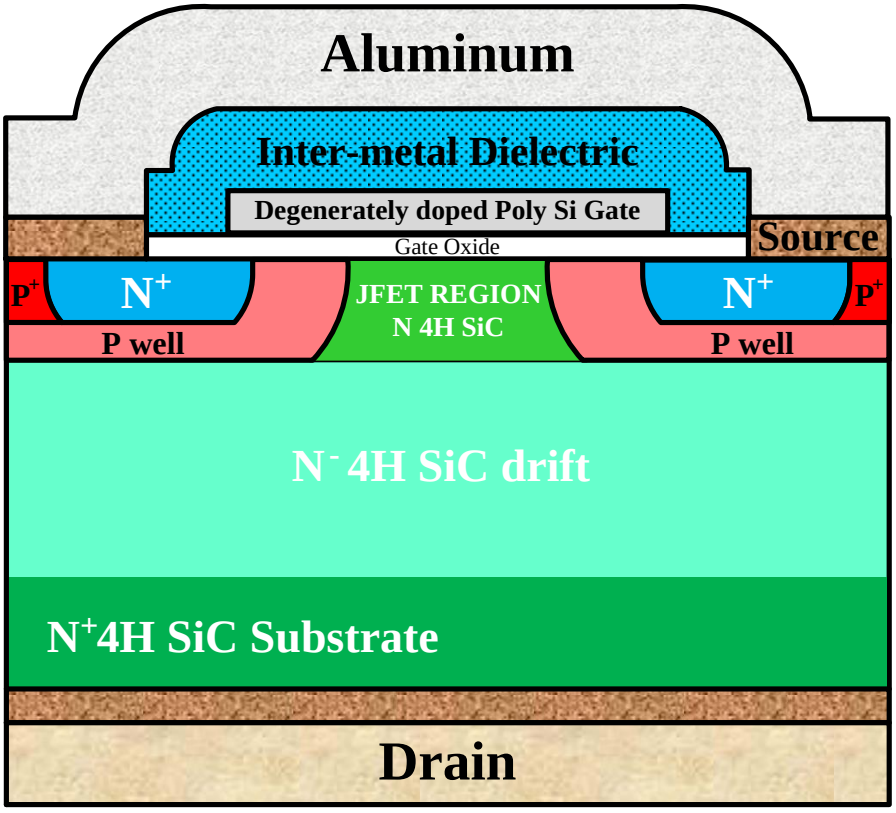

Figure 3-16 Simplified cross section of a 10-kV SiC MOSFET [22]

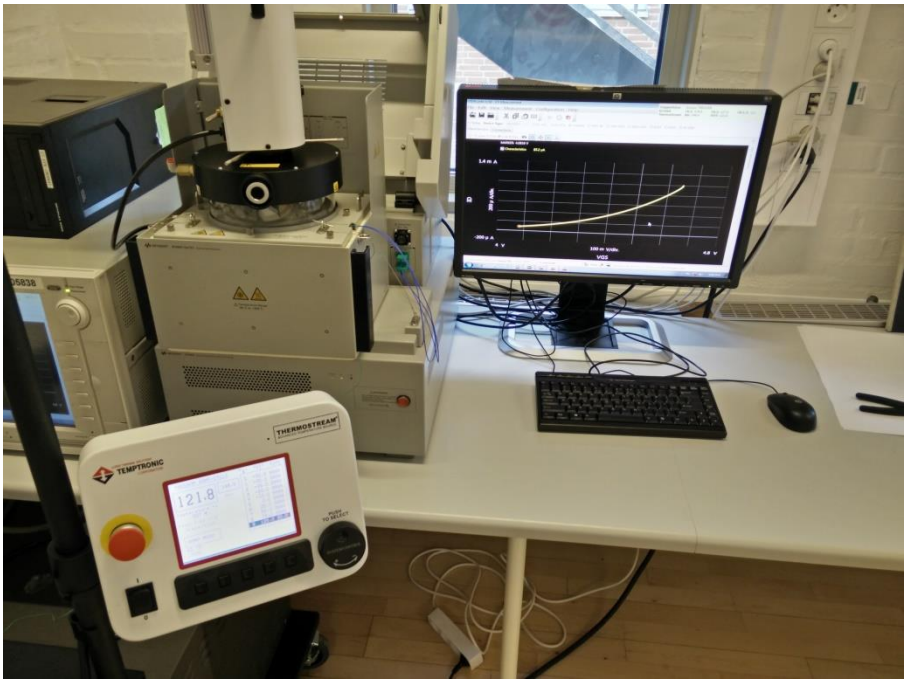

Figure 3-17 DC-characterisation setup

measurement at 25 °C, 50 °C, 75 °C, 100 °C, 125 °C and 150 °C. After reaching a temperature set point the device was soaked for ten minutes at each temperature before the measurements where performed in order to ensure good thermal distribution throughout the device. Two K-type thermocouples were also used to measure the temperature in different locations of the device in order to ensure the device was measured at the desired temperature.

During the test, in order to avoid self-heating of the device, the applied V_{DS} is pulsed for 200µs for each point measurement and a sufficiently long break (>50ms) is taken between each measurement. Each point measurement is repeated for at least 3 times and then the results are averaged in order to ensure accurate measurements.

Based on the information received from Cree, the maximum allowable gate voltage of the device is 20V for turn-on and −5V for turn-off. These are the same values that are going to be used. The turn-on voltage is desired to be as high as possible due to the low channel mobility specific to SiC devices, thus allowing for a better conduction and higher current through the device. The turn-off voltage is advisable to be as low as possible in order to ensure that during high temperature operations, when the device threshold voltage starts decreasing, the device will not turn-on parasitically, due to currents running through the Miller capacitance which

has been observed in SiC devices [13]. This will become more evident as the DC-characteristics are presented.

Despite close collaboration with Cree, the device specific dimensions have not been shared by Cree as they are considered sensitive proprietary information, thus some of the device parameters which might be influenced by the structure, or doping concentration cannot be investigated.

The device forward I-V characteristics have been measured at room temperature and are shown in Figure 3-18. The drain-source voltage was swept from 0V up to 40V while the gate was stepped from 5V to 20V in steps of 1V. Figure 3-19 shows the same measurement performed at 150°C. It can be observed that at higher temperature the current limit of 20A is reached at a higher V_{DS} in the case of high gate voltages (V_{GS}>12V). On the other hand, for lower gate voltages (V_{GS}<12V) the device can conduct higher currents at higher temperature. These two phenomena can be observed better in Figure 3-20 and Figure 3-21 where the influence of temperature on the waveform is shown for a gate voltage of 5V and 20V, respectively. This is mainly related to the device on-state resistance which is defined by the competition of two temperature dependent internal resistances of the device, the channel resistance, R_{ch}, which shows a negative temperature coefficient and the remaining part of the total resistance (commonly referred to as the "residual resistance"), R_S, which has a positive temperature coefficient. The residual resistance is comprised of the contact resistance, JFET region resistance, drift region resistance and the substrate resistance, with the drain region resistance, R_{Drift},

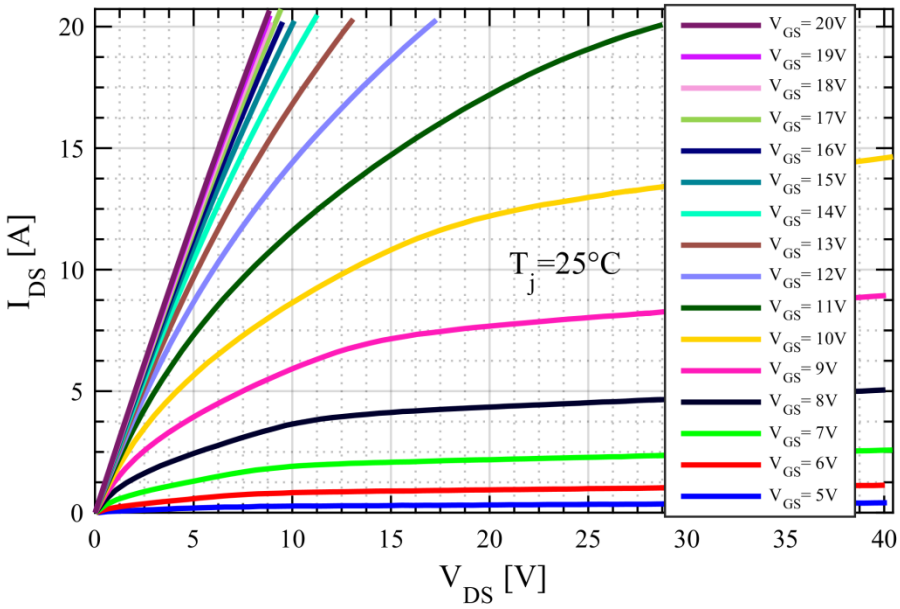

Figure 3-18 Measured forward I-V characteristics of 10kV 10A 4H-SiC MOSFET at 25°C

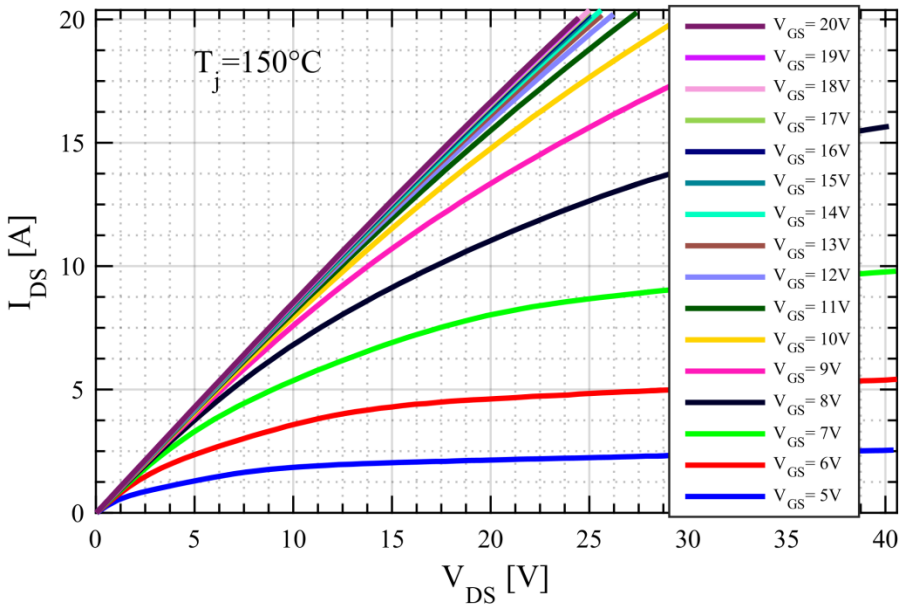

Figure 3-19 Measured forward I-V characteristics of 10kV 10A 4H-SiC MOSFET at 150°C

being the dominant one [91]. R_{Drift} has shown a positive thermal coefficient. This will be discussed in more detail later in this subchapter.

Another observation which can be made from the measured I-V characteristics of the device is the very small difference between the higher gate voltages (V_{GS}*=18-20V)* the device conduction variation is minimal. Thus in case the gate driving circuit has oscillations and overshoots the set limit, a lower driving voltage can be selected in order to avoid damage to the gate oxide with minimal impact on the conduction performance [92].

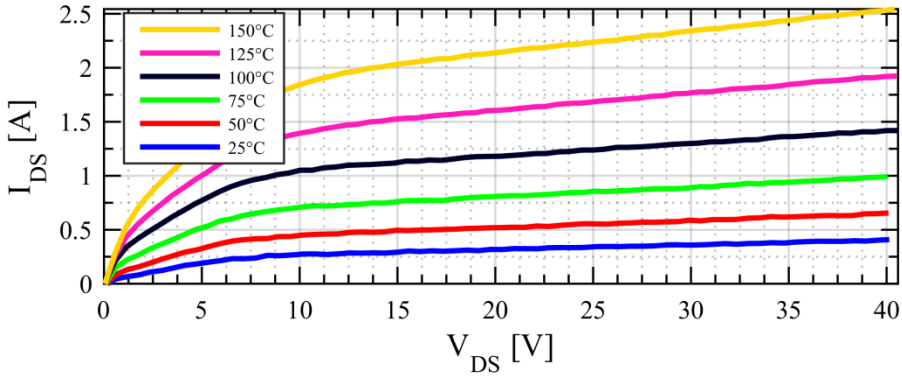

Figure 3-20 Measured forward I-V characteristics of 10kV 10A SiC MOSFET for V_{GS}=5V at different temperatures

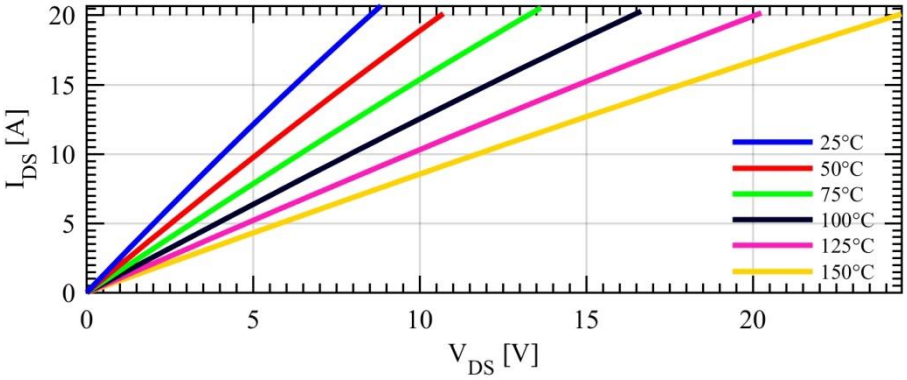

Figure 3-21 Measured forward I-V characteristics of 10kV 10A SiC MOSFET for V_{GS}=20V at different temperatures

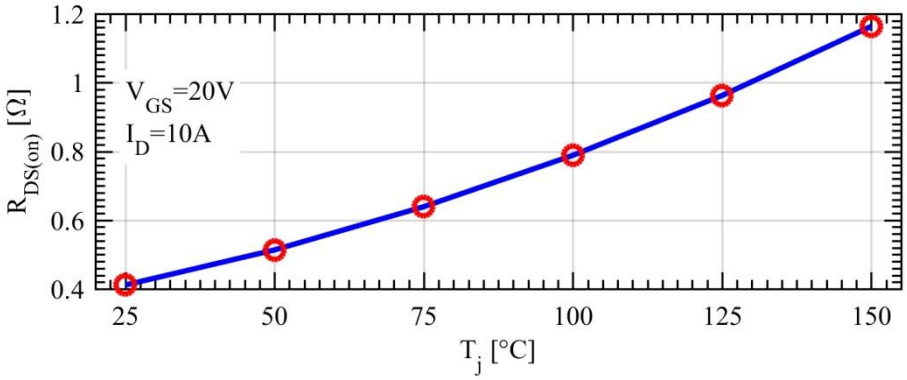

Figure 3-22 Measured on-state resistance of 10kV 10A 4H-SiC MOSFET as a function of junction temperature

The on-state resistance of the device was also measured as a function of the junction temperature for a gate-source voltage of 20V and a drain current of 10A and is shown in Figure 3-22. The device on-state resistance increased from 0.41Ω at room temperature to 1.16Ω at 150°C. The positive temperature coefficient of the on-state resistance is a result of the decrease of the bulk mobility in 4H-SiC with temperature increase and is attributed to the resistance of the drift region and at high gate biases it dominates the total resistance of the device [93]. This can be better observed in Figure 3-23.

Figure 3-24 shows the measured transfer characteristics of a 10kV 10A 4H-SiC MOSFET at different junction temperatures. The measurements where performed at a drain voltage of 20V. It shows the negative temperature coefficient of the threshold voltage, as it decreases with temperature. The measurements also show the change in dominance between the channel resistance and the drift region

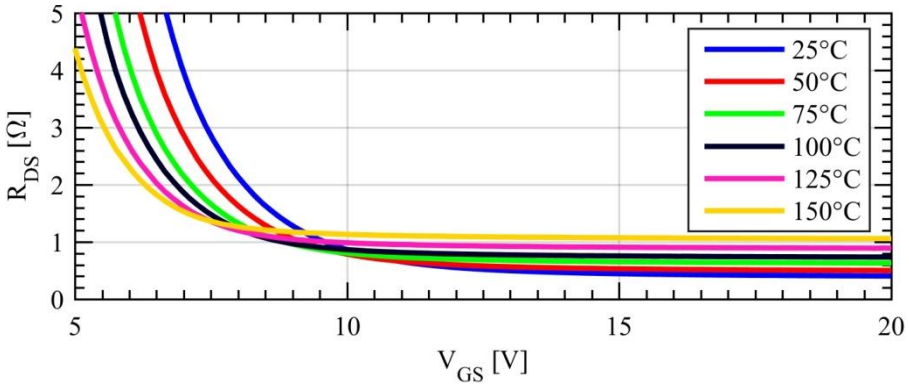

Figure 3-23 Measured on-state resistance of 10kV 10A 4H-SiC MOSFET as a function of temperature and gate votlage for I_D=10A

resistance. Since R_{ch} has a positive temperature coefficient, the device conducts more current at gate voltage values closer to the device threshold voltage, where R_{ch} is dominating the on-state resistance, $R_{DS,on}$. At high gate voltages, R_{Drift} takes over and becomes dominant, and since this increases with temperature, the device current conduction capability decreases.

Generally, in the device datasheet, the threshold voltage is given as the V_{GS}

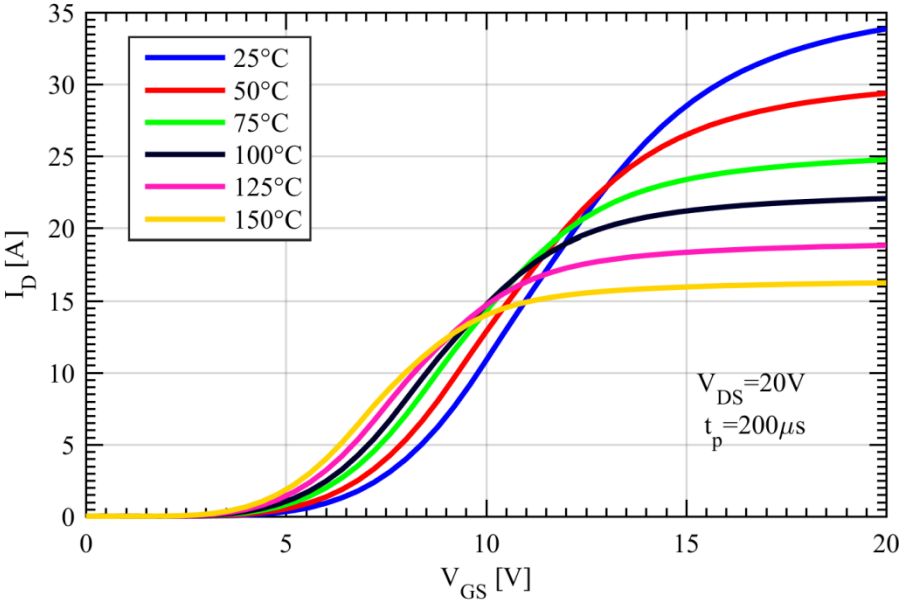

Figure 3-24 Measured transfer characteristics of 10kV 10A SiC MOSFET at different temperatures

value at which the device conducts a specific current when the gate and drain terminals are connected together. While this value is not the correct threshold voltage value it is easier to obtain and it aids the user of the device in comparing similar devices. The threshold voltage is important for the converter designer and aids him in designing the gate driving circuit and selecting the proper gate supply voltage or voltages in case of a bipolar gate driver. Based on the above measuring process, Figure 3-25 shows the measured threshold voltage as a function of temperature for a drain current of 0.1mA.

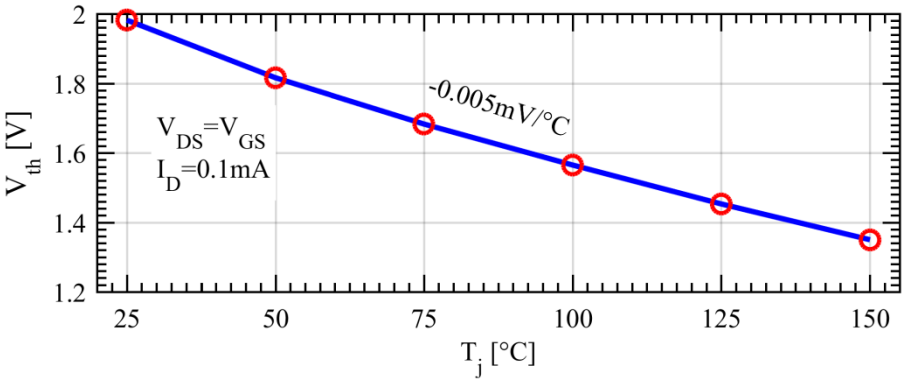

Figure 3-25 Measured threshold voltage variation with temperature for a drain current of 0.1mA

Based on the measurements from Figure 3-24 the transconductance $g_m$was extracted and plotted in Figure 3-26. For this device g_m increases monolithically as V_{GS}increases for low V_{GS} values up to its maximum values and afterwards decreases as V_{GS} continues to increase. It can also be observed that the transconductance increases with temperature at low gate-source voltages and decreases at temperature at higher gate-source voltages. This can be explained by the presence of the residual

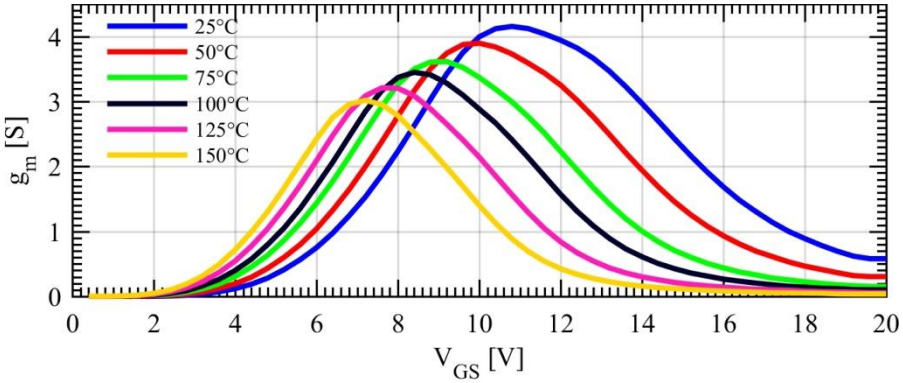

Figure 3-26 Derived transconductance for a 10kV 10A 4H-SiC MOSFET

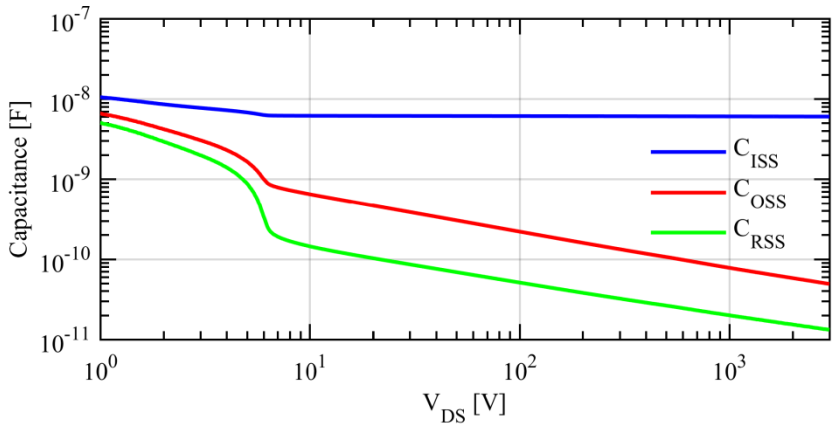

Figure 3-27 Internal capacitances sweep from 1V to 3kV for 10kV 10A SiC MOSFET

resistance in series with the device channel resistance, and the point where g_m is the maximum represents the gate-source voltage where the residual resistance becomes dominant.

The device internal capacitances are shown in Figure 3-27 where the input capacitance, C_{ISS}, is equal to $C_{GS} + C_{GD}$ in Figure 3-3, the reverse transfer capacitance, C_{RSS}, is equal to C_{GD} and the output capacitance, C_{OSS}, is equal to $C_{DS} + C_{GD}$. Considering the current carrying capabilities of the device, the capacitances measured are large, and will play a big role in the behavior of the device in a circuit. C_{ISS} will influence the device transition from conduction to blocking and vice versa. C_{DS} will show a bigger role in a circuit, where it will need to be charged and discharged, thus requiring extra energy input.

3.5.1.1 Channel Resistance and Internal Transconductance

The first 4H-SiC DMOSFETs which were presented in literature had the on-state resistance of the device dominated by the channel resistance, as reported in [70], [71], similar to low voltage MOSFETs. As the channel mobility improved, the device on-state resistance is shared among the residual resistance and channel resistance, with the channel being dominant at lower gate voltages and showing a negative temperature coefficient and the residual resistance dominating in the upper range of the gate voltages and showing a positive temperature coefficient. This behavior can be clearly observed in Figure 3-23, Figure 3-24 and Figure 3-25. While in the early devices current concentration and thermal runaway was a concern as the MOSFET cells in the devices could present mismatches, with the newer devices, this is not the case anymore, because the residual resistance which has a positive temperature coefficient dominates the upper range of the gate voltages, and the cells will self-limit. This would also create challenges when trying

to parallel chips in a module, because the mismatch between devices would result in an unbalance in current sharing.

The total on-state resistance of the device can be expressed as [91]:

$$R_{DS,on} = \frac{L_g}{\mu_n C_g W} \times \frac{1}{(V_{GS} - V_{th})} + R_s \tag{3.8}$$

where L_g is the gate length, C_g is the gate oxide capacitance and W is the gate width.

From equation (3.8) it can be observed that when V_{GS} approaches the threshold voltage, $(V_{GS} - V_{th})^{-1}$ approaches infinity, the total device on-state resistance is largely determined by the channel resistance. Due to the sublinearity of the device output characteristics, the device on-state resistance is highly dependent on the drain voltage even at low drain-source biases as it can be seen in Figure 3-28. This dependence is getting smaller as the applied gate biased is increasing or as the junction temperature increases [93]. Thus, the residual resistance and subsequently the channel resistance can be extracted from the measurements in Figure 3-28 by interpolating the dependencies as shown in Figure 3-29 with the y-axis. This will give the R_S values based on the temperature of the device junction [94], [95]. In [93], the on-state resistances of a vertical DMOSFET (VDMOSFET) and a lateral

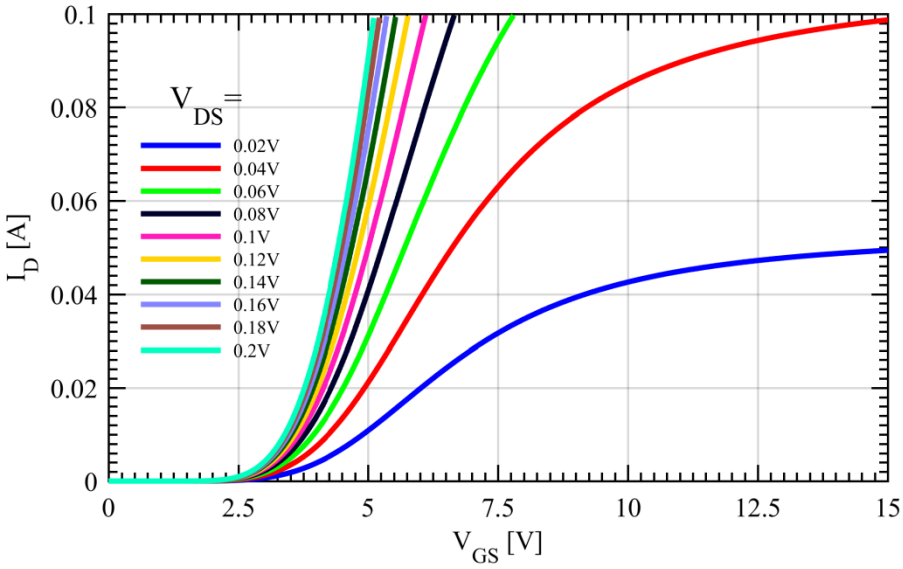

Figure 3-28 Measured transfer characteristics at room temperature for different low drain biases

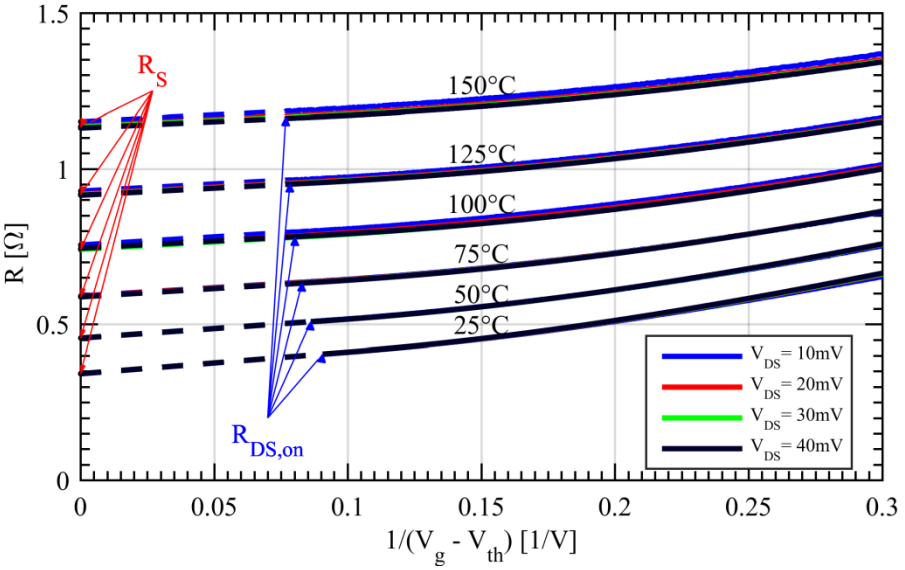

Figure 3-29 Dependences of the total source–drain resistance on $(V_{GS} - V_{th})^{-1}$ for MOSFET under study at different temperatures and drain biases[89]

DMOSFET (LDMOSFET) with similar characteristics have been investigated. It was shown that in the case of VDMOSFETs, the residual resistance is very small (more than 50-100 times smaller) and does not have a dependence on the temperature, thus almost all the residual resistance present in the VDMOSFETs is associated with the drift region resistance. Thus, from this point on R_S and R_{Drift}will be used interchangeably.

In order to better highlight the change in dominance between the residual resistance and channel resistance, Figure 3-31 shows the on-state resistance, derived residual resistance and channel resistance as a function of temperature for two distinct gate voltages. At low gate source voltages (V_{GS}=5V) the channel is dominating the total on-state resistance at low temperatures. But as the temperature increases the channel mobility improves and the channel resistance decreases. On the other hand as the temperature increases, so does the drift region resistance, and at high temperatures becomes dominant. At high gate biases (V_{GS}=20V) the channel conduction improves and its resistance decreases dramatically. The residual resistance dominates the total on-state resistance as it increases with temperature. Despite the fact that the channel conduction improves with the increase in temperature, its impact on the total resistance is negligible at high gate biases. Figure 3-30 shows the same shift in dominance between R_{ch} and R_S at 25°C and 150°C while the gate voltage is swiped from 5V to 15V. At room temperature, the channel resistance dominates the total on-state resistance, but as the gate voltage increases, the channel conduction improves and its resistance decreases, becoming insignificant when compared to the residual resistance. At higher temperature the

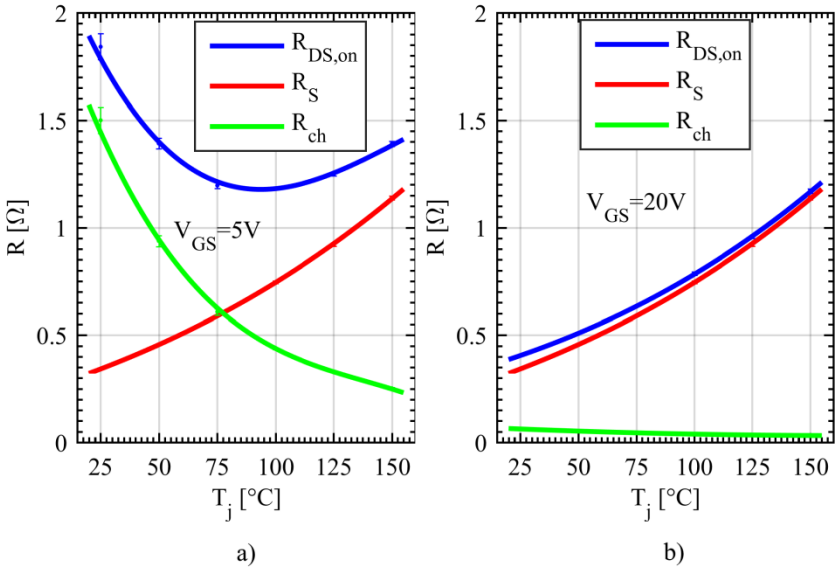

Figure 3-31 Temperature sweep of the onstate resistance, derived residual resistance and channel resistance for gate voltage: a) 5V; b) 20V

electron density and mobility increases in the channel. While at low gate voltages the channel still shows an impact on $R_{DS,on}$ as the gate bias is increased, the channel resistance decreases and so does its impact on the device total resistance.

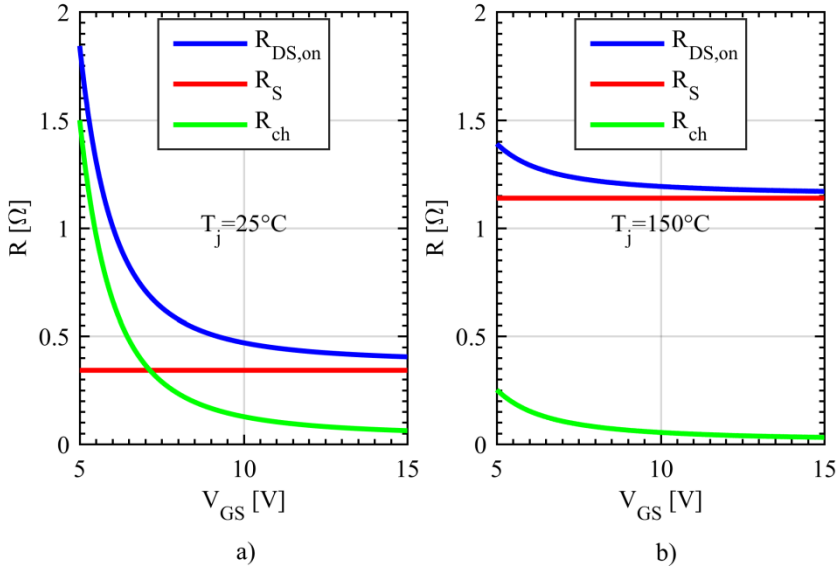

Figure 3-30 V_{GS} sweep of the on-resistance, derived residual resistance and channel resistance for junction temperatures of a) 25°C; b)150°C

Since the measurements performed for Figure 3-28 where done at very low drain-source voltages in order to limit the influence of V_{DS} on the measurements and in order to use the high resolution analog to digital converter of the B1506A curve tracer the threshold voltage can be extracted from the same measurements with a high accuracy.

It can be noticed that in the case of the vertical DMOSFET, the residual resistance is most of the times larger than the channel resistance. This means that the transconductance measured in Figure 3-26 is external transconductance of the device as the residual resistance influences its shape and it is smaller than the intrinsic ("internal") transconductance of the 10kV MOSFET [93]. Considering the linear region, and assuming there is no residual source resistance present, based on [93], the drain current can be expressed as:

$$I_D = C_g \left(V_{GS} - V_{th}\right) \mu_n \left(V_{DS} - I_D R_{DS,on}\right) \frac{W}{L_g} \tag{3.9}$$

where μ_n is the charge-carrier effective mobility. Expressing $g_m = \partial I_D / \partial V_{GS}$ as the external transconductance, the internal transconductance of the device can then be derived as:

$$g_{m0} = g_m \left(1 + \frac{R_{DS,on}}{R_{ch}}\right)^2 \tag{3.10}$$

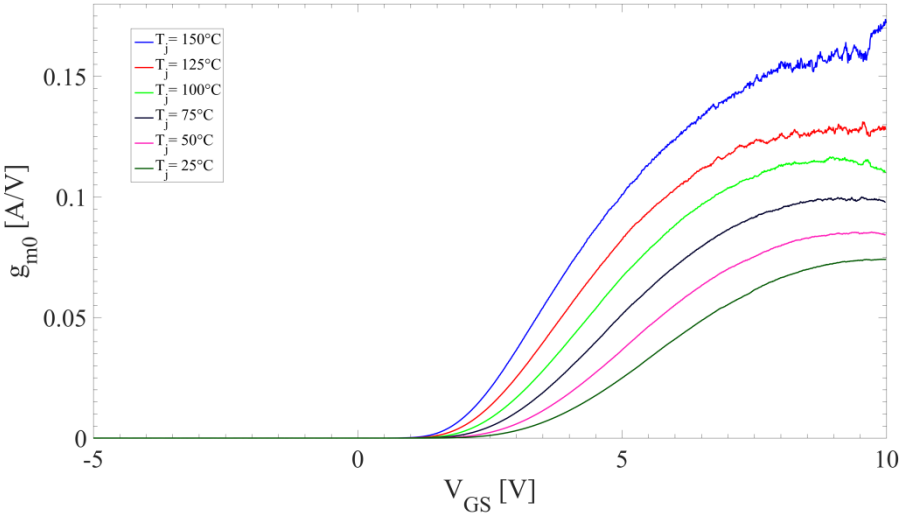

Figure 3-32 Internal transconductance of the 10kV 10A SiC MOSFET

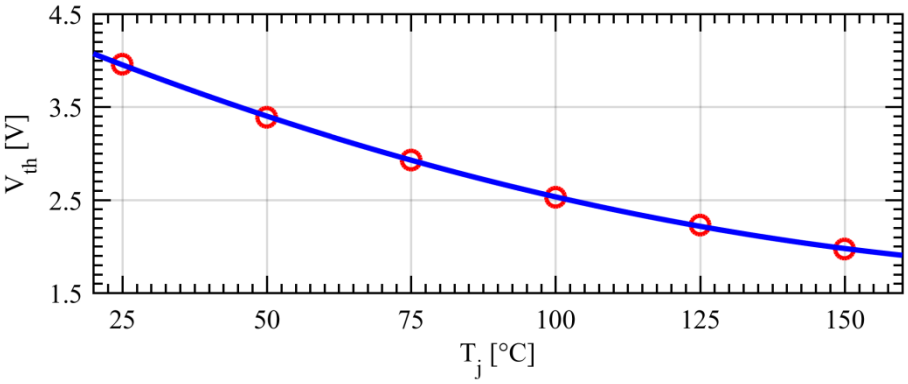

Figure 3-33 Threshold voltage temperature dependence for V_{DS}=5V[30]

By using equation (3.10) and the data for the external transconductance from Figure 3-26, the trend of the internal transconductance of the device is plotted in Figure 3-32. Unfortunately, as the measurement was performed at lower voltages to show the channel impact on the total device resistance, the channel transconductance is also limited in value, but non-the-less, the trend can be observed.

The threshold voltage was extracted as a function of temperature using the second derivate method as described in [96] and it is shown in Figure 3-33. The second derivative method showed good accuracy, similar to that of the first derivative method but improved when compared to the linear extrapolation method. As an advantage this method is not dependent on series resistances of the device. Comparing the results from Figure 3-33 to those in Figure 3-25 a large difference can be observed. The results measured for a current of 0.1mA can be considered too conservative and might lead to overdesign of the gate-driving circuits or excessive slowing down of the device during normal operation in order to ensure parasitic currents flowing through the Miller capacitance would not turn on the device.

3.5.2. DYNAMIC CHARACTERISTICS

Since most power devices application involve clamped inductive switching, it is relevant to investigate the 10kV 10A 4H-SiC MOSFET behavior during such transients. For the inductive clamped switching, the circuit presented in chapter 3.4 was used. The DC-link was set to 60% of the device rating and a gate driving resistance of 3 Ω was used. The resistance was selected as a tread-off between fast switching times and device stability, based on the recommended value from the manufacturer and laboratory investigations. In order to measure the device behavior at elevated temperature, a custom heating element had to be design as the baseplate is soldered to the drain of the chip, thus baseplate temperature measurement and

baseplate heating was not direct. In order to provide insulation for the high levels, DBC used in power module manufacturing was cut and etched to the size of the packaged 10kV 10A 4H-SiC MOSFET. The heating element and temperature measurements where soldered on one side of the DBC while the other side was connected though thermal compound to the baseplate of the DUT, with temperature compensation being performed before testing. As it can be observed from Figure 3-23 at constant temperature, there is no noticeable difference in the $R_{DS,on}$ of the device for a gate voltage of 18V or 20V.

In order to avoid stressing of the gate oxide, as a precaution, V_{GS} was chosen at 18V when the switching behavior was investigated. Figure 3-34 and Figure 3-35 show the turn-on and turn-off waveforms of the 10kV 10A 4H-SiC MOSFET at different temperature for a DC-link voltage of 5kV. The turn-on currents were approximately 5A while the turn off currents where 7A. It can be observed that during turn-on, the ramps of both V_{DS} and I_D become steeper as the temperature increases, while at turn-off the opposite can be noticed. This can be linked with the decrease in threshold voltage and plateau voltage due to an increase in temperature. Since in the case of SiC, the device capacitances have very negligible temperature dependence [97], the plateau voltage variation can be observed from [98]:

$$V_{plateau} = g_{m0}^{-1} \cdot I_D \tag{3.11}$$

As shown in Figure 3-32, the internal transconductance of the device increases

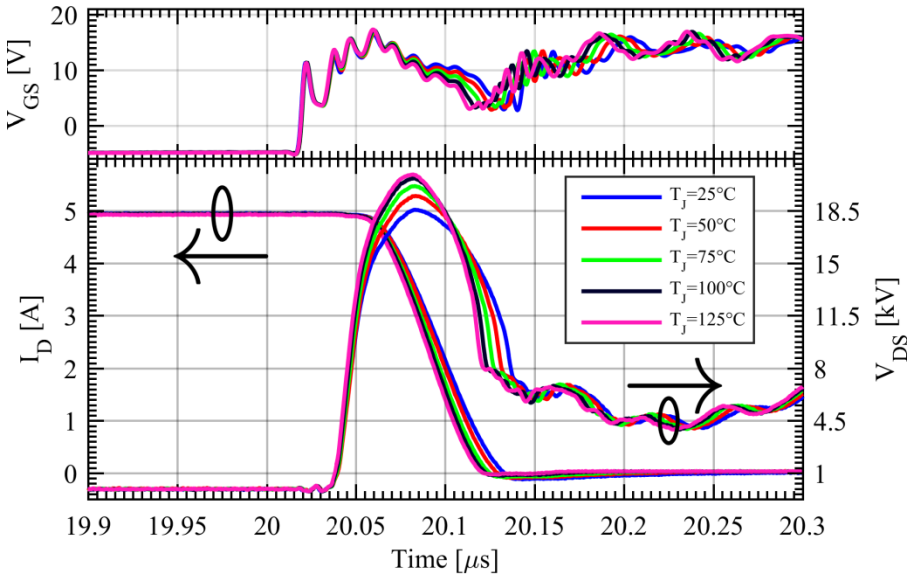

Figure 3-34 Turn-on waveforms for 10 kV 10 A SiC MOSFET at 5 kV 5 A for different junction temperatures

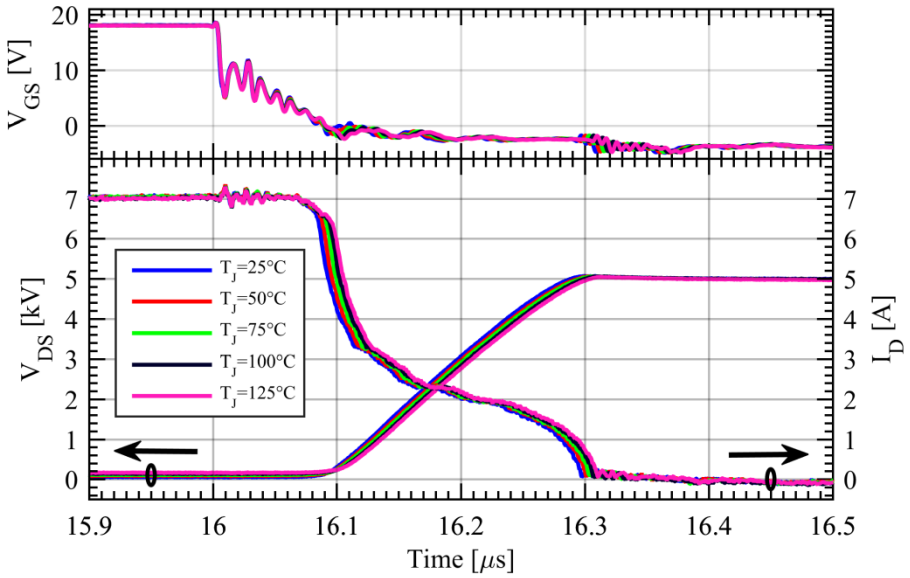

Figure 3-35 Turn-off waveforms for 10 kV 10 A SiC MOSFET at 5 kV 7 A for different junction temperatures

with temperature, resulting in a decrease with temperature in $V_{plateau}$ for a given drain current.

At the same time, an interesting phenomena is observed related to current of the device during the switching transitions. At turn on the current has an overshoot, which would normally be associated with the reverse recovery of the free-wheeling diode in parallel to the inductor as it was shown in Figure 3-6, but as mentioned earlier, the test setup uses a SiC 4H-SiC JBS diode, thus no reverse recovery exists in this case. By observing the turn-off waveforms, the current seems to show an abrupt drop as it would be influenced by a capacitive snubber [99]. Despite the fact that the JBS diode does not show a reverse recovery, the internal parasitic capacitance of the device shows a similar behavior. While the losses in the diode are insignificant, the large capacitance, associated with its large dimensions [100] plays an important role on the losses of the lower device, or in this circuit on the 10kV MOSFET, especially if the operating voltages are considered. This parasitic capacitance of the JBS SiC diode will give rise to an overshoot during turn-on due to the high dv/dt encountered, and during turn off it will aid in the decay of the current in the first part of the transient.

The reduction in the two voltages, V_{th} and $V_{plateau}$ will also result in faster di/dt and dv/dt for the same current and voltage during turn-on but a slower di/dt and dv/dt during turn-off. From the two switching waveforms it can also be observed that during turn-on the delay decrease with temperature while during

Table 3-1 10kV 10A 4H-SiC MOSFET switching characteristics at room temperature [48]

Gate Charge (Q_G)	350 nC
Rise time (t_r)	90 ns
dV/dt (rise rate)	$40kV/\mu s$
Fall time (t_f)	50 ns
dV/dt (fall rate)	$84kV/\mu s$
Turn-on energy (E_{on})	6.2 mJ
Turn-on energy (E_{off})	1.3 mJ

turn-off they increase with temperature. This will show an influence on the device switching losses as the turn-on transients will be accelerated with temperature but the turn-off times will decrease with temperature. As a result the losses will be smaller with temperature during turn-on for the same voltage and current but, during turn-off of an identical current and voltage the losses will increase with temperature.

The main switching characteristics at room temperature for the 10kV 10A 4H-SiC MOSFET for a V_{GS}=18V have been measured at 10A and a DC-link voltage of 6kV and are summarized in Table 3-1.

In order to observe the influence of the gate voltage on the switching behavior of the 10kV MOSFET, the device was characterized at two V_{GS} turn-on voltages of +15V and +18V while the turn-off voltage was kept at -5V. Three different drain-source voltages where used, V_{DS}=4kV, 5kV and 6kV respectively. The

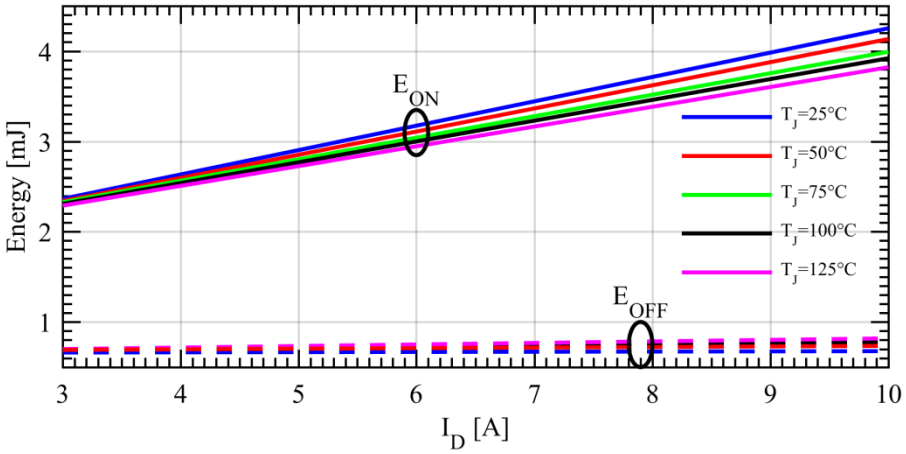

Figure 3-36 Switching losses at V_{DS}= 4 kV and V_{GS}=15 V as a function of temperature and current for 10kV 10A 4H-SiC MOSFET [48]

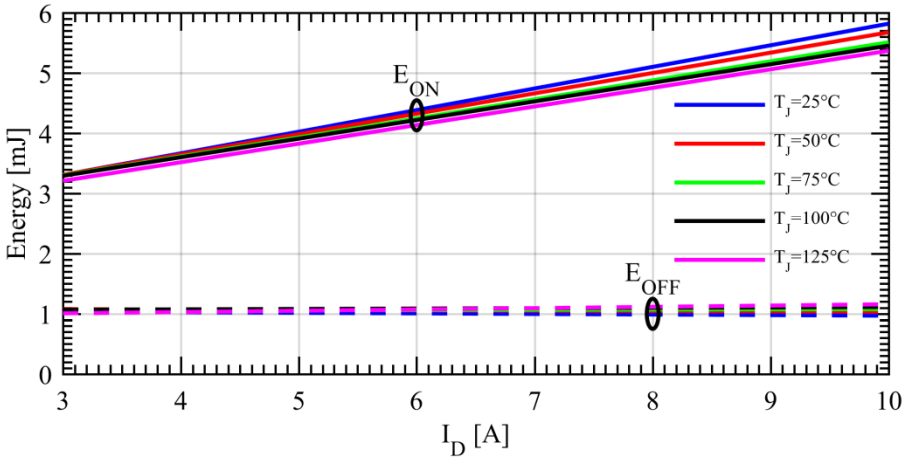

Figure 3-37 Switching losses at V_{DS}= 5 kV and V_{GS}=15 V as a function of temperature and current for 10kV 10A 4H-SiC MOSFET [48]

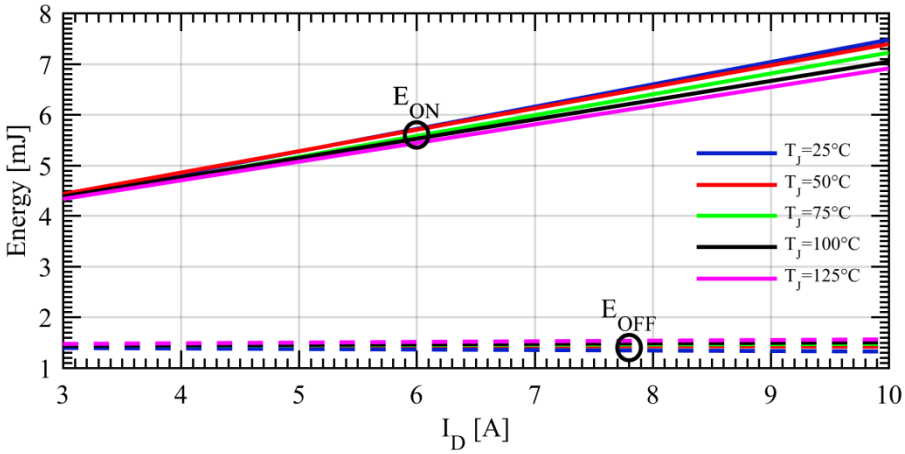

Figure 3-38 Switching losses at V_{DS}= 6 kV and V_{GS}=15 V as a function of temperature and current for 10kV 10A 4H-SiC MOSFET [48]

junction temperature was varied in steps of 25 °C from room temperature up to 125 °C. The switching losses where then calculated for the different gate and drain voltages as a function of temperature and drain currents.

Figure 3-36, Figure 3-37 and Figure 3-38 show the turn-on and turn-off losses at V_{DS}= 4kV, 5kV and 6kV for a V_{GS}=+15V/-5V as a function of temperature and current. As mentioned earlier and observed from Figure 3-34 and Figure 3-35, the turn-on losses are decreasing with temperature for the same voltage and current

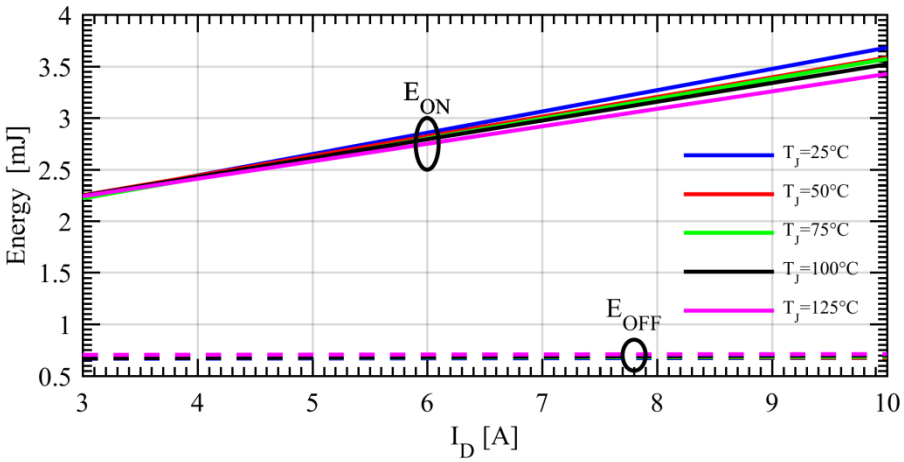

Figure 3-39 Switching losses at V_{DS}= 4 kV and V_{GS}=18 V as a function of temperature and current for 10kV 10A 4H-SiC MOSFET [48]

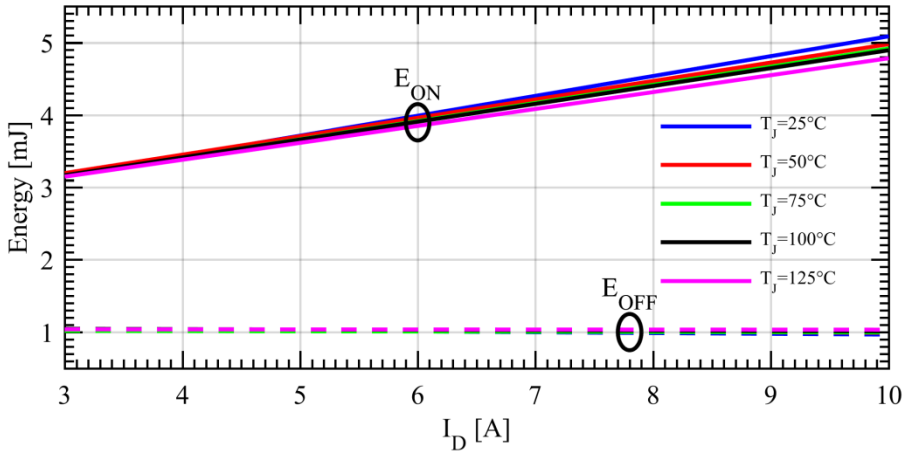

Figure 3-40 Switching losses at V_{DS}= 5 kV and V_{GS}=18 V as a function of temperature and current for 10kV 10A 4H-SiC MOSFET [48]

rating, while during turn-off they are increasing for an identical current-voltage pair.

Figure 3-39, Figure 3-40 and Figure 3-41 Figure 3-38 show the turn-on and turn-off losses at V_{DS}= 4kV, 5kV and 6kV for a V_{GS}=+18V/-5V as a function of temperature and current. As in the case of the lower gate voltage, the turn-off losses seem to be constant despite an increase in temperature while the turn-on losses show an identical behavior.

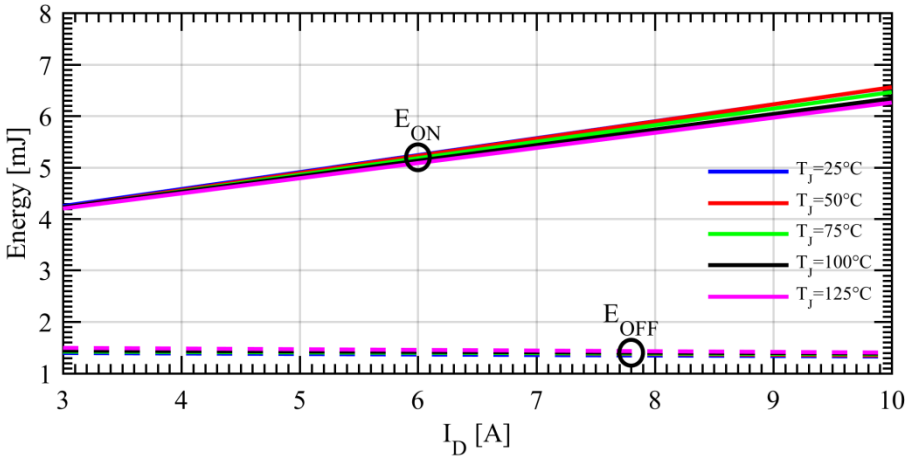

Figure 3-41 Switching losses at V_{DS}= 6 kV and V_{GS}=18 V as a function of temperature and current for 10kV 10A 4H-SiC MOSFET [48]

An interesting observation can be made during turn-off, where the losses are not increasing with current at the same rate as the turn-on losses. As the losses are very small during turn-off, measurement noise can have a high impact on the measured data. Despite this, it can be observed that for a given temperature, an increase in measured drain current does not increase the losses of the device proportionally. This can be explained by the higher current running through the inductor, which during turn-off will aid in charging the device capacitances faster, thus reducing the switching times for a higher current at a constant temperature.

The phenomena can be observed in Figure 3-42 where the device is turn-off at different drain currents while keeping temperature, gate voltage and drain voltage constant. Each color in Figure 3-42 represents the turn-off transient for a different drain current. It can be observed that the higher the current it is, the faster it decays to zero, and at the same time the sharper V_{DS}rises to nominal voltage. Considering the parasitic capacitances of the device C_{GD} and C_{DS} shown in Figure 3-3 and Figure 3-5 need to be charged as the device transitions from conduction to blocking state, the higher current running through the drain terminal will contribute to the charge needed for the transition, thus aiding the device to turn-off faster and decreasing the switching time while keeping the switching losses constant in relation to the drain current.

If the losses between the two gate voltages are compared, the turn-on losses for the higher gate voltage have decreased under similar temperature, voltage and currents conditions. This was an expected behavior as the bias applied to the device gate is higher, allowing for a faster charging of the input capacitance and at the same time increasing the channel mobility. At turn-off, the plots show no difference in switching losses for the same temperature, voltage and current condition because

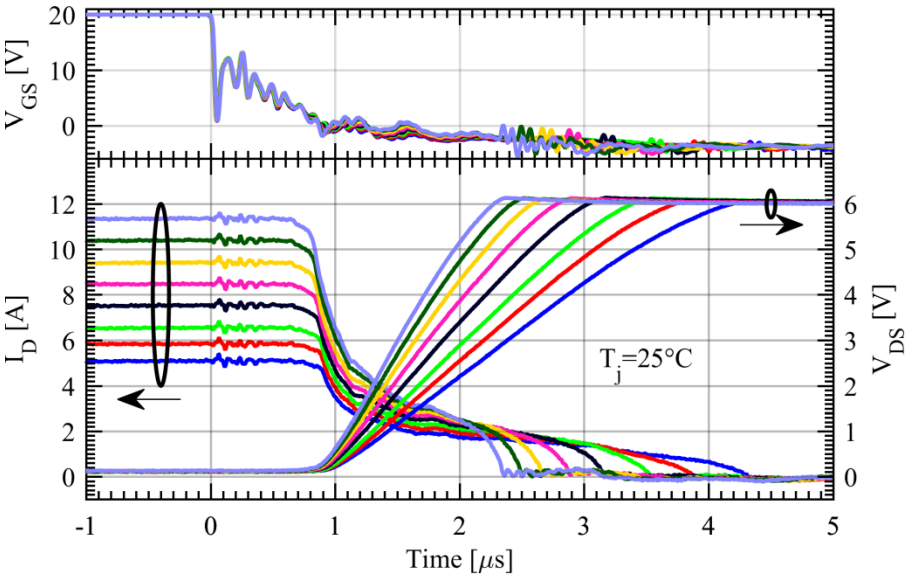

Figure 3-42 Turn-off of 10kV 10A 4H-SiC MOSFET as a function of drain current at room temperature

the same turn-off voltage was used. As explained earlier and shown in Figure 3-42 during this transition the device output capacitance dictates in this case the turn-off speed of the device.

3.6. Summary

In the beginning of this chapter the power MOSFETs was presented and analyzed in simplified manner in order to offer a background for the power SiC MOSFET analysis. The static characteristics of the power MOSFET where briefly presented together with the parasitic components of the device which will influence the behavior of the device during both switching and conduction.

Afterwards the evolution of SiC power MOSFETs during the last 25 years was investigated, starting with the first demonstrated SiC power MOSFET up to current times. Highlighting the big progress research in the manufacturability of SiC power MOSFET has achieved.

Next the test setup designed for the 10kV 10A 4H-SiC MOSFET was described and its inductance and current sharing was investigated in order to validate it. While the circuit does not allow for non-destructive testing or other exotic tests, its low inductance design and simplicity make it ideal for testing the 10kV 10A 4H-SiC MOSFET during different scenarios, from simple switching

behavior as a double-pulse tester, to short-circuit or avalanche breakdown by simply removing or inserting the diode and inductor as needed.

The characteristics of the device were also investigated both during static and dynamic conditions. During the DC-characterization the device showed improvements over the previous attempts at designing a 10kV 4H-SiC MOSFET [71] as the $R_{DS,on}$ of the first generation 10kV 10A 4H-SiC MOSFET showed an overall positive temperature coefficient. While at low gate biases where the channel resistance is dominant the device on-state resistance shows a negative positive coefficient, at high gate biases, where the SiC power MOSFET would normally operate the on-state resistance has a positive temperature coefficient. This would allow the chips to be parallel in high power modules without concerns regarding uneven current sharing. From the DC-characteristics it was also observed that the device behavior for gate voltages above 18V is almost identical. This would allow for the device to be turned on with a gate voltage of 18V instead of the maximum 20V while obtaining the same performance during operation. On the other hand the smaller voltage would allow for a 2V gate oscillation without exceeding the manufacturer maximum allowable gate voltage of 20V. The device channel resistance was also extracted based on measurements at very low V_{DS} in order to limit the influence of the drain bias on the total drain resistance. The "internal" transconductance of the device was also extracted and calculated as the measured "external" transconductance showed a decrease in current which was not correct.

In the last part of the chapter the dynamic characteristics of the DUT where investigated. The device switching performance was investigated at three different drain voltages of 4kV, 5kV and 6kV for two different turn-on gate voltages of 15V and 18V at temperatures ranging from 25°C up to 125°C in steps of 25°C. As expected, the lower gate voltage will increase the device losses as the channel is still limiting the current and contributing to the total on-state resistance.

It was observed that during turn-on the parasitic capacitance of the JBS diode used in the test setup would generate an overshoot in the current due to the high dv/dt experienced during turn-on. Despite this, due to the fast switching capabilities of the device, the losses are relatively small, under 7mJ for a V_{DS}=6kV and I_D=10A.

Moreover during turn-on the device losses decreased with temperature due to a decrease with temperature of the threshold voltage and the plateau voltage. The decrease in the plateau voltage with temperature is attributed to an increase in the internal transconductance of the device with temperature, allowing for the device to be turned on faster for a higher junction temperature while the drain current, drain-source voltage and gate voltage are kept constant.

During turn-off, the losses of the device for a given drain current and drain-source voltage increase with temperature for a given gate voltage. This is related to the same decrease in threshold voltage and plateau voltage as difference between the voltage applied to the gate of the device and the above mentioned voltages is smaller, thus the current which is sinked as the charges in the gate are removed is also smaller. This was also experimentally investigated.

Overall the first generation 10kV 10A 4H-SiC MOSFET showed good DC-characteristics and consistent switching behavior. The device gate-driving requirements are minimal, allowing the end user to obtain fast switching times and high blocking capabilities by using a voltage controlled unipolar device with a basic gate driver instead of complex series connected devices which might require complex current control gate-drivers.

Chapter 4.
Short-Circuit Analysis of 10kV 4H-SiC MOSFETs

In this chapter the short-circuit capabilities of the 10kV 10A 4H-SiC MOSFET will be investigated and the degradation mechanisms associated with the short-circuit will be investigated.

4.1. Introduction

SiC power MOSFETs have potentially better electrical performance than their Si counterparts and are a promising solution for future high power, high voltage the SiC power devices are not yet cost competitive with Si device for same ratings and voltage in the 1.2kV range, they are considered in applications which require high efficiency, compact power converters [4], [101]-[103] under harsh environment which would allow them to operate at high ambient temperature. Similar investigations performed for the 10kV 4H-SiC MOSFETs have shown them to be a suitable replacement for 6.5kV Si IGBTs or series connection of lower voltage Si devices in power applications with high voltage DC-links, where the SiC power device could potentially outperform their competition [39]-[43], [72], [81], [83], [104]-[108].

In order for such devices to be fully considered, the ability to guarantee their reliability and safety is crucial, especially during harsh, abnormal operations and stressful conditions which define their operating condition and might provide helpful design rules and engineering improvements to the end user and to the manufacturer in order to push the device performance boundaries [31], [109], [110]. Nowadays, power semiconductor devices employed in converters are expected to be able to operate for short amount of times outside their designed safe operating area (SOA) during transients. Short-circuit is one of the most stressful events which might be encountered by a power device in a grid connected application and the power devices should show a short-circuit withstand time sufficiently long for the protection circuits to interact and take actions in order to remove the fault, through control of the active device gate signal or though external circuit breakers.

Since SiC unipolar power devices with voltage ratings above 10 kV have only been available since 2004 [70], to the authors knowledge, up to the time of the writing no prior investigations into the short-circuit behavior and degradation of such devices has been published.

The research in the field has instead focused on commercially available 1.2kV 4H-SiC devices and their behavior and degradation during short-circuit events. Despite the fact that the devices ratings are different, the manufacturing process is similar, thus insights from the lower voltage devices could contribute to a better understanding of the behavior of 10kV 4H-SiC MOSFETs during short-circuit events.

4.2. Overview of the short-circuit behavior in 4H-SiC MOSFETs

In recent year, in the case of 1.2 kV SiC MOSFETs, research has been carried out on the reliability and robustness of SiC devices under short-circuit transients.

The main investigation is focusing on hard-switching faults where the device turns on and goes into short-circuit with the full DC-link voltage applied across its power terminals. This type of fault is encountered in all inverter applications and is associated with a gate driver fault in a half-bridge configuration, where one device remains one while the other one switches, leading to the full DC-link energy being discharged across the device which is turning on.

In [34], [111]-[114] the authors investigate the behavior of 1.2 kV SiC unipolar power devices during short-circuit events. The devices show good performance during the transient with short-circuit withstand time up to 80 µs, but the studies cannot be fully considered as they do not represent real life applications scenarios due to the selected testing conditions, which range from too small DC-link voltages, under 400 V or smaller, to incorrect gate-source voltages, 10 V-15 V. In this case a DC-link voltage of at least 600 V would be required and a gate-source voltage similar to the real life applications should be used. At the same time, the main advantage of the SiC devices is their fast switching times, which would determine a system designer to use the maximum allowable turn-on voltage, generally 20 V, when turning on the device, in order to have a very fast turn on in power electronics applications.

One of the main failures found during short-circuit for such devices has been attributed a failure of the gate oxide [31], [34], [112]-[121]. One key advantage of SiC MOSFETs is related to the high electric field ratings of the gate oxide, which at the same time is a naturally occurring oxide for SiC, making this part of the fabrication easier [75], [115]. This high electric field rating allows for the design of very fast unipolar power devices which will in terms allow for lower switching frequencies [115], [122]. Considering that the gate oxide is generally in the 50 µm-100 µm thick [75], [123] and has a oxide field rating in the range of 4-6 MV/cm, in order to maintain good reliability and lifetime of the device, the maximum field experiment by the oxide should be limited. In the case of Si NMOS devices, for ten year lifetime expectancy, the gate oxide field is limited to 4-5 MV/cm [75]. Full

studies regarding this problem can be found in [75], [123].Since SiC devices have a low channel mobility a high inversion channel is desired, at the same time, for the typical oxide thickness, the electrical field in the dielectric ranges between 2-4 MV/cm, thus the gate oxide is susceptible different defects associated with the high electric fields experienced by it, such a tunneling, interface states, and charge traps especially when operating at high junction temperatures. This becomes even more concerning, when the device will turn on with a large bias across the drain-source terminals, which will create an even large electric field across the gate dielectric. The studies analyzed the reliability of the gate oxide during short-circuit transients and observed an increased gate leakage current after systematic stressing which would leak to an eventual loss of gate control, where the gate would short to the source terminal [117], [119]-[121], thus losing the control of the device, in a non-destructive manner, or shorting of the gate to the drain terminal [121], which would suggest a complete failure of the device structure.

Another failure mechanism during short-circuit was associated to thermally generated leakage currents. Due to the increased temperatures inside the device during short-circuit transient, electro-thermal runaway of the device or even destructive leakage currents after turn-off could be observed [112]-[114], [116], [118]-[121]. This is observed as an increase in current towards the end of the short-circuit pulse or, more often, as tail currents during turn-off. It is the result of two concomitant phenomena, on one hand carrier mobility in the channel and drift region decrease with temperature and leakage current generated by thermally induced impact ionization. The main contributors to the device leakage current are: thermally generated currents [124], diffusion currents [3], [125], [126] and avalanche multiplications currents [127]-[129]. A full discussion regarding leakage currents in 1.2 kV 4H-SiC MOSFETs can be found in [119].

In some studies [34], [113], [114], [116]-[118], [130], the degradation of SiC devices has been noted after prolonged or cyclic short-circuit pulses, presented as a peak short-circuit current decrease, linked to an increase in the device's measured on-state resistance and, as a consequence of the localized heating on the surface metalization, reconstruction of the aluminum metalization on the source side. The main reasons for the decrease in the conduction capabilities of the devices, were associated mainly with degradation of the gate and changes in the threshold voltage, mainly attributed to, among others, charge and interface traps SiO_2/SiC interface. For the surface aluminum reconstruction and degradation, as the most plausible solution, current crowding on the surface was given. None the less, the majority of the studies performed on 1.2 kV SiC MOSFETs agreed that the temperature during the short-circuit transient is the most important factor in the degradation and failure of SiC devices during short-circuit.

Figure 4-1 shows a theoretical representation of the observed short-circuit

waveforms in the case of 1.2 kV devices [31], [34], [112]-[121], [123]. The short-circuit event can be split up in five stages and are going to be explained in a simplified manner bellow [119].

Stage 1, from t_1 to t_2: the device is turned at the chosen DC-link voltage and the currents ramps up rapidly due to the, ideally, low inductance design of the test setup. The device switches from the linear region to the saturation region due to the very high V_{DS} experienced by the device. The current keeps increasing due to the positive temperature coefficient of the channel up to a temperature of

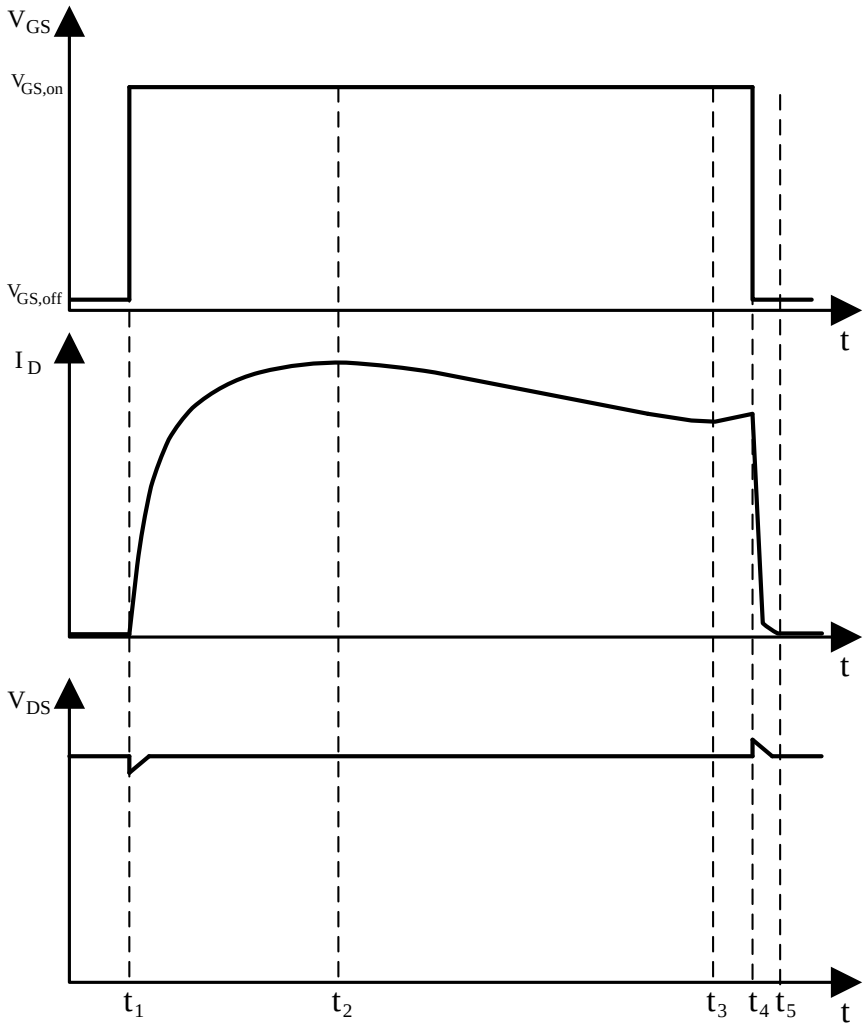

Figure 4-1 Theoretical short-circuit behaviour observed in 1.2 kV 4H-SiC MOSFETs

approximately 600 K [127] and at the same time a decrease in device threshold voltage with temperature. As the device is supporting the full DC-link voltage and the saturation currents reaches values twenty times larger than the nominal current, a considerable amount of energy is dissipated in the device.

Stage 2, from t_2 to t_3: The device is in saturation while sustaining the full DC-link voltage. The temperature inside the device continues to increase due to the increased power loss. As the temperature has surpassed 600 K, the carrier mobility in the device starts to decrease, thus, the saturation current starts to decrease with time. Despite the fact that the threshold voltage is still decreasing, its impact is smaller than that of the decreasing mobility. Electron saturation velocity has also been shown to decrease with temperature, mainly due to phonon [131], [132]. The device could still be turned-off safely in this interval, if the temperature inside the device has not reached critical levels.

Stage 3, from t_3 to t_4: At this point the temperature inside the device has given rise to the before mentioned leakage currents generated by the thermally induced impact ionization. The slope of the device saturation current becomes positive as the decrease as the impact of the decreasing mobility is smaller than that of the leakage currents. This is an optional stage and most of the times will lead to a destruction of the device after turn-off, similar to the one reported in the case of Si IGBTs in [133].

Stage 4, from t_4 to t_5: At this point the device is switched off and tail currents appear as the current decreases to zero. The tail currents are given by the high leakage current in the device, same ones that generated the change of slope in stage 3. If stage 3 was not present during short-circuit the temperature inside the device might still be within safe limits and the device might survive the turn off, on the other hand, the presence of stage 3 will most of the times result in a destruction of the device.

Stage 5, from t_4 onwards: The device turns off, and depending on the temperature inside the device, the device might go into thermal runaway and fail or safely survive the short circuit. The presence of stage 3 and magnitude of the tail currents in stage 4 are a tell sign of the device survivability.

4.3. Maximum short-circuit withstand capability of 10kV SiC MOSFETs

Short-circuit analysis of the 10 kV device is highly relevant, both in order to assess the requirements of the protection circuits which need to be developed in order to protect the device from short-circuit but also in order to gain insight into the failure mechanisms of the device.

Similar to the investigation performed in [120] and [121] for the 1.2 kV 4H-SiC MOSFETs, the 10 kV 10 A 4H-SiC MOSFET was investigated in order to observe its maximum short-circuit withstand time and the full results were presented in [30]. The opinions regarding the testing procedure for the maximum short-circuit withstand time are split between two different testing procedures: single pulse until device failure or increasing length repetitive pulses until device failure. While the first case is more widely used and ensures the device is not degraded before failure, the failure times give a false approximation of the maximum failure time, because there are no guarantees of what the device is capable of safely turn off. And this would require subsequent single shot test on new devices in order to properly determine the maximum short-circuit time. The second testing procedure provides a more conservative value for the maximum short-circuit withstand time. This is due to the device degradation in the increasing length pulse before failure. An advantage of this testing procedure is due to the fact that after a single investigation, a conservative estimation of the maximum short circuit time can be obtained. In the case of the 10 kV 10 A 4H-SiC MOSFET the second testing procedure was chosen as cost associated with the device and packaging it would make it unfeasible to test multiple devices for the study.

The 10 kV 10 A 4H-SiC MOSFET was placed in the test circuit presented in chapter 3.4 after the inductor and diode where removed, as shown in Figure 4-2 and the DC-link voltage was set to 6 kV. The gate voltage during the short-circuit was chosen at V_{GS}=+18V/-5V in order to ensure that the gate oxide will not get affected in case the gate driver will malfunction and overshoot the maximum allowable gate voltage, V_{GS}=+20V. At the same time, based on the measured I-V characteristics of the device, the different between the chosen gate voltage and the maximum allowable gate voltage shows only minor variations in the current.

Because no previous investigations for such a device have been presented until now in literature, and in order to observe the behavior of the device during different length of the SC, the initial width of the pulse was chosen at $t_{SC,init}$= 500 ns. This

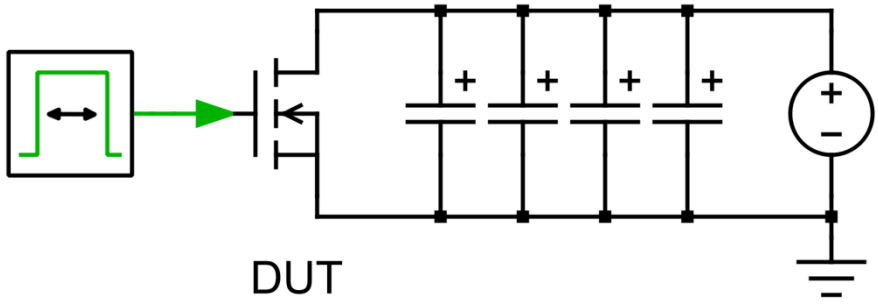

Figure 4-2 Simplified test setup schematic for short-circuit investigation [89]

ensures the device has sufficient time to turn on. Afterwards the pulse width was increased in steps of 100 ns until catastrophic failure was observed. A break of approximately 3 minutes was allowed between each pulse in order to ensure the device cooled down.

In order to aid the reader all the measured pulses for the investigation are shown in Figure 4-3. As it can be observed, during the entire study, the gate voltage remains stable during the entire investigation. Since the V_{GS} waveforms look identical and no variation can be observed, in future plots they will not be included, in order to simplify the figures. At the same time V_{DS} looks stable through the entire investigation. The length of the V_{GS} pulse for each of the pulses in the waveforms can be calculated by multiplying the pulse number with 0.1 μs and then adding 0.4

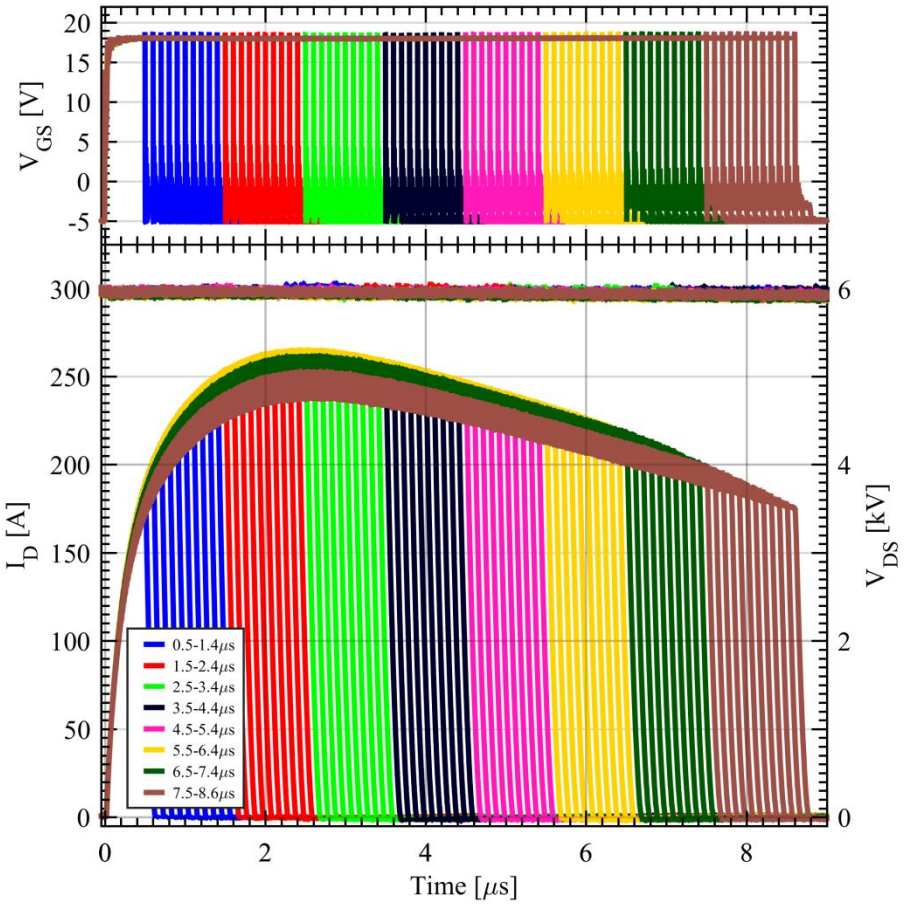

Figure 4-3 Evolution of V_{GS}, V_{DS} and I_D during maximum short-circuit capability investigation.The figure shows all the 82 pulses of the investigation overlapped in order to highlight the evolution of the current in relation to the pulse number

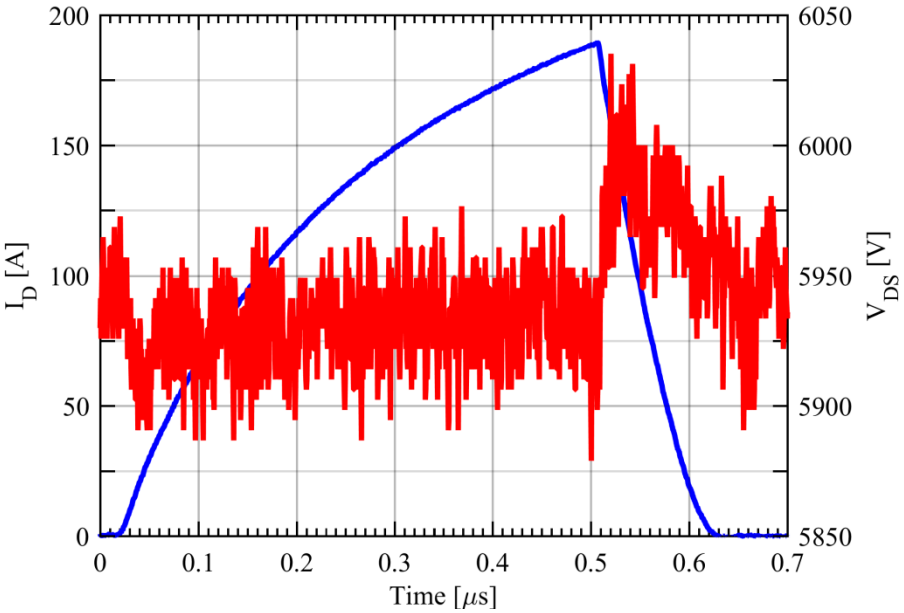

Figure 4-4 10 kV 10 A SiC MOSFET current and voltage waveforms for pulse 1 (500 ns) short-circuit at a $V_{GS} = +18\ V\ /\ -5\ V$ [30]

µs to it.

Figure 4-4 shows the waveforms for the first pulse in this investigation. The current rises up to 190 A before the MOSFET is turned off and the total short-circuit energy for the pulse is 0.42 J. Compared to classical Si devices, which have a saturation current during short-circuit 3-5 times higher than their nominal rating, the saturation current in the case of the 10 kV 10 A 4H-SiC MOSFET is 20 times larger than the nominal rated current. This could be explained by a derating of the device performance due to thermal management considerations. The device was only in the first stage of the short-circuit (Figure 4-1) during the short-circuit pulse.

Figure 4-5 shows the 20th, 55th,81st and 82nd pulses during the investigation in relation to the 1st pulse. Pulse 20 represents the maximum peak saturation current of the device (266 A) reached at the end of stage one of the short-circuit (Figure 4-1). Subsequent pulses with longer length will enter the second stage of the short-circuit. The short-circuit energy of pulse 20 was 3.24 J.

After the 55th pulse the device started showing aging and degradation as a decrease in peak saturation currents. The pulse shows a change in sign of the saturation current ramp, di/dt. While in stage one the 10 kV 10 A 4H-SiC MOSFET current showed a positive temperature coefficient, after it passed 2.4 µs, the short-circuit current started decreasing. This change is current shape has been

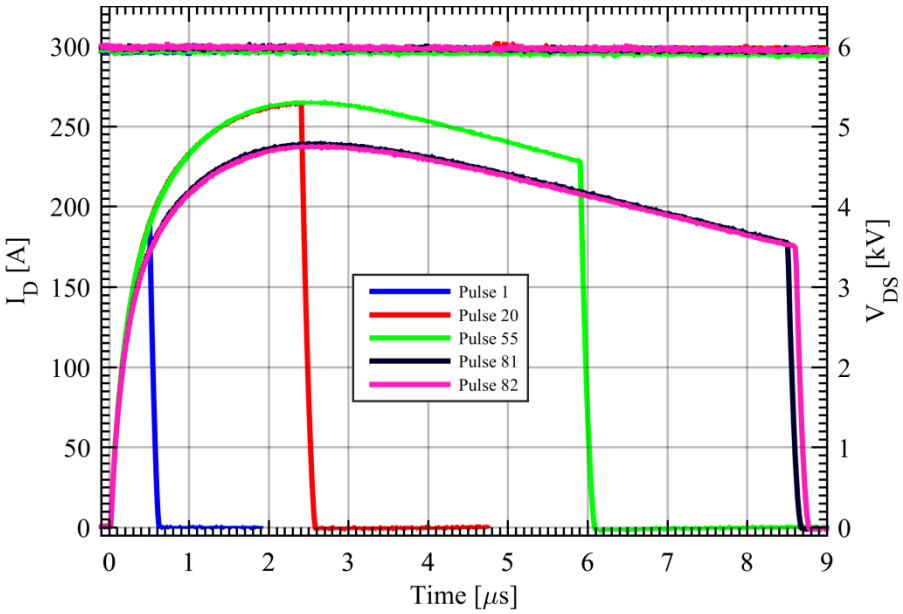

Figure 4-5 10 kV 10 A SiC MOSFET current and voltage waveforms short-circuits at a $V_{GS} = +18\ V\ /\ -5\ V$: pulse 1 (500 ns), pluse 20 (2.4 µs , pluse 55 (5.9 µs) , pluse 81 (8.5 µs) and pluse 82 (8.6 µs)

observed in the low voltage 1.2 kV 4H-SiC MOSFETs. The rising characteristics of the current can be attributed to the increasing temperature of the device due to the large short-circuit energy. Up to a junction temperature of approximately 600K the mobility of the device especially in the MOS channel, but also in the bulk region, will increase [34], [116], [117], [119], [127], [132], allowing for the device resistance to decrease. At the same time the threshold voltage has a positive temperature coefficient as shown in chapter 3.5.1 [34], [119]. As the MOSFET surpasses 600 K, when the saturation current reaches its peak, in enters the second stage of the short-circuit and the current starts showing the negative temperature coefficient. This can be explained by the decrease of the mobility in the MOS channel and drift regions with temperature increase [34], [117], [119], [127], [132]. At the same time the electron saturation velocity starts decreasing with temperature, mainly due to phonon scattering [131], [132]. The threshold voltage is still decreasing with the increase in temperature, but its influence on the saturation current is much smaller than that of the other two mechanisms.

Pulse 81 shows a decrease in peak saturation current down to 239A. This is the last pulse the device could safely turn-off while supporting a V_{DS}=6 kV, despite the obvious degradation of the device.

Pulse 82 was the last pulse in the study of the maximum short-circuit

withstand time. The device was turned off after 8.6 µs, and failed after turn-off, exploding. This made impossible the post-degradation analysis of the device.

4.3.1. THERMAL MODEL AND SIMULATION OF 10 KV 10 A 4H-SIC DURING SHORT-CIRCUIT

Investigations into the short-circuit behavior of lower voltage 4H-SiC MOSFETs have shown that during short-circuit, the generated heat flux does not propagate all the way to the drain terminal of the device [119]. In order to evaluate the evolution of temperature in the 10 kV 10 A 4H-SiC MOSFET during short-circuit pulses, a 1-D, time dependent, thermal simulation was implemented in COMSOL FEM solver to observe how the temperature propagates in the device [89]. The model for the short-circuit investigation considers a 1 mm copper substrate, a thin layer of SAC 305 solder layer on top, 0.5 mm SiC MOSFET chip with a 5 µm aluminum surface. A layer of silicone gel was added to the top in order to mimic the actual device. The dissipated power measured during short-circuit experiments was modeled as a heat source with a triangular profile, similar to that of the electric field in the device. As to simplify the simulation, the temperature was averaged in three distinct regions: 1) the aluminum metalization layer on top of the device; 2) the region at the top of the SiC chip where the short-circuit energy is dissipated based on the electric field, as it was discussed in [112], [114], [118], [119], [130]; and 3) the remaining volume of the SiC chip.

Figure 4-6 shows the simulated average temperature profiles in the three

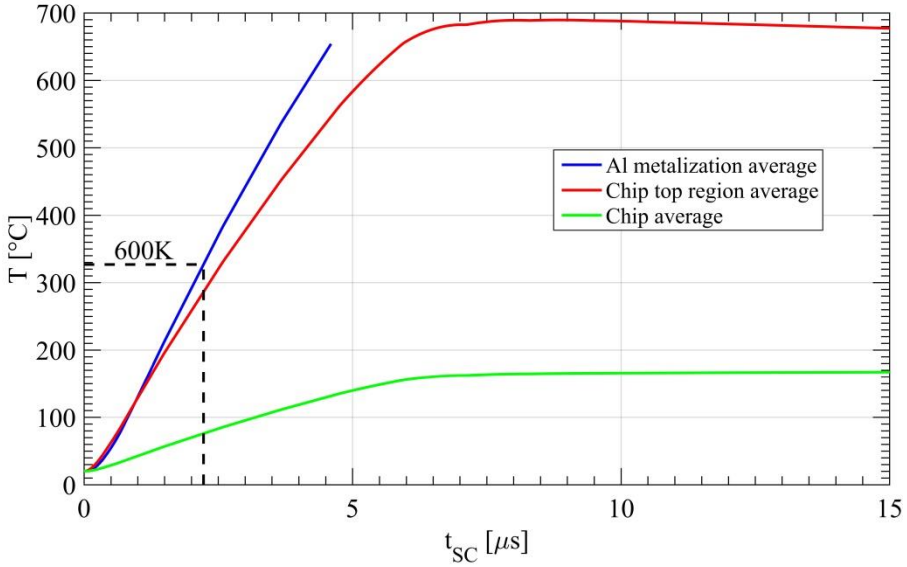

Figure 4-6 Temperature profile of the volumes in the device for the 55th pulse during the investigation

above mentioned volumes of the device during the short-circuit. Because the simulation assumes all the materials in the device are solid, the aluminum metalization average temperature above its melting temperature (660 °C) has been cropped. On the graph, the 660 K value at which the mobility in the device was found to change from positive temperature coefficient to negative temperature coefficient has also been marked [119], [127]. The peak temperature in the chip top region reached 689 °C, and the aluminum reached its melting point before the short-circuit pulse ended, at 5.9 µs. This was the last pulse before the device started showing degradation signs in the peak saturation current.

Figure 4-7 shows the simulated temperature profiles in the 10 kV 4H-SiC MOSFET during the 81st short-circuit pulse, the last pulse that the device managed to safely turn-off. The degradation of the device and decrease in peak saturation current during short-circuit can also be observed in the ramp of the simulated temperature profiles. There is an observable increase in the time needed for the aluminum metalization layer to reach its melting point, but as the pulse was longer, the peak temperature of the chip top region reached 831 °C.

The simulated temperature during the last pulse of the short-circuit investigation is shown in Figure 4-8. The peak simulated temperature of the chip top average reached a temperature of 851 °C. The chip body average temperature reached 200 °C and the aluminum reached its melting point at the same time as the

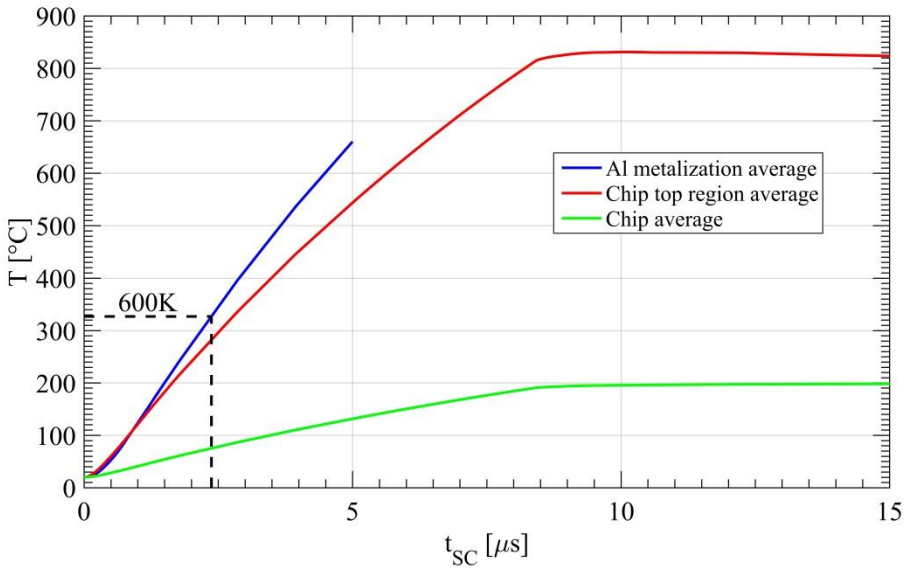

Figure 4-7 Temperature profile of the volumes in the device for the 81st pulse during the investigation

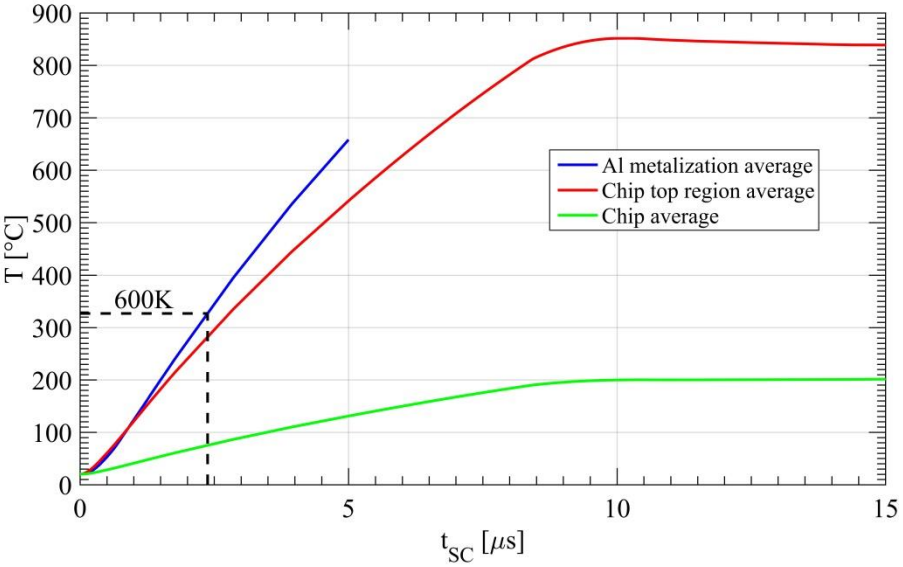

Figure 4-8 Temperature profile of the volumes in the device for the 82nd pulse during the investigation

previous pulse.

Overall, the thermal simulations show that the simulated temperatures inside the device exceed the maximum allowable junction temperature of 175 °C from the first few microseconds. Based on the simulation, the mobility change in temperature coefficient seems to happen also around 2.4 µs. The similarity between the thermal model and the observations in literature seems to support the thermal simulations.

4.4. Investigation of degradation during short-circuit in 10kV-SIC MOSFETs

Since the degradation and failure of the device are of high interest in order to improve and better understand the device, a new study was done in order to evaluate the cause of the reduction in device peak current during short-circuit. Because the initial study which investigated the maximum short-circuit withstand capability was destructive, and no intermediate measurements of the device were performed in order to observe the failure, the new study was planned in order to allow for a better identification of the structure degradation, and if possible, to identify the cause of the degradation. The full study has been published in [89].

While testing more devices in a similar manner represent good practice, due to the scarcity of the 10 kV 10 A 4H-SiC MOSFETs and the associated costs of

packaging and fabricating the device, only a single device was used for the following investigation.

The testing procedure is similar to the one in the previous chapter, where the device is shorted across the capacitors for a time varying from 0.5 µs up to 7.5 µs in steps of 0.1 µs. A break of at least ten minutes between each short-circuit even was allowed in order for the device to cool down and the setup to be reinitialized. As the gate voltage measurements in the previous investigation showed no variation in the gate voltage and the gate driver showed a clean output voltage with no overshoots, the turn-on gate-source voltage was increased up to the maximum allowable gate voltage, of 20 V.

Initially the device was fully characterized in the B1506A curve tracer at room temperature in order to obtain a reference for the unstressed device and to be used as comparison throughout the investigation. The devices was also fully characterized, at room temperature, periodically throughout the test in the curve tracer, initially every tenth short-circuit event, and towards the end, every fifth short-circuit even in order to observe degradations in the different regions of the 10 kV 10 A 4H-SiC MOSFET as the degradation rate increased. Visual inspection was also performed when the device was placed in the curve tracer in order to observe any degradation on the device surface metalization.

In order to simplify the explanation the investigation was split into eight test cycles, representing the tests performed between each characterization. Test cycle zero defines the initial characterization of the device before it was stressed.

Figure 4-10 shows the eight test cycles, containing all the short-circuit pulses performed throughout the investigation. A full characterization at room temperature was performed after the last pulse of each test cycle. Between each test cycle a break of twelve hours was allowed in order to ensure any degradation observed in the device is permanent, and not temporary as reported in [31].

Because the gate-source voltage waveforms show no variations, they will not be included in future figures, in order to simplify the plots.

The first pulse of the investigation had a length of 0.5 µs and the waveforms acquired during the short-circuit are shown in Figure 4-9. The peak saturation current reached 201 A. Considering the same pulse length in the previous investigation, the 2 V higher gate voltage in this investigation yielded an increase of 11 A in peak saturation current for the first pulse. The drain-source voltage showed good stability also in this case.

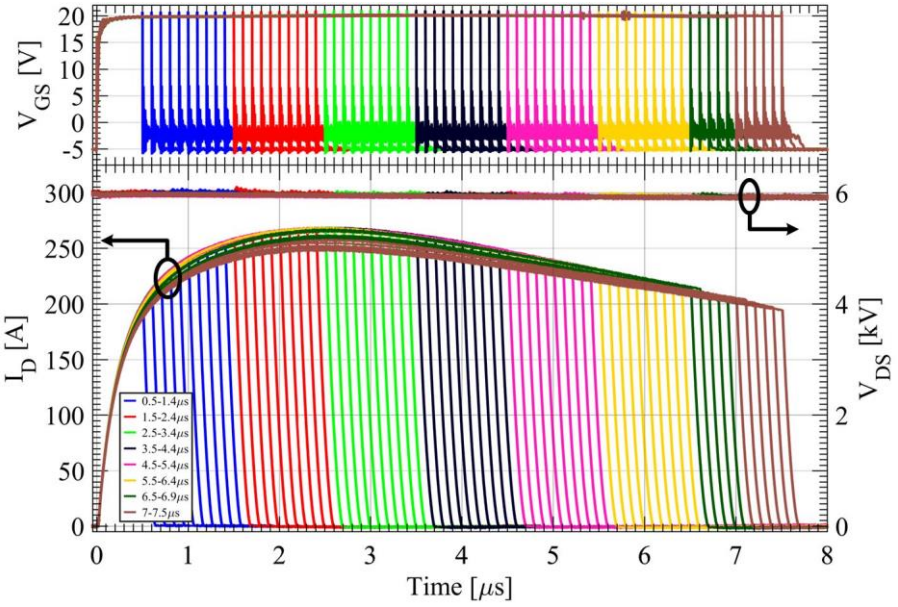

Figure 4-10 Evolution of V_{GS}, V_{DS} and I_D during the study. Each color represents the waveforms associated with the eight test cycles of the study.[89]

Figure 4-11 displays the waveforms associated with the 10th, 20th, 30th and 40th in reference with the 1st pulse of the investigation. After these pulses a characterization was performed, but no degradation was observed. The peak saturation current during short-circuit, of 269 A, for this investigation was reached during pulse 20, with a length of 2.4 µs. As the pulse length increased above 2.4 µs,

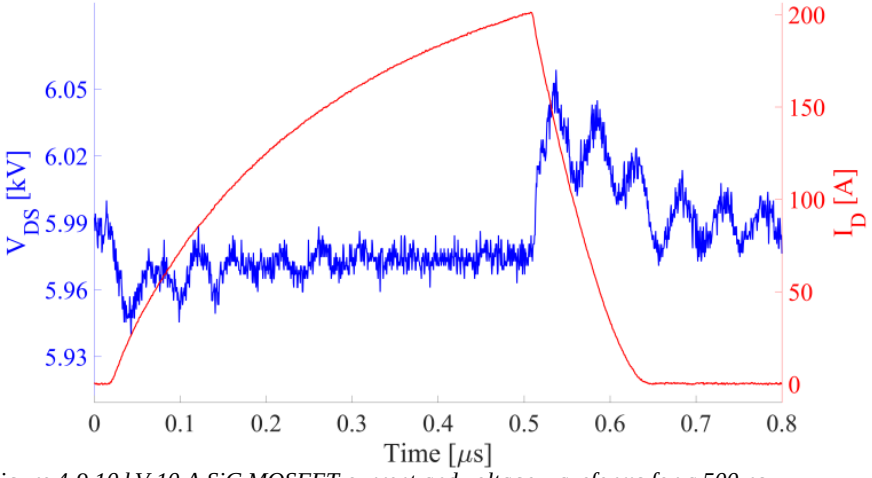

Figure 4-9 10 kV 10 A SiC MOSFET current and voltage waveforms for a 500 ns short-circuit [89]

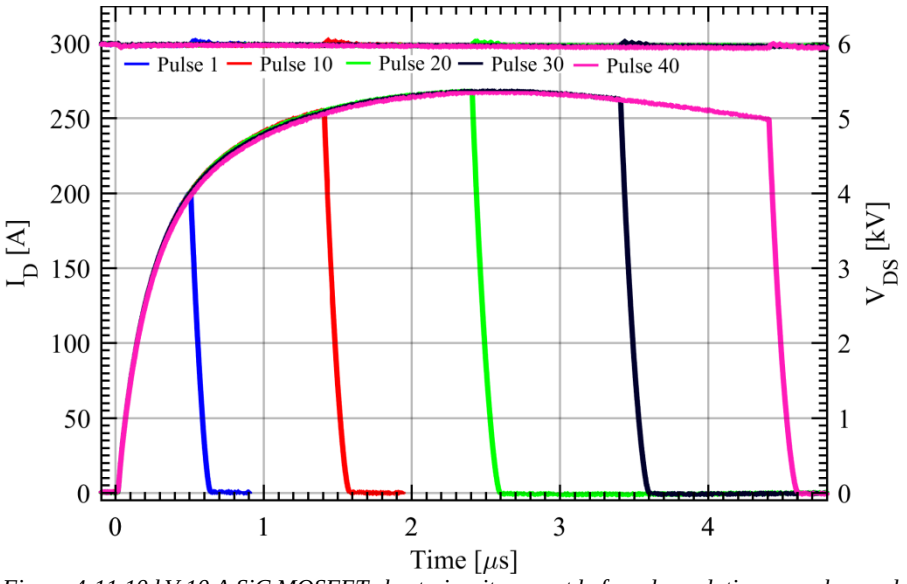

Figure 4-11 10 kV 10 A SiC MOSFET short-circuit current before degradation was observed for different SC pulse length [89]

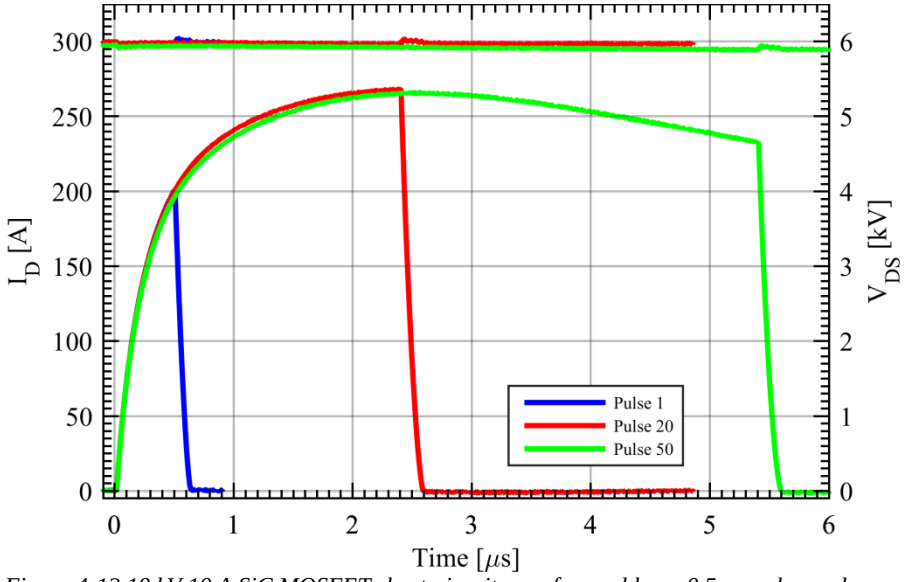

Figure 4-12 10 kV 10 A SiC MOSFET short-circuit waveforms; blue – 0.5 µs pulse, red – 2.4 µs pulse, light green – 5.4 µs pulse [89]

the current changed the temperature coefficient and started to decrease with time due to the internally generated heat, as explained earlier in chapter 4.2. Observing the figure, no degradation can be observed in the current waveforms for the different pulse length, as they overlap.

In Figure 4-12, with light green, the 50th pulse is shown with a peak saturation current of 266.5 A. This was the first sign of degradation observed in the peak saturation current during the short-circuit. The degradation measured was approximately 3A or a bit over 1%. The first and 20th pulse are also included in the figure in order to aid the observation of the degradation in peak current. After this pulse a full characterization was performed, but the variations in electrical parameters were negligible.

Figure 4-13 shows the recorded waveforms for the 60th, 65th, 71st pulses and as a reference the 1st and 20th pulses in order to aid in the observation of the degradation. Each of the 3 pulses are the last one in their cycle, thus a full characterization was performed after them. Pulse 60 had a length of 6.4 µs and a peak saturation current of 266 A. For the 65th pulse, the decrease in saturation current was more evident, with a peak of 275.8 A for a pulse length of 6.9 µs. Pulse 71 was the last one in the investigation, as the short-circuit energy, pulse length and degradation in the peak current were approaching the device limits observed earlier. Its peak saturation current decreased to 248.8 A.

4.4.1. DEVICE DEGRADATION ANALYSIS

4.4.1.1 Degradation observations in the electrical parameters

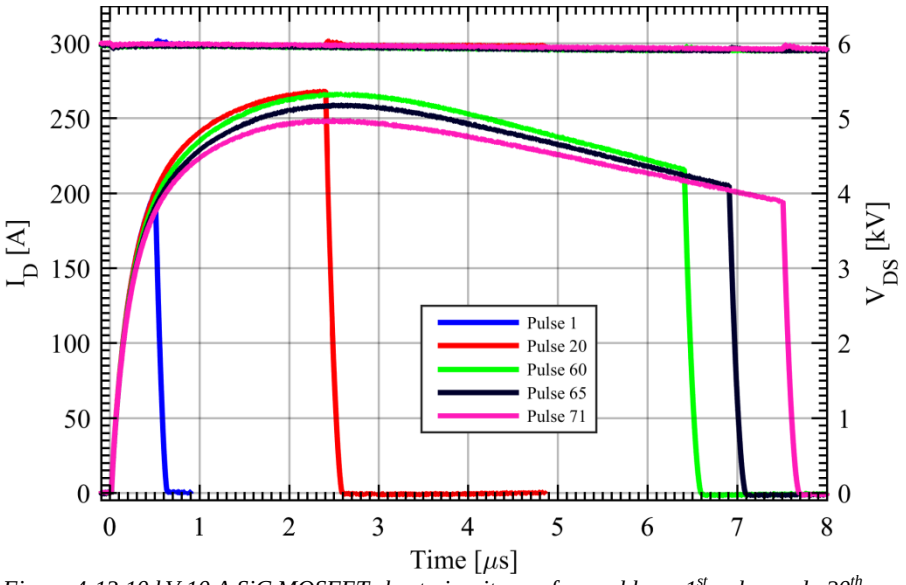

Figure 4-13 10 kV 10 A SiC MOSFET short-circuit waveforms; blue – 1st pulse, red –20th pulse, light green – 60th pulse, black – 65th pulse, pink 71st pulse [89]

Table 4-1 Measurement and degradation summary [89]

Test cycle	Pulse numbers	Pulses length [µs]	Peak I_{Dsat} during interval [A]	Characterization data observation
0	0	0	0	OK (reference)
1	1-10	0.5-1.4	258.4	OK
2	11-20	1.5-2.4	268.2	OK
3	21-30	2.5-3.4	268.4	OK
4	31-40	3.5-4.4	267.9	Small increase in R_{ch}
5	41-50	4.5-5.4	266.2	Small increase in R_{ch}
6	51-60	5.5-6.4	266.1	Increase in R_{ch}
7	61-65	6.5-6.9	257.8	Increase in $R_{DS,on}$
8	66-71	7-7.5	248.8	Increase in R_{ch}

Table 4-1 summarizes each test cycle, and the variation in the electrical parameters observed in the device after each full characterization. This should allow an easy correlation between pulse length, peak current, pulse number and observed degradation in electrical parameters. The zero test cycle is used as a reference against which, each next characterization is compared in order to identify deviation in the electrical parameters. Some of the data acquired during the characterization is extensive and sometimes measured parameter variation can be redundant. In order not to confuse the reader, only the relevant variation in parameters will be presented.

4.4.1.1.1 Device resistance variation

Figure 4-14 shows the I-V measurements performed periodically at the end of each test cycle at a gate-source voltage of 7 V. At this voltage, the R_{ch} is dominating the device on-state resistance, so any variation in $R_{DS,on}$ will mainly be attributed to the channel region resistance, allowing for identifying degradations in the channel resistance.

As it is difficult to observe the data variation in Figure 4-14, different drain-source voltage values have been selected, and the current variation for those voltages throughout the test has been summarized in Figure 4-14. By observing the figure the first slight variation in the current carrying capability of the device, at different drain biases for a V_{GS}=7 V, starts after the fourth test cycle, with a minor increase in $R_{DS,on}$, which would translate in a small degradation of the channel resistance. This was also observed in the peak saturation current during short-circuit during the 50th pulse, where a small decrease in the peak was observed.

The degradation becomes more evident in the channel resistance after the sixth test cycles and continues through the rest of the characterizations, showing a

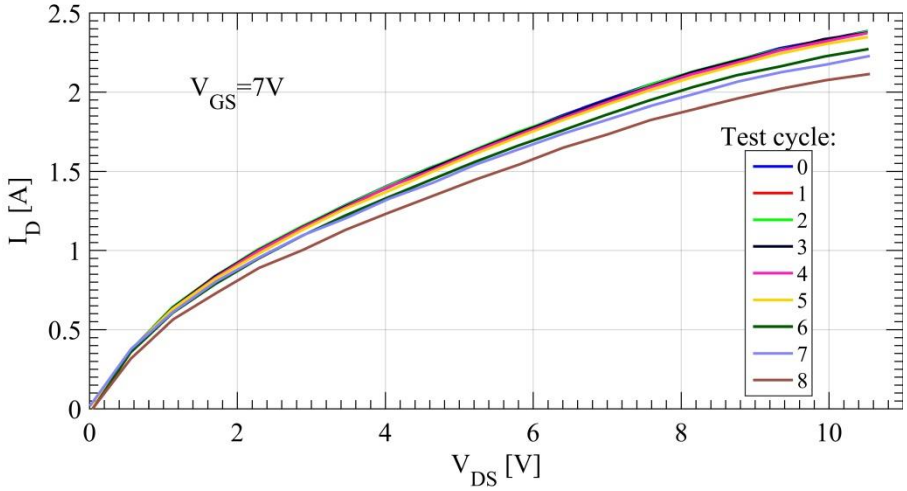

Figure 4-14 Degradation in the I-V measurements of 10 kV 10 A SiC MOSFET after short-circuit stressing for a V_{GS}=7 V [89]

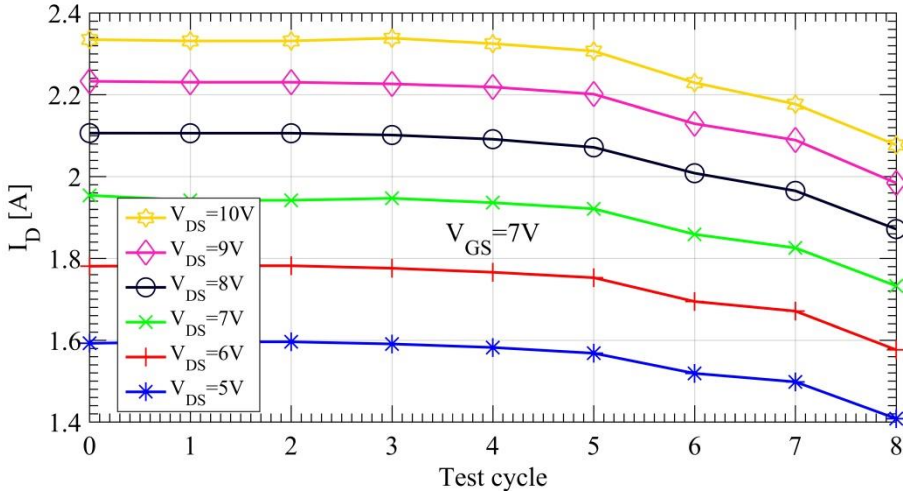

Figure 4-15 Detail of the degradation in the I-V measurements of 10 kV 10 A SiC MOSFET after short-circuit stressing for a V_{GS}=7V observed at different drain-source voltages [89]

systematic increase in the channel resistance, which was shown to be permanent, as it did not recover even after a twelve hour break.

After observing variations in the device channel resistance, the residual resistance can be investigated. The main regions of the residual resistance which can get affect and degraded during short-circuit are the source aluminum metalization, JFET region and drift region. This would be seen as a variation in the

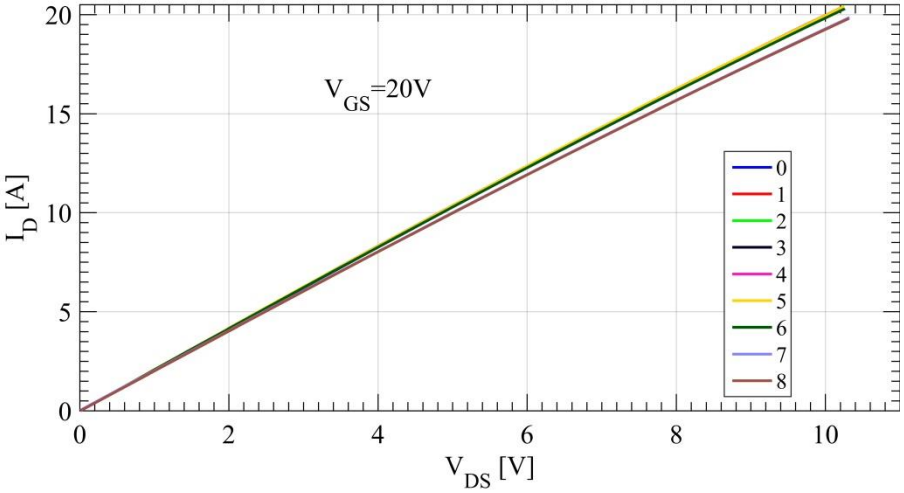

Figure 4-17 Degradation in the I-V measurements of 10 kV 10 A SiC MOSFET after short-circuit stressing for a V_{GS}=20 V [89]

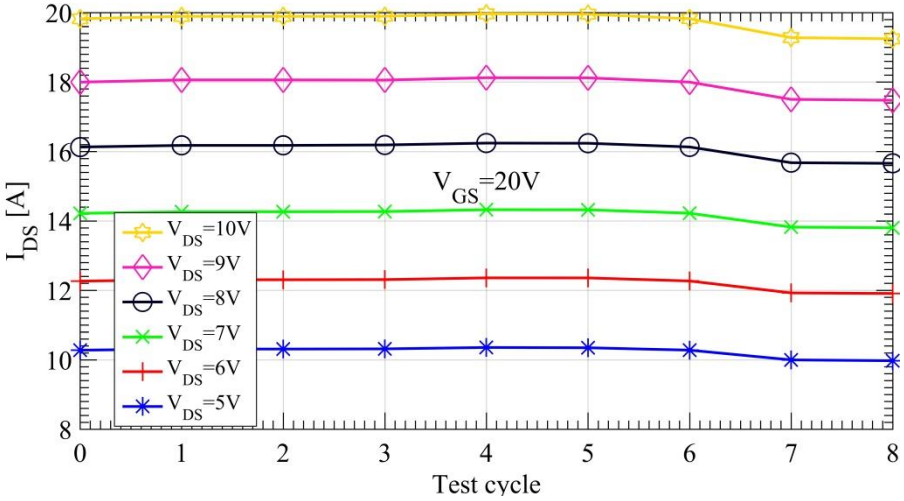

Figure 4-16 Detail of the degradation in the I-V measurements of 10 kV 10 A SiC MOSFET after short-circuit stressing for a V_{GS}=20 V observed at different drain-source voltages [89]

residual resistance, but their individual variations are not easily obtainable, as they can be hardly isolated from each other.

Figure 4-17 shows the same periodically measured I-V curves of the 10 kV 10 A 4H-SiC MOSFET but for a V_{GS}=20 V this time. At this gate voltage, the dominant component of $R_{DS,on}$ is R_S, thus any variation in the device on-state resistance will be mainly given by the residual resistance changes.

As before the variations of the current for different drain-source voltages were extracted for easier reading and are shown in Figure 4-16. The first variation in the residual resistance can be observed after the sixth test cycle, as a small decrease in current carrying capabilities at the selected drain-source voltages. The seventh test cycle characterization shows a permanent, larger decrease in current carrying capability, pointing towards a degradation in the residual resistance components, which manifests itself as an increase in R_S. The last test cycle for a V_{GS}=20 V shows no further degradation in the residual resistance.

The initial degradation seems to start in the channel regions, with a small increase in the resistance of the channel showing first after the fourth test cycle and a much larger increase in resistance after the sixth test cycle until the end of the investigation. The residual resistance only starts showing sign of degradation later in the investigation, with minor increase in resistance after the sixth tests cycle and a larger increase after the characterization at the end of the seventh test cycle. After the eighth test cycle, no degradation was observed in the residual resistance.

Figure 4-18 shows variation of $R_{DS,on}$ of the device during conduction at a current of 10 A for different drain-source voltages. During the last three test cycles

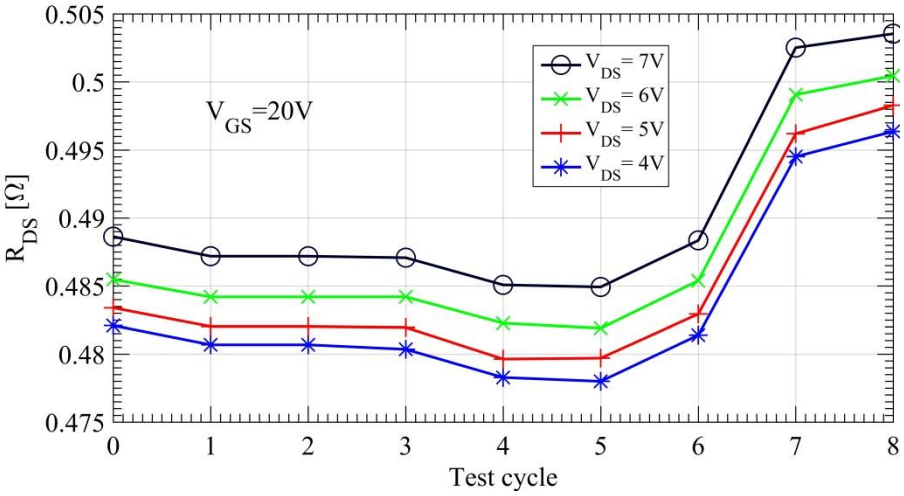

Figure 4-18 $R_{DS,on}$ degradation with stressing at different V_{DS} values for a V_{GS} [89]

the resistance of the device seems to increase by 3% or 0.15 mΩ.

In Figure 4-19 the variation of the device transfer characteristics through the entire investigation study is shown and confirms the degradation observed in the I-V measurements of the 10 kV 10 A 4H-SiC MOSFET. The characterization waveform for the seventh test cycle was not recorded due to a software error during measurement.

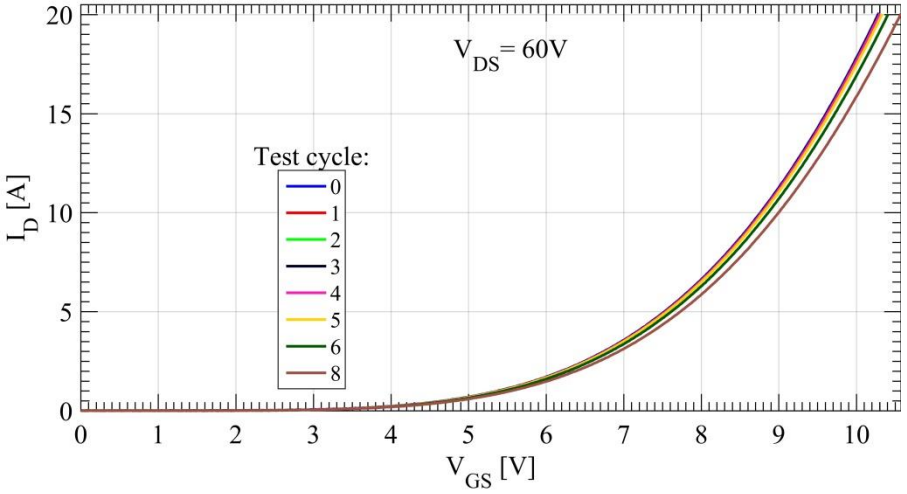

Figure 4-19 Degradation in the transfer characteristics of 10 KV 10 A SiC MOSFET after short-circuit stressing [89]

4.4.1.1.2 Gate structure degradation

The gate structure degradation can be observed in the threshold voltage and gate leakage current measurements. The measurements used to obtain the initial threshold voltage variation with temperature have not been recorded due to technical reasons. Because of this, the threshold voltage, and its variation throughout the test cycles had to be obtained from the transfer characteristics in Figure 4-19. As the measurements of the transfer characteristics are obtained with

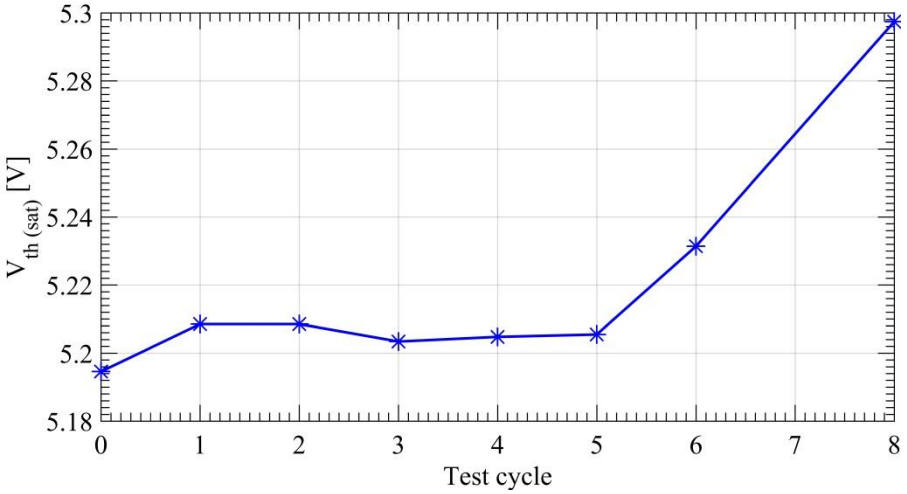

Figure 4-20 Threshold voltage variation during the short-circuit investigation for a 10 kV 10 A 4H-SiC MOSFET [89]

the device operating in the saturation region, the threshold voltage was extracted using a different method. By using the linear extrapolation method for a device operating in the saturation regime, the threshold voltage was extracted following the procedure described in [96]. The extracted threshold voltage is shown in Figure 4-20. The extraction method used is affected by residual resistance, and would contain an offset when compared to the initial measurements of the threshold voltage. Despite the offset, the variation of the threshold voltage during the investigation can be observed as a slight increase of 0.1 V in its measured value. The gate leakage currents were also measured during the investigation, and are shown Figure 4-21. The measured values were affected by the measuring error of the curve tracer as it changed scale after the fifth test cycle. The scale selection is beyond the control of the operator. None the less, the error due to the resolution of the equipment has also been included. Assuming the worst case scenario, where the leakage currents increase up to 60 nA, the values is still well under the

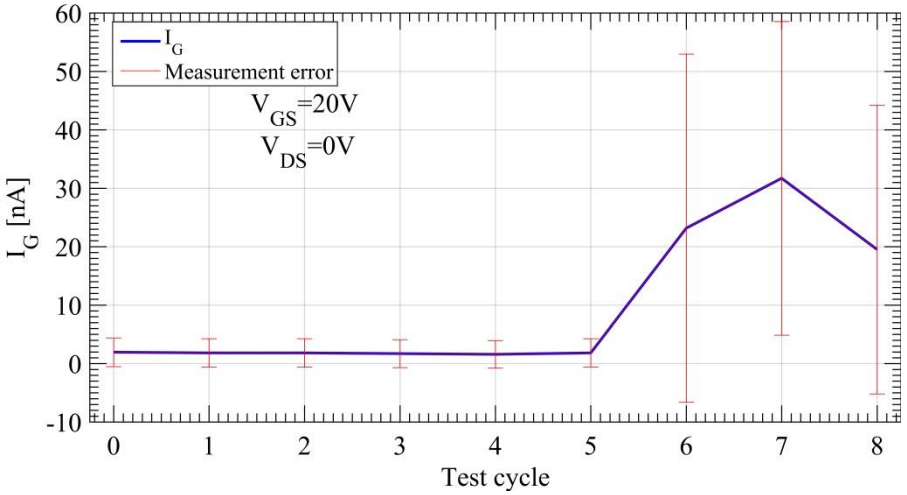

Figure 4-21 Gate leakage variation during the short-circuit investigation for a 10 kV 10 A 4H-SiC MOSFET

manufacturer acceptable gate leakage values.

4.4.2. DEVICE VISUAL DEGRADATION

As mentioned earlier, the device was visually inspected at the end of each test cycle, in order to observe variation of the surface metalization.

After the sixth test cycle, the surface metalization of the 10 kV 10 A 4H-SiC MOSFET started showing visual degradation signs. As the device investigation was not finished, a microscope picture of the chip surface was taken through the

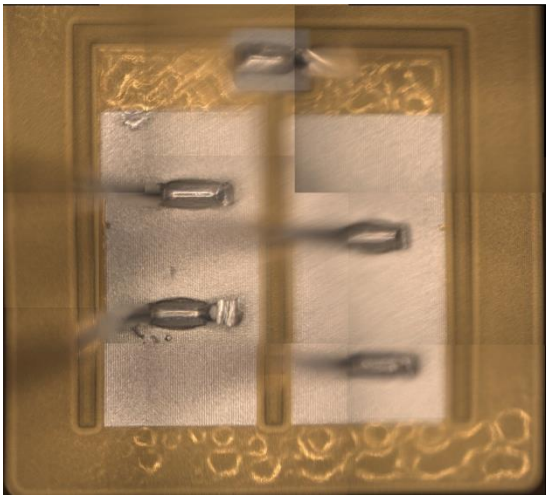

Figure 4-22 Stitched image of chip surface degradation of 10 kV 10 A 4H-SiC MOSFET after the sixth test cycle [89]

insulating silicone gel and is shown in Figure 4-22. On the top edge of the left bonding pad, a melted like region can be observed on the aluminum surface metalization, possibly due to a hot spot creation during short-circuit. The insulating polyamide used outside the bonding areas also shows bubble like degradation in different regions. The temperature reached by the aluminum metalization during the last pulse of the sixth test cycle will be simulated in order to investigate the possibility of aluminum melting.

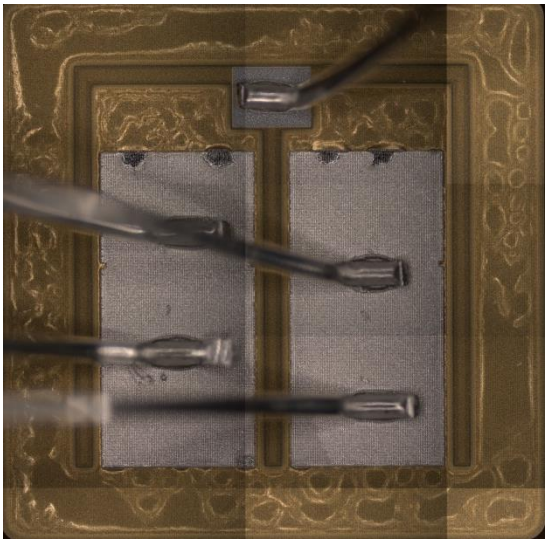

Figure 4-23 Stitched image of chip surface degradation of 10 kV 10 A 4H-SiC MOSFET at the eight test cycle, the end of the investigation [89]

At the end of the short-circuit stressing, the device was decapsulated and prepared for a scanning electron microscope inspection. The removal off the insulating silicone gel resulted in a better microscope picture, as the refraction and other artifacts caused by the gel disappeared. The degradation of the device at the end of the short-circuit stressing can be observed in Figure 4-23. Compared to the previous visual investigation, the aluminum metalization showed overall signs of reconstruction. The previously observed melted region got more accentuated and more hot spot like regions appeared around the upper edges of both bonding pads and in the bottom edge of the left bonding pad. The insulating polyamide showed even more signs of bubbling on almost the entire surface of the chip.

4.4.3. THERMAL SIMULATION OF REPRESENTATIVE PULSES

Using the same thermal model presented in chapter 4.3.1, the average temperatures in the device during pulse 60, 65 and 71, which represent each of the last pulses of the last three test cycles, have been simulated.

Figure 4-24 shows the simulated temperatures in the device for the 60th pulse of the investigation, the last one in the sixth test cycle. As before, as the model assumes all materials stay solid, and cannot account for the phase change, the aluminum temperature is not simulated above its melting point. This might be an explanation for the visual degradation of the chip surface metalization. During the pulse, based on the dissipated short-circuit energy, the peak temperature of the top

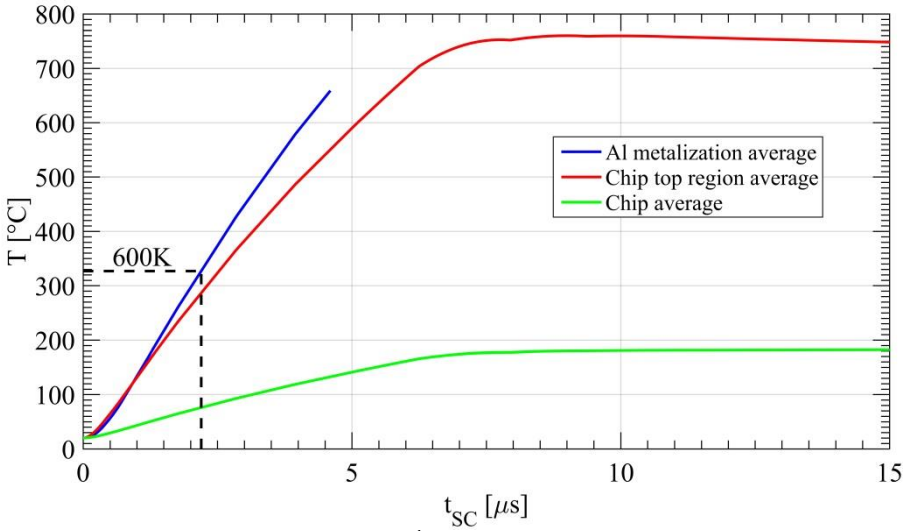

Figure 4-24 Thermal simulation for the 60th pulse, the last one in the sixth test cycle; solid blue – Average temperature for aluminum top metalization; red – chip short-circuit region; green – rest of chip [89]

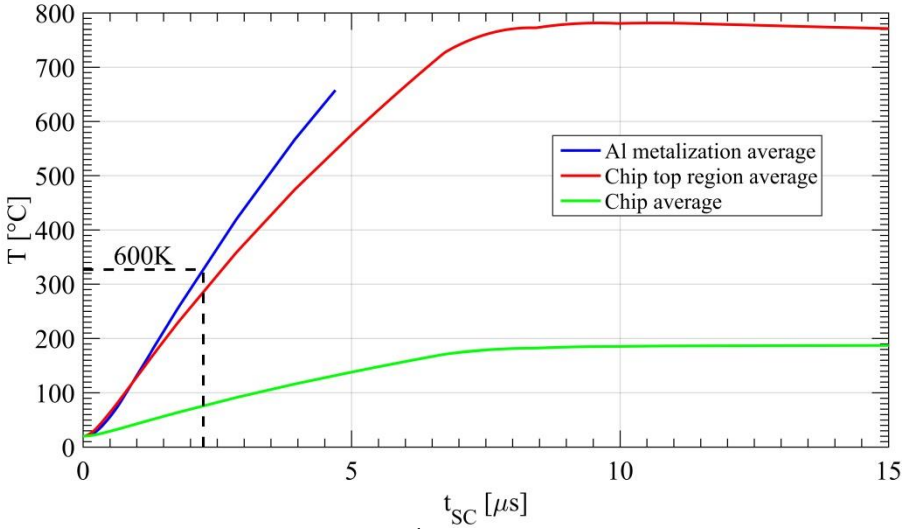

Figure 4-25 Thermal simulation for the 65th pulse, the last one in the seventh test cycle; solid blue – Average temperature for aluminum top metalization; red – chip short-circuit region; green – rest of chip [89]

region in the chip reaches 760 °C.

Figure 4-25 shows the simulated temperatures inside the chip during the 65th short-circuit pulse, the last pulse in the seventh test cycle. In this case, the chip top region average simulated temperature reached 780 °C, an increase compared to the

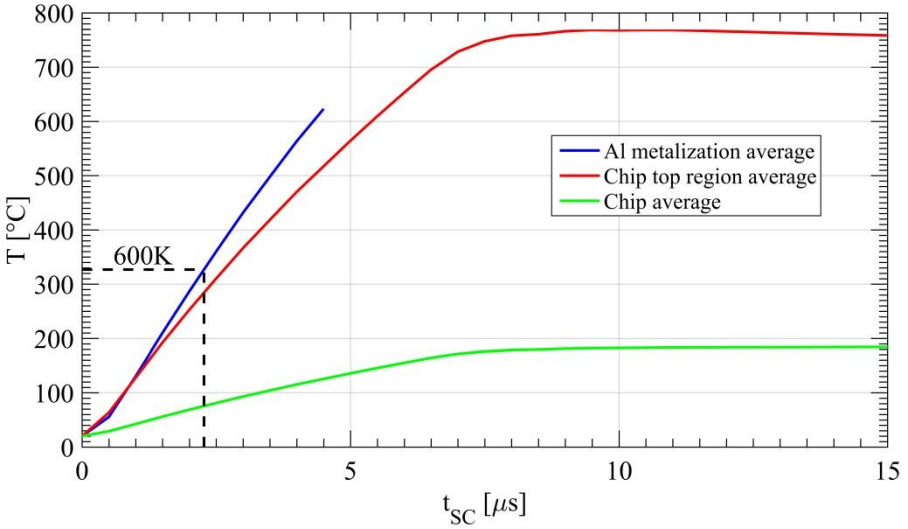

Figure 4-26 Thermal simulation for the 71st pulse, the last one in the investigation; solid blue – Average temperature for aluminum top metalization; red – chip short-circuit region; green – rest of chip [89]

previously simulated short-circuit pulse. The aluminum average temperature also reached its melting temperature.

Figure 4-26 shows the simulated temperature profiles for the 71st pulse, the last one in the investigation. As overall short-circuit current decreased in the last test cycle, the simulated peak average temperatures reached in the chip also decrease, as the longer pulse length allowed for a better diffusion of the temperature in the chip mass. Nonetheless, the melting point of the aluminum surface metalization was still reached, and the peak chip top region average temperature was 768 °C.

4.4.4. SCANNING ELECTRON MICROSCOPE INVESTIGATION

At the end of the investigation the device was decapsulated and a post degradation investigation of the device structure was performed. Initially, a slot was cut in-between two adjacent cells in the 10 kV 10 A 4H-SiC MOSFET using a focused ion beam and afterwards the structure was inspected using a scanning electron microscope. This allowed for the top surface metalization, which connect the mosfet cells to the bond wires, and the top structure of the device to be inspected for degradation.

Because this process is time consuming and costly, a single dig site was selected on the top surface metalization, shown in Figure 4-27. In order to get an estimate of the overall impact of the short-circuit on the device surface metalization, the dig site was chosen away from the melted looking regions and the bond wires, in an average looking location. The melted regions would have showed

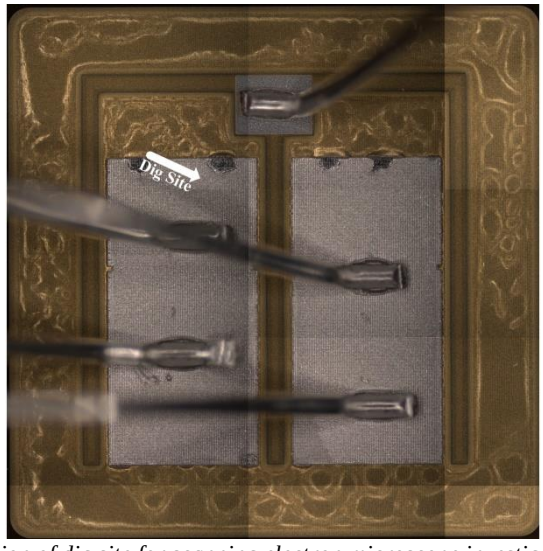

Figure 4-27 Location of dig site for scanning electron microscope investigation [89]

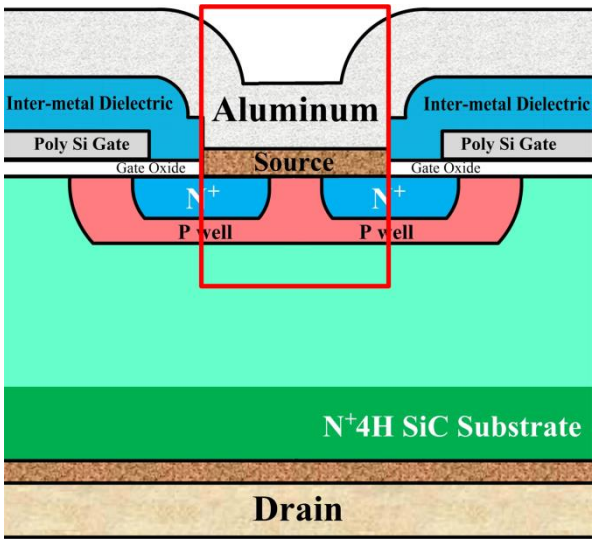

Figure 4-28 Location of scanning electron microscope image in the chip structure [89]

the worst degradation, as the degradation was already visible in the visual inspection, as shown in Figure 4-23 while the region adjacent to the bond wires might have been less degraded if the bond-wires acted like heatsink. Due to the proprietary nature of the chip structure and dimensions, the measuring scale has been removed and the image from the scanning electron microscope has been cropped. As this has made identifying the dig site and scan region difficult, Figure 4-28 was created in order to aid the reader identify the region shown in the scanning electron microscope image.

For a comparison and in order to better observe the degradation, a similar focused ion beam cut and scanning electron microscope investigation was performed on an unstressed 10 kV 10 A 4H-SiC MOSFET. Figure 4-29 shows a high magnification image of the contact region between the 4H-SiC source regions and the surface metalization. The dark region in the image is the 4H-SiC semiconductor and the middle section with the bright gray nuance, sitting on top of the SiC material is the aluminum source metalization. The bright, clear straight line represents the interface between the two materials.

Figure 4-30 shows the scanning electron microscope image of the same contact region between the 4H-SiC semiconductor source regions and the aluminum surface metalization at the dig site shown in Figure 4-27. The aluminum surface metalization shows clear signs of severe reconstruction. Large voids in the aluminum have formed at the interface region as a result of the reconstruction. As a consequence of the created cavities which diminished the contact interface between

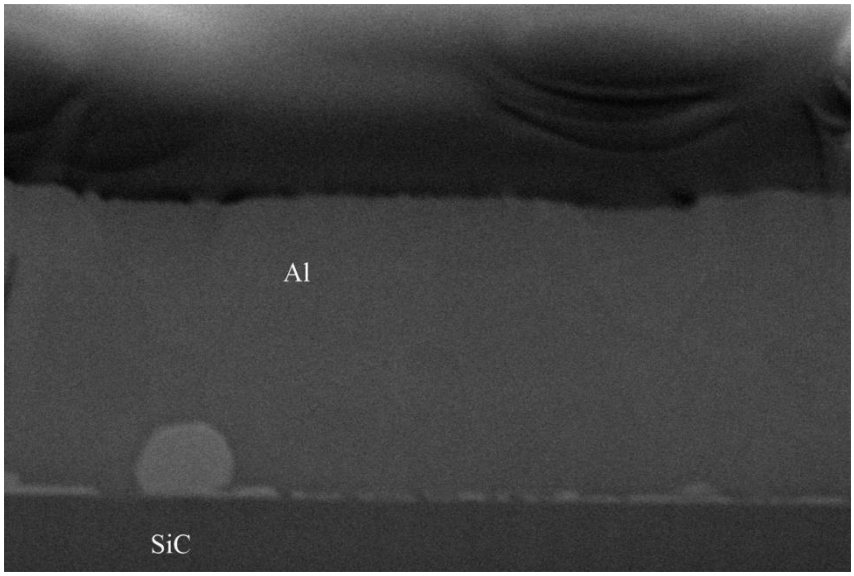

Figure 4-29 scanning electron microscope image of an unstressed 10 kV 10 A 4H-SiC MOSFET aluminum metalization at the source contact region between two MOSFET cells. Due to proprietary information the scale has been removed and the image has been cropped [89]

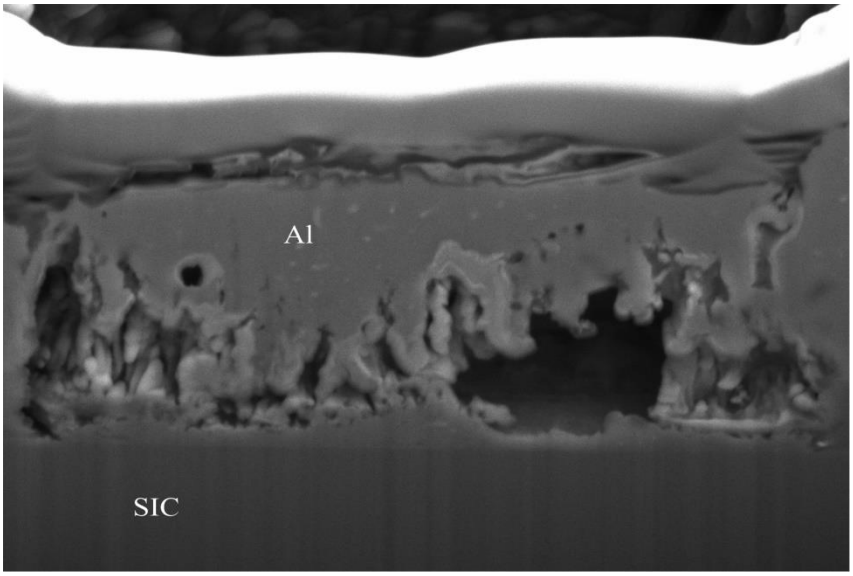

Figure 4-30 scanning electron microscope image of a stressed 10 kV 10 A 4H-SiC MOSFET aluminum metalization at the source contact region between two MOSFET cells. Due to proprietary information the scale has been removed and the image has been cropped [89]

the aluminum surface metalization and the SiC semiconductor, the on-state resistance of the 10 kV 10 A 4H-SiC MOSFET is expected to have increased.

As the dig site was chosen outside the hot-spot like region, in an average looking location, the aluminum reconstruction seems to be severe. Taking also into consideration the visually observed polyimide degradation over large areas of the chip, it can be strongly assumed that the entire chip aluminum metalization ^has undergone high thermal stresses during the investigation, supporting the thermal simulation of the short-circuit pulses. It is safe to assume that the degradation is not only limited to the hot-spot like region, and it might be homogenous across the entire chip surface.

4.4.5. DISCUSSION OF DEGRADATION

While the degradation in peak short-circuits saturation currents also observed in lower voltage 4H-SiC devices in literature [112]-[114], [120], [121], the studies were mostly focusing on degradation and subsequent failure of the gate oxide or leakage current increase. The most observed failure mechanism during short circuit for the lower voltage SiC devices has been related to gate oxide degradation, which would manifest either as increased gate leakage currents or in extreme cases even shorting of the gate and source terminals, which would prevent the device from turning on [31], [34], [112]-[121]. This type of degradation was not observable in the 10 kV 10 A 4H-SiC MOSFET during the studies. Throughout the investigation the gate-source voltage showed a consistently steady form and the measured gate leakage currents were within the manufacturer acceptable limits at the end of stressing. Another degradation sign in the 1.2 kV 4H-SiC MOSFETs was observed as a shift in the threshold voltage after stressing [113], [114]. This was not the case for the 10 kV 10 A 4H-SiC MOSFET, as the threshold voltage increase was negligible. This type of degradation and failure does not seem to be observed for the 10 kV devices.

The decrease in peak saturation currents during short circuit can be clearly observed for the 10 KV 10 A 4H-SiC MOSFET during the study only after the sixth test cycle. The characterization performed after the test cycle showed an increase in the channel resistance, emphasizing a degradation in the channel region of the device. During the same characterization, only a small variation in the device residual resistance was observed in the I-V measurements, performed at a V_{GS}=20V. At the same time the visual inspection through the insulating gel of the aluminum surface metalization showed degradation signs. Thermal simulation performed with measured data from the last pulse in the test cycle confirmed that the surface aluminum metalization reached its melting point, making aluminum reconstruction highly likely.

Continuing with the seventh test cycle, the peak short-circuit saturation currents showed a continuous decreasing trend. I-V measurements performed at the end of the test cycle highlighted a continued increase in channel resistance, pointing

to a continuous degradation of the channel region. The characterization, showed, that after this test cycle, also the residual resistance in the device increased, emphasizing a degradation in the elements associated with the residual resistance. The thermal simulation showed again high temperatures in the device top region and aluminum melting point being exceeded in the surface metalization.

The saturation current during short-circuit and its peak continued to decrease throughout the last test cycle of the investigation. The device characterization, at the end of the test cycle, showed degradation in the channel region, as an increase in channel resistance. The residual resistance also increased, but only by a small percentage, possible due to the aluminum metalization continuous degradation.

There are multiple factors which could explain the degradation in the channel resistance and, as a result, the channel resistance increase, which include, among others, a degradation in the device gate oxide, a shift in threshold voltage, trapped charges interface states or other defects which might have appeared in the SiC crystal structure due to the very high temperatures experienced by the device, especially towards the end of the investigation [134]. As a consequence of the high thermal stresses induced by the high density short-circuit energies, changes in the semiconductor material could of resulted in a degradation of the mobility in the crystal, and subsequently lead to an increase in channel resistance. The high temperatures experienced in the channel and JFET regions, and their vicinity, could have created different mechanisms which would negatively affect the mobility. The main degradation mechanism could be related to oxide charges and interface traps, which can generate high carrier scattering, negatively affecting the current flow. The scattering process can also be amplified by an increase in SiC semiconductor defects, like broken bonds, dislocations and other crystal associated defects which can be caused by high temperatures [134]. The main causes and mechanisms that led to degradation in channel mobility cannot be concluded based on this investigation, as this would require a deeper knowledge into the device structure and characteristics, such as doping levels, etc. At the same time, more specific tests and investigations are required in order to aid in isolating the impact of each mechanisms. This process, besides being time consuming, is also unfeasible, as it would require a large number of these costly devices to be degraded.

The increase in residual resistance could be expressed by a degradation in one or more of the components which define the residual resistance, and subsequently increase in their resistance. The degradation in the drift and JFET regions that would lead to an increase in their resistance can be a consequence of a decrease in their mobility, based on similar degradation mechanisms as in the case of the channel region. The SEM investigation highlighted surface aluminum metalization reconstruction and voids at the interface between the source region and the aluminum metalization which would reduce the contact area and increase the contact resistance of the interface. Similar to the observation in literature,

temperature was observed also in this case to play an important role in the overall degradation of resistance in the device.

As a side note, when comparing the 10 kV 10 A 4H-SiC MOSFET with the 1.2 kV 4H-SiC MOSFETs studied in literature, no thermally generated tail currents have been observed at turn-off after long pulses. While the aim of this study was to avoid destruction of the device, even in the case of the investigations performed in chapter 4.3, where the aim was to assess the maximum short-circuit withstand time capability, thermally generated currents, observable as tail currents during turn-off where not observed.

4.5. Summary

The 10 kV 10 A 4H-SiC first generation MOSFET short circuit capabilities and degradation where investigated. In the first part of the chapter an overview of the short-circuit in MOSFET devices was presented, together with typical waveforms generally experienced during the short-circuit events of such unipolar devices. As, up to the date of the writing, this was the first published investigation of 10 kV 10 A 4H-SiC MOSFETs during short-circuit, no prior arts was available in order to have some guidelines regarding the expected maximum short-circuit withstand time capability. An overview and review of observation regarding low voltage, 1.2 kV, 4H-SiC MOSFETs from the same manufacturer was presented and used as a guideline for possible observations, as the technology of the device under study and the literature is almost identical. Similar behavior of the short-circuit saturation current was observed in both 10 kV and 1.2 kV 4H-SiC devices, where for the initial part of the pulse the current has a positive temperature coefficient, up to the point when the temperature in the top region reaches 600 K, at which point the currents shows a negative temperature coefficient and decreases.

As no prior study regarding the short-circuit capability of 10 kV 10 A 4H-SiC MOSFETs was published, a more conservative approach was initially taken in order to observe the behavior of the device during short-circuit and the maximum short-circuit time the device could withstand for a V_{DS} = 6 kV. The device was subjected to pulses of increasing length in order to observe its limits, both in terms of energy and pulse length. The initial device short-circuit saturation current was more than 26 times higher than the nominal rated current, in contrast to the typically observed ratio, in Si devices, of 5-8 times. Degradation was observed in the initial investigation, and thermal simulation have shown that the device experienced temperatures in the junction region of 1000 °C, with the surface metalization aluminum reaching its melting temperature after the short-circuit saturation currents started showing signs of degradation. The device, despite the degradation, managed to safely turn off a pulse of 8.5 µs with a short-circuit energy of 10.65 J. The investigation ended when the device failed, after it turned off a

pulse of 8.6 µs. The device exploded moments after turn off, pointing towards an increased leakage current, possibly due to the high temperature reached in the device structure. The failure mode made it impossible for a post failure analysis to be performed. The 8.5 µs short-circuit withstand time capability is a conservative value, as the device started showing degradation much earlier and managed to turn off more than 25 extra pulses before it failed, leading to the conclusion that an unstressed device, should be capable of turning of a pulse of at least 8.5 µs if not more.

Encouraged by the findings in the first part of this chapter, a new investigation was set up in order to observe the degradation mechanism of the 10 kV 10 A 4H-SiC MOSFET during short-circuit. This investigation would be similar to the previous one, with the difference that after a significant number of short-circuit pulses of increasing length a full device electrical characterization would be performed in order to observe the regions of the device which are degrading.

During the robustness investigation, the initial degradation appeared in the channel region and as the test advanced, the residual resistance regions (drift, JFET, metalization, etc.) started to also show signs of degradation due to the short-circuit energy concentrated in the top region of the SiC chip. This was seen as an overall increase in device on-state resistance, both in the characterization measurements and during the short-circuit investigation.

The threshold voltage variation observed through the test was insignificant, and its impact on the device performance was neglectable, while the measured gate leakage current, assuming the largest measurement errors was still within manufacturer acceptable limits. Thermally generated currents and degradation in the gate structure of the 10 kV 10 A 4H-SiC MOSFET could not be observed during experiments, nor measured during the characterization as in the case of 1.2 kV 4H-SiC MOSFETs using the same technology.

The visual inspection of the aluminum surface metalization showed signs of reconstruction and degradation. This was confirmed by the thermal simulation of the short-circuit pulses, in which the aluminum melting temperature was reached and surpassed, making the reconstruction of the surface metalization possible. The SEM investigation also confirmed that the aluminum reconstruction took place, and at the same time cavities have formed at the interface between the SiC MOSFET cells source region and the surface metalization. This would result in an increase residual resistance and possibly a higher temperature do to the reduction in area of contact and subsequent increase in contact resistance.

While it was clear that the temperature experienced by the device during short-circuit is initiating the degradation observed in the device, it is not possible from the conducted measurements to clearly identify the main degradation

mechanism of the device without deeper knowledge of the device characteristics. Degradation of the SiC crystal structure, charges implanted in the oxide during the short-circuit, interface state charges or other similar material defects associated with the high temperature stressing and high electric field experienced during short-circuit are the most plausible explanation for the degradation in device mobility.

Chapter 5.
Conclusion and future work

The main conclusions of the PhD thesis are summarized in this chapter alongside recommendations for future work, which might give a better insight into the usefulness and applications of the devices studied.

5.1. Summary of conclusions

In order to overcome the challenges mentioned in Chapter 1 and to accelerate the adaptation of 10 kV 4H-SiC devices into the high voltage, high power market the Ph.D. study has focused on two main topics, required for the understanding and implementation of such devices in power electronics converter: characteristics of 10 kV 10 A 4H-SiC MOSFETs and short-circuit capability and degradation.

Chapter 2 provided an introduction into the still novel SiC unipolar power devices, and compared from a theoretical point of view the preferred power semiconductor for unipolar devices, Si, with its most promising successor in the high voltage range, 4H-SiC. Advancement during the past few decades on Si semiconductor materials have been pushing the material very close to its theoretical edge, while, sometimes, even surpassing them with unique structures, such as super junction MOSFETs. Compared to Si, SiC has been the focus of research only recently, and has already shown outstanding performance, and better material characteristics. Continuous improvements on the power semiconductor devices structure, similar to those in Si, could achieve even higher performances. Because of this uneven focus on the devices structure which would better suite each semiconductor material, a theoretical material comparison promised to highlight only the material advantages, and not the advantages gained from the research on the materials. During the comparison, SiC has showed significantly better performance in terms of both switching and conduction losses, thinner chip sizes and better thermal management. In all, SiC managed to surpass Si as a semiconductors and its promising to be the material of choice for the next generation high voltage power semiconductor.

Chapter 3 investigates the history and improvements of SiC unipolar power devices from the first report of such a device up to current days. As the 10 kV 10 A is a relatively new device, which has been available only recently as an engineering sample, the study of the device characteristics required new a new test setup to be designed in order to study the characteristics of the device at the expected nominal operating values. The test setup was custom designed around the packaged 10 kV 10 A 4H-SiC MOSFET with the aim of reducing as much as possible the parasitic

inductance in the switching loop, in order to limit the impact of the circuit on the device behavior and evaluate only the device under test.

Static and dynamic characteristics of the device are of high interest and required in order to efficiently design a converter, which employs such devices, and operate it correctly and safely. The 10 kV 10 A 4H-SiC MOSFET has been extensively characterized at temperatures varying from room temperature up to 150 °C in order to observe its expected behavior during operation. The dynamic behavior of the device during switching has been studied for different gate voltages, drain-source voltages, temperatures and drain currents in order to assess the devices in as many as possible situations, as to get a better understanding of the device behavior during switching.

The second part, discussed in Chapter 4 has evaluated the short-circuit behavior of the first generation 10 kV 4H-SiC MOSFET. The short-circuit behavior and capability is very important in order to evaluate the robustness of power devices, and gives an insight for the converter designer of the minimum required protection times before employing such a device in an application which requires high availability.

By modifying the setup used for the dynamic characterization, the short-circuit withstand time of the 10 kV 10 A 4H-SiC MOSFET can be investigated. As this was the first short-circuit study done on such a device and due to the limited availability of such packaged devices, a more conservative approach was taken into the investigation. The short-circuit capability was investigated by constantly and systematically increasing the pulse length until the device failed. As the device started showing degradation signs and increased resistance, half way in the short-circuit investigation, it was clear that an unstressed device, should be capable of supporting a short-circuit for at least as long as the device tested. Considering the short-circuit voltage and currents the device experienced, its capabilities seemed quite remarkable, considering it was never designed for such operation, being just a first iteration research sample. The failure of the device was destructive, after turn-off and was most probably due to an increased leakage current in the device. Thermal simulation of the short-circuit revealed high temperatures throughout the top surface of the chip, with the aluminum surface metalization surpassing its melting point.

Motivated by the degradation observed during the search for a short-circuit withstand capability, a new study was performed in order to investigate the variation in the electrical parameters during the short-circuit degradation, in an attempt to better understand the device behavior during short-circuit.

The testing procedure for the new investigation was selected to be as similar as possible to the previous investigation. This allowed for the device to be stressed

up to the limits observed earlier and at the same time avoid a destructive failure. By avoiding the device catastrophic failure, the chip could be decapsulated and then studied in a SEM in order to observe any irregularities in the structure of the MOSFET. In addition, the device was periodically electrically characterized and visually inspected in order to observe any variation in the electrical parameters which might provide an insight into the degradation mechanism during short-circuit. The observed degradation was observed in regions corresponding to both channel resistance and residual resistance, with first signs of degradation commencing in the channel region and then propagating to the residual resistance throughout the investigation. While in similarly designed devices with lower voltage ratings the degradation was mostly attributed to gate oxide degradation in the case of the 10 kV 10 A 4H-SiC no such degradation was observed.

Non the less the degradation was generated by the high temperatures experienced by the device during short-circuit at drain-source biases of 6 kV and currents more than twenty-five times larger than the nominal rated current which would concentrate a large energy in the top portion of the 4H-SiC chip.

After degradation the device aluminum surface metalization was visually inspected and showed signs of degradation, which was confirmed by the SEM images showing cavities that formed at the interface between the source region of the semiconductor material and the aluminum. This also was in accordance with the temperatures observed during the thermal simulation where the aluminum melting point was reached.

While the study could not conclude the exact physical mechanism of the failure during short-circuit, it was able to highlight the process of the degradation and affected regions providing a new insight into the operation of the 10 kV 10 A 4H-SiC MOSFETs. Possible degradation mechanism have been proposed, but further investigation into the physical degradation of the device are required in order to narrow down the possible degradation mechanisms during short-circuit. This can be used by the manufacturer in order to improve the structure and design of the device and at the same time by converter designer in order to proper design their short-circuit protection circuits and at the same time identify devices which have been degraded during operation, allowing them to better estimate device lifetime or imminent failure.

5.2. Main contributions from author’s point of view

The main contributions of this Ph.D. work from point of view of the author are summed up as follows:

Design of a custom, low inductance, unified test circuit for 10 kV 10 A 4H-SiC MOSFETs:

- Development of custom DC-link suitable for 10 kV 10 A 4H-SiC MOSFETs with off-the-shelf parts;
- Development of low inductance test setup suitable of characterizing 10 kV 10 A 4H-SiC MOSFETs during switching, short-circuit and unclamped inductive switching for a wide range of temperatures with voltages up to 15 kV and currents in excess of 250 A;

Analysis of the dynamic and static characteristics of 10 kV 10 A 4H-SiC MOSFETs:

- Investigation of static characteristics of 10 kV 10 A 4H-SiC MOSFETs;
- Investigation of the switching characteristics of 10 kV 10 A 4H-SiC MOSFET over a wide range of drain-source voltages, drain currents, junction temperatures and gate-source voltages;
- Analyzing the switching losses variations and characteristics of 10 kV 10 A 4H-SiC MOSFET over a wide range of parameters;

Analysis of the short-circuit capability of 10 kV 10 A 4H-SiC MOSFETs:

- Identifying the maximum short-circuit time capability of the device with a conservative approach;
- Identifying the short-circuit saturation current of the 10 kV 10 A 4H-SiC MOSFET and variation with pulse length;
- Simulation of device average temperatures during short-circuit operation and correlation between temperature and mobility in the investigated device;

Analysis of the short-circuit degradation in 10 kV 10 A 4H-SiC MOSFETs:

- Observation of degradation in 10 kV 10 A 4H-SiC MOSFETs during short-circuit stressing;
- Correlation between short-circuit degradation observations and variations of the electrical parameters of the 10 kV 10 A 4H-SiC MOSFETs;

- Visual and FEM imaging degradation observations in 10 kV 10 A 4H-SiC MOSFETs in order to highlight the degradation impact on the device surface metalization;

- Thermal simulation of the average temperatures in the device during short-circuit operation, and variation with time to confirm the current and mobility variation in relationship with short-circuit pulse variation.

5.3. Future Work

As the 10 kV 10 A 4H-SiC MOSFET is a very novel device which has yet to be fully studied, especially from the reliability point of view, there are different subjects which can be investigated to further improve the work. The main research topics for further investigation could include:

- Further investigations into the physical structure of the device after degradation in order to observe physical changes in the device. This way a defect density increase could be observed and at the same time, each region of the device could be studied for alterations or crystal defects increase which could give a better insight into the cause of the degradation.

- Investigation of the avalanche capability of the 10 kV 10 A 4H-SiC MOSFET. Considering a test setup capable of testing the avalanche capability of such a device is already available, such a study could be easily performed and would give a better insight into the reliability and suitability of such a device to be deployed in grid connected power converters.

- Comparison between the third generation 10 kV and 15 kV 4H-SiC MOSFETs and the first generation device. Considering the advancements in manufacturing which were observed between the first and third generation in the 1.2 kV devices, the latest generation high voltage SiC MOSFETs should outperform the device in this study, not only during dynamic events, but also from the reliability point of view.

- Development of a better thermal model for the device. A 3D model of the device which would also consider the phase change in the aluminum surface metalization could better identify the temperatures inside the device during short-circuit. .

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