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A Fixed-Frequency Bidirectional Resonant DC-DC Converter Suitable for Wide Voltage Gain Range

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***Abstract*—This paper proposes a new bidirectional resonant dc-dc converter suitable for wide voltage gain range applications (e.g., energy storage systems). The proposed converter overcomes the narrow voltage gain range of conventional resonant DC-DC converters, and meanwhile achieves high efficiency throughout the wide range of operation voltage. It is achieved by configuring a full-bridge mode and a half-bridge mode operation during each switching cycle. A fixed-frequency phase-shift control scheme is proposed and the normalized voltage gain can be always from 0.5 to 1, regardless of the load. The transformer root-mean-square (RMS) currents in both the forward and reverse power flow directions have a small variation with respect to the voltage gain, which is beneficial to the conduction losses reduction throughout a wide voltage range. Moreover, the power devices are soft-switched for minimum switching losses. The operation principles and characteristics of the proposed converter are firstly analyzed in this paper. Then the analytical solutions for the voltage gain, soft-switching and RMS currents are derived, which facilitates the parameters design and optimization. Finally, the proposed topology and analysis are verified with experimental results obtained from a 1-kW converter prototype.**

***Index Terms*—Bidirectional dc-dc converter, resonant converter, wide voltage gain.**

I. Introduction

Recently, bidirectional dc-dc converters (BDCs) have gained much popularity because of their applications in energy storage systems [1]-[2], electric vehicles (EVs) [3]-[5], vehicle-to-grid (V2G) [6]-[7], and microgrids [9]-[10]. Normally, BDCs are connected with energy storage devices, e.g., the battery and supercapcitor, whose voltage usually varies over a wide range during operation [11]. Therefore, how to keep high efficiency over a wide voltage range becomes a challenge to BDCs.

Bidirectional dc-dc converters can be divided into non-isolated [2], [7]-[9] and isolated [1], [3]-[7], [10]-[39] topologies. Compared to non-isolated circuits, isolated bidirectional dc-dc converters (IBDCs) are more advantageous in terms of safety, soft-switching and step-up/-down ratio [13]. For the IBDC topologies, two basic categories, i.e., the current-fed [14]-[20] and voltage-fed [21]-[39] IBDCs, can be found in literature. Current-fed IBDCs feature a smaller input/output current ripple, smaller input/output capacitor size and a wider voltage gain range [15], but the voltage stress of switches is high, a large dc inductor is usually required, and in general, the reported experimental efficiency is inferior to voltage-fed IBDCs. For example, the peak efficiencies of 92.2% at 1.6 kW [14], 96.4% at 2.35 kW [15], 95.2% at 200 W [16], 93%-95% at 200W [17], 96% at 200 W [18], 95.4% at 3.2 kW [19] and 92 % at 600 W [20] can be found in the literature of current-fed IBDCs. However, higher peak efficiencies, e.g., 98% at 2.5 kW in [7], 97.7% at 4 kW in [21], 97.2% at 600 W in [22], 96.7 % at 700 W in [23] and 98% at 5 kW in [24], have been achieved for voltage-fed IBDCs. Therefore, the voltage-fed IBDCs seem more promising in terms of achieving high efficiency.

Among various voltage-fed IBDC topologies, the dual active bridge (DAB) converter [25] has been attracting many research interests for its excellent performance in efficiency, power density, buck/boost operation, reliability and modularity [26]-[30]. However, when the normalized voltage conversion ratio deviates from unity, the soft-switching range becomes narrow and the circulating current inside the DAB converter increases remarkably [27]-[28]. Thus, it is challenging for the DAB converter to maintain high efficiency over a wide gain range. Although many improved modulation strategies, e.g., the extended phase-shift [29], dual phase-shift [27], triple phase-shift (TPS) [31], have been proposed, the reported efficiency performance of DAB converter is still inferior to resonant-type IBDCs [21]-[24], [32]-[39] where the direct power transfer from the source to the load is possible, switches are soft-switched and the circulating current is relatively smaller [40].

The series resonant DAB (SR-DAB) [32]-[35] can operate with a variable-frequency control or with a fixed-frequency control. In [32], a fixed-frequency phase-shift controlled 1-MW SR-DAB is designed and evaluated, resulting in a theoretical peak efficiency of 98.6%. In addition to the single-angle phase-shift control in [32]-[34], more degrees of freedom can be achieved by applying the triple-phase-shift modulation to the SR-DAB [35], resulting in a marked efficiency improvement due to the root-mean-square (RMS) current minimization; but the soft-switching may not be realized when the voltage gain or the load changes.

By changing the structure of the resonant network, several resonant-type IBDCs are proposed in [21]-[22], [36]-[39] for performance improvement. Particularly, the CLLC- and CLLLC-type resonant IBDCs gain much attention due to their symmetrical characteristics in both the forward and reverse power flow directions [7], [21], [37]-[39]. In [21] and [39], the variable-frequency controlled bidirectional CLLLC resonant

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dc-dc converter is studied, but the normalized voltage gain is fixed at unity. In order to maintain high efficiency over a wide gain range, a design method for the bidirectional CLLC and CLLLC resonant converters is proposed in [7]. Nevertheless, the charging efficiency degrades dramatically when the battery voltage changes and the frequency varies over a wide range in the discharging operation.

LLC resonant converters feature high efficiency, high power density and low cost, and therefore have been widely applied in industry [11]. However, when used for the reverse power transfer, the LLC resonant converter operates as a conventional series resonant converter whose gain range is very narrow [7]. In [22], an extra inductor is added to the LLC resonant converter such that the circuit becomes symmetric for both the forward and reverse operation. A fixed-frequency modulated bidirectional three-level LLC resonant converter is proposed in [23], and a wide gain range can be achieved; however, the accurate analytical gain model is not derived, and also twelve switches are used.

This paper proposes a new bidirectional resonant dc-dc converter which can achieve high efficiency over a wide voltage gain range. Instead of the conventional variable-frequency modulation, a fixed-frequency phase-shift modulation is proposed, and thus both the half-bridge mode and the full-bridge mode occur on the secondary side over each switching cycle. By adjusting the duration of half-bridge mode, a wide normalized gain range from 0.5 to 1 can be achieved in both power transfer directions regardless of the load. Instead of the widely used first harmonic approximation (FHA) method, the time-domain analysis is conducted in this research; as results, the analytical models for the voltage gain, power transfer, soft-switching, and RMS currents are derived and verified with simulations and experimental results. It is found that the inductors ratio has no impact on the voltage gain range; thus, on the premise of achieving ZVS, the magnetizing inductance can be designed possibly large to reduce conduction losses. Furthermore, the variation of conduction losses with respect to the voltage gain is small. As a result, high efficiency can be achieved over a wide gain range. The paper is organized with Section II presenting the operating principles in both the forward and reverse power flow directions. The key operating characteristics including the voltage gain, power transfer, soft-switching, RMS currents, and performance comparison are studied in Section III, before experimental results are presented in Section IV. Finally, conclusions are drawn in Section V.

II. Operating Principles

A. Topology Description

The proposed bidirectional resonant dc-dc converter is shown in Fig. 1(a). There are two switching modes for the secondary circuit, i.e., the full-bridge (FB) mode and the half-bridge (HB) mode, as shown in Fig. 1(b) and (c), respectively. When operated in the FB mode, the voltage across the secondary transformer winding, u_{cd}, is equal to $\pm V_s$; whereas in the HB mode $u_{cd} = \pm V_s/2$, as illustrated in Fig. 2 It should be noted that both the FB and HB modes can exist during each switching cycle, but the time interval ratio of the two operation modes can be controlled to regulate the power transfer between the primary and secondary sides. The major benefit of the dual-bridge configuration is that it can adapt to a wide voltage variation on the secondary source V_s, i.e., the conduction losses can be kept low and the soft-switching can be realized over a wide gain range, which will be detailed in Section III.

The bidirectional power transfer capability is enabled for the proposed converter. In the reverse power flow direction, the magnetizing inductor L_m is always clamped by the secondary ac voltage u_{cd}, and the proposed circuit is an LC series resonant converter. However, in the forward power transfer mode, the magnetizing inductor L_m takes part in the resonance, and the proposed circuit is actually an LLC resonant converter. The LC series resonant frequency f_r is determined by the resonant inductor L_r and resonant capacitors C_{r1} and C_{r2}, i.e.,

$$f_r = \frac{1}{2\pi\sqrt{L_r(C_{r1} + C_{r2})}} \tag{1}$$

B. Operation Principle

In this research, the switching frequency is fixed at the LC resonant frequency, i.e., $f_s = f_r$. Fig. 2(a) and (b) depicts the fixed-frequency phase-shift modulation schemes for the forward and reverser power flow directions, respectively. In the forward operation, the gate signals of S_3-S_6 are blocked; neglecting the deadtime, the primary switches S_1 and S_2 are operated complementarily with a constant duty cycle of 0.5, whereas S_7 and S_8 have a variable duty cycle but they are phase shifted with a constant π. At the turn-on moment, S_1 and S_2 are synchronized with S_8 and S_7, respectively; but for the turn-off, S_1 and S_2 are leading S_8 and S_7, respectively, by a phase angle ϕ which is also the time duration of the HB mode (cf. Fig.2). The switching pattern in the reverser operation, however, is different from that in the forward operation. Specifically, the primary switches S_1 and S_2 are blocked; S_3 and S_4 are operated complementarily with a constant duty cycle of 0.5, whereas S_7 and S_8 have a variable duty cycle but they are phase shifted with a constant π. In the reverse operation, S_8 and S_7 are synchronized with S_3 and S_4, respectively, at turn-off; but S_8 and S_7 are leading S_3 and S_4, respectively, by a phase angle ϕ at turn-on; For the gate signals of S_5 and S_6, when neglecting the deadtime, they are complementary with those of S_8 and S_7, respectively. In both power flow directions, the duty cycle of S_8 and S_7, D_{S78}, can be always expressed by $D_{S78} = 0.5 + \phi/(2\pi)$.

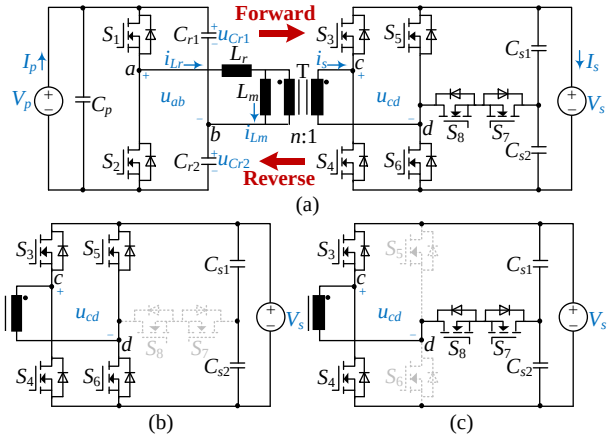


Fig. 1. (a) Schematic of the proposed bidirectional resonant dc-dc converter; (b) full-bridge mode and (c) half-bridge mode on the secondary side.

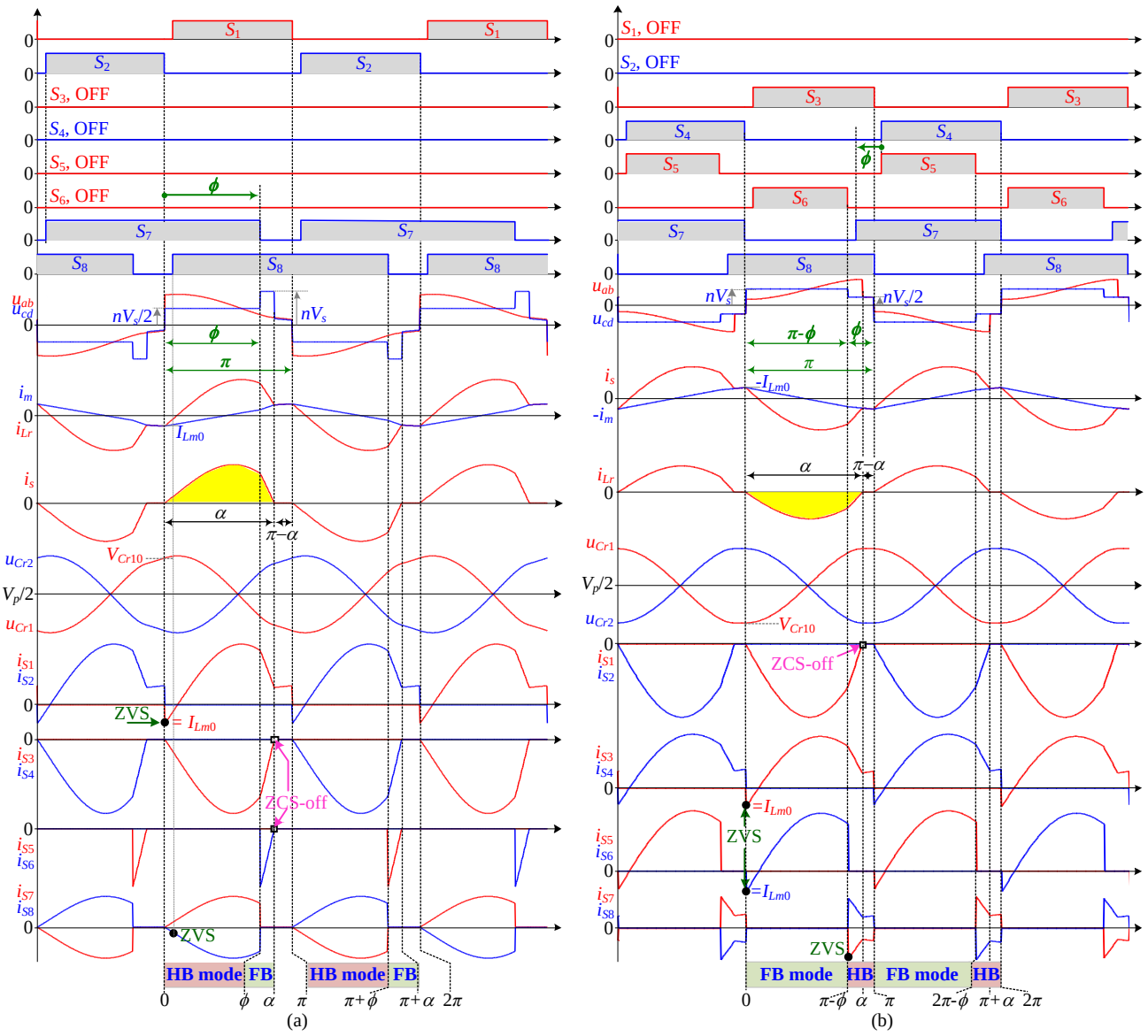


Fig. 2. Modulation scheme and steady-state operating waveforms of the proposed converter in (a) forward and (b) reverse power flow directions.

The phase shift angle ϕ is used to regulate the power transfer for both power flow directions. The key operating waveforms are shown in Fig. 2 as well. The yellow areas of i_s in the forward operation and of i_{Lr} in the reverse operation are the current directly transferred to the secondary and primary sources, respectively. The duration of the two areas is defined as phase angle α. In addition, it can be seen that in the forward operation, the driven switches S_1–S_2 and S_7–S_8 achieve ZVS-on, and the anti-parallel diodes of switches S_3–S_6 turn off with ZCS; in the reverse operation, all secondary-side switches S_3–S_8 can achieve ZVS-on, and the anti-parallel diodes of S_1–S_2 operate under ZCS.

In order to simplify the analysis on the converter, assumptions and definitions are made in the following:

1) C_{r1} and C_{r2} are assumed to be equivalent in capacitance, and this value is represented as C_r;
2) the inductors ratio of L_m to L_r is denoted as m, i.e., $m = L_m / L_r$;
3) all voltages and currents are referred to the primary side and are normalized based on $V_{base} = V_p$ and $I_{base} = V_p / Z_r$ where the characteristic impedance $Z_r = \sqrt{L_r / (2C_r)}$;
4) the voltage gain is defined as $G = nV_s / V_p$, where n denotes the transformer turns ratio;
5) the quality factor Q is defined as $Q = 4Z_r / R_p = 4Z_r |P| / V_p^2$, where P is the transferred power. For the forward and reverse power flow directions, the polarity of P is positive and negative, respectively.

The normalized initial voltage across the resonant capacitor C_{r1}, i.e., V_{Cr10} (cf. Fig. 2), can be obtained as

$$V_{Cr10} = 1 / 2 + d\pi Q / 4 \tag{2}$$

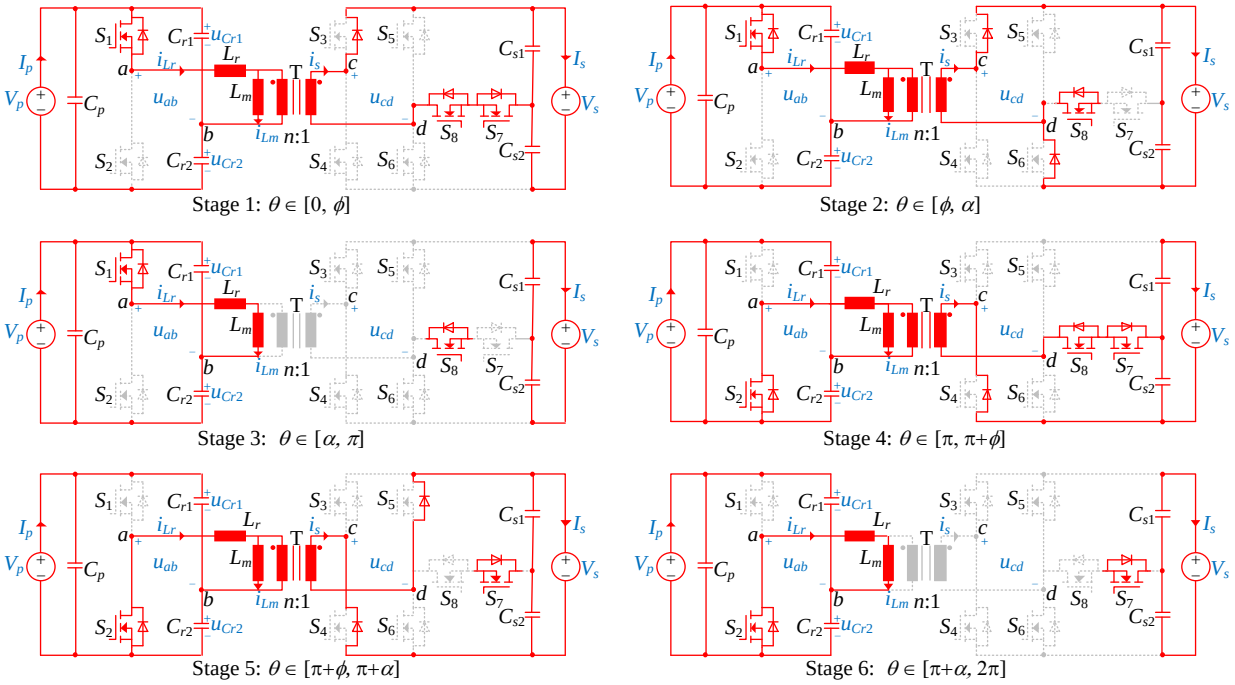


Fig. 3. Operation stages of the proposed converter in the forward power flow direction.

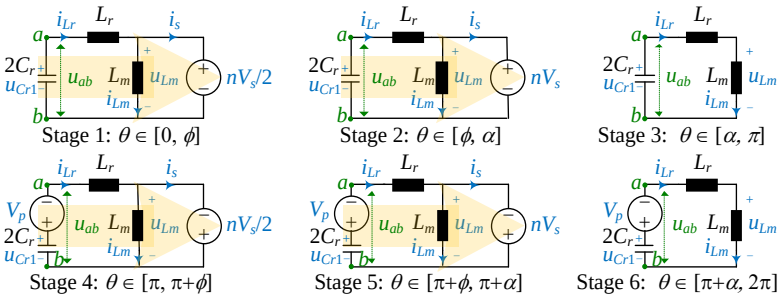


Fig. 4. Equivalent circuits of the proposed converter in the forward power transfer mode.

where d is the sign function of the power flow direction, i.e., d = 1 for the forward operation, and d = -1 for the reverse operation.

During all stages, the secondary current i_s can be always obtain by $i_s = i_{Lr} - i_{Lm}$.

1) Forward Operation

Neglecting the deadtime, six stages can be identified over one switching cycle. Due to the symmetry of operation, only stages 1-3 over the first half switching cycle [0, π] are described in this paper.

Stage 1 ($\theta \in [0, \phi]$, see Fig. 2(a), Fig. 3 and Fig. 4): Before the time instant 0, S_2 and S_7 are conducting. At θ= 0, S_2 is turned off, the negative magnetizing current I_{Lm0} begins to charge/discharge the output parasitic capacitors C_{oss1}-C_{oss2}, such that S_1 can achieve ZVS-on. During this stage, L_r and the parallel combination of C_{r1} and C_{r2} resonate, and the magnetizing inductor L_m is clamped to half of the output voltage because S_7 is triggered on. Thus, the magnetizing current i_{Lm} increases linearly. This stage corresponds to the half-bridge operation. For the secondary current i_s, it rises from 0 and begins to discharge the output capacitance of S_8, i.e., C_{oss8}. When C_{oss8} is fully discharged, the antiparallel diode of S_8 conducts. Thus, ZVS-on of S_8 can be achieved subsequently by applying a drive signal. The equivalent circuit at this stage is shown in Fig. 4. Since S_1 is conducting, C_{r2} in series with the primary source V_p is connected in parallel with the resonant capacitor C_{r1}. The equivalent resonant capacitance is $2C_r$, and the resonant tank voltage u_{ab} equals to the resonant capacitor voltage u_{Cr1}. Thus the normalized equations for the resonant tank can be expressed as

$$\begin{cases} i_{Lr}(\theta) = \lambda_1 \sin\theta + I_{Lm0}\cos\theta \\ u_{Cr1}(\theta) = \lambda_1 \cos\theta - I_{Lm0}\sin\theta + G/2 \\ i_{Lm}(\theta) = G\theta/(2m) + I_{Lm0} \end{cases} \tag{3}$$

where $\lambda_1 = V_{Cr10} - G/2$.

Stage 2 ($\theta \in [\phi, \alpha]$, see Fig. 2(a), Fig. 3 and Fig. 4): At θ = ϕ, S_7 is turned off, and secondary current is diverted from S_7-S_8 to the antiparallel diode of S_6. Thus, the secondary ac voltage u_{cd} is equal to the secondary output voltage nV_s which causes the magnetizing current to linearly increase with a sharper slope. In this stage, the converter operates in the full-bridge mode. The capacitor voltage u_{Cr1} at this stage is lower than nV_s, and therefore i_{Lr} decreases. The equivalent circuit can be found in Fig. 4, and the normalized equations are expressed as

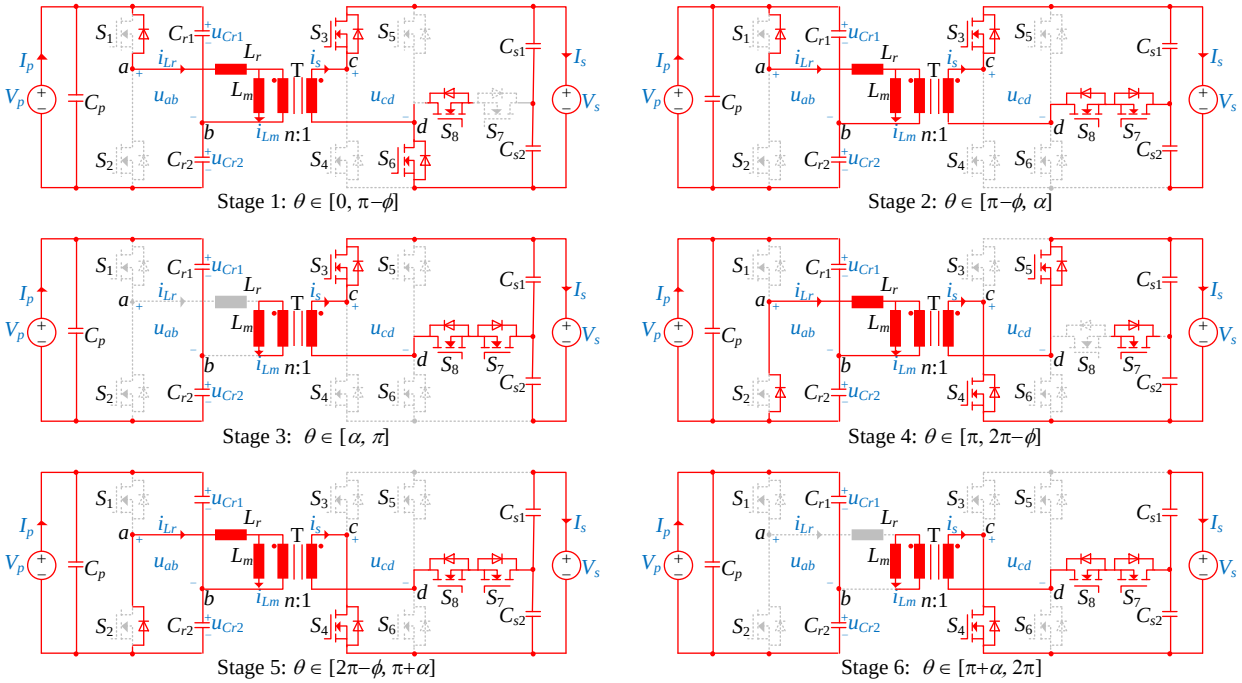


Fig. 5. Operation stages of the proposed converter in the reverse power flow direction.

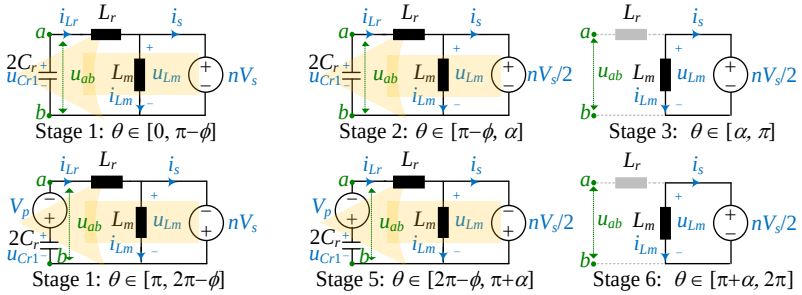


Fig. 6. Equivalent circuits of the proposed converter in the reverse power transfer mode.

$$\begin{cases} i_{Lr}(\theta) = \lambda_2 \sin(\theta-\phi) + i_{Lr}(\phi)\cos(\theta-\phi) \\ u_{Cr1}(\theta) = \lambda_2 \cos(\theta-\phi) - i_{Lr}(\phi)\sin(\theta-\phi) + G \\ i_{Lm}(\theta) = G(\theta-\phi)\,/\,m + i_{Lm}(\phi) \end{cases} \tag{4}$$

where $\lambda_2 = u_{Cr1}(\phi) - G$.

Stage 3 ($\theta \in [\alpha, \pi]$, see Fig. 2(a), Fig. 3 and Fig. 4): When the resonant current i_{Lr} decreases to be equal to the magnetizing current i_{Lm}, the secondary ac current i_s falls to 0. Thus, the antiparallel diodes of S_5 and S_6 turn off with ZCS. At this stage, the magnetizing inductor L_m takes part in the resonance, and the equivalent circuit is shown in Fig. 4. The mathematic expressions of the resonant tank can be derived as

$$\begin{cases} i_{Lr}(\theta) = i_{Lm}(\theta) = k u_{Cr1}(\alpha)\sin[k(\theta-\alpha)] \\ \qquad\qquad + i_{Lr}(\alpha)\cos[k(\theta-\alpha)] \\ u_{Cr1}(\theta) = u_{Cr1}(\alpha)\cos[k(\theta-\alpha)] \\ \qquad\qquad - k^{-1} i_{Lr}(\alpha)\sin[k(\theta-\alpha)] \end{cases} \tag{5}$$

where $k = (1+m)^{-1/2}$.

At $\theta = \pi$, S_2 starts to conduct; thus C_{r1} in series with the primary source V_p is connected in parallel with the resonant capacitor C_{r2}. The equivalent resonant capacitance is still $2C_r$, but the resonant tank voltage u_{ab} is equal to $u_{Cr1} - V_p$, as shown in Figs. 3 and 4.

2) Reverse Operation

Similarly to the forward operation, six stages can also be identified over one switching cycle if the deadtime is neglected. Due to the symmetry of operation, only the first three stages are detailed. Different from the forward operation, the magnetizing inductor in the reverse operation is always clamped by the secondary voltage u_{cd}.

Stage 1 ($\theta \in [0, \pi-\phi]$, see Fig. 2(b), Fig. 5 and Fig. 6): Before time instant 0, S_8 has been turned on. At $\theta = 0$, S_4 and S_7 are turned off, the negative magnetizing current begins to charge/discharge the output parasitic capacitors C_{oss3}-C_{oss7}, such that S_3 and S_6 can achieve ZVS-on subsequently. During this stage, the secondary resonant tank voltage u_{cd} equals to the secondary voltage nV_s; the converter operates in the full-bridge mode. Inductor L_r resonates with the parallel combination of C_{r1} and C_{r2}, which causes the antiparallel diode of S_1 to conduct. As a result, C_{r2} in series with the primary source V_p is connected in parallel with the resonant capacitor C_{r1}. The equivalent resonant capacitance is $2C_r$, and the resonant tank voltage u_{ab} equals to the resonant capacitor voltage u_{Cr1}. The normalized mathematic equations for the resonant tank can be expressed as

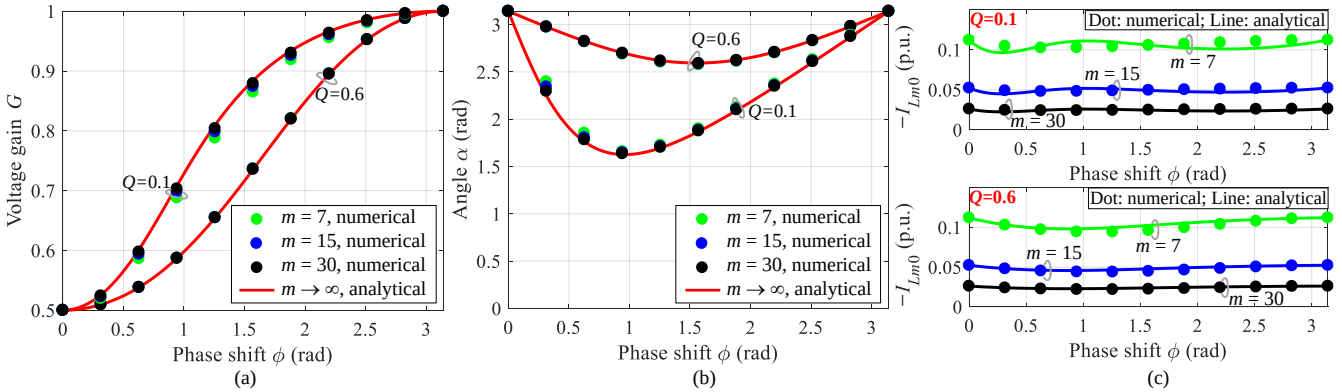


Fig. 7. Numerical and analytical results of (a) the voltage gain G, (b) angle α, and (c) initial magnetizing current I_{Lm0} for the forward operation.

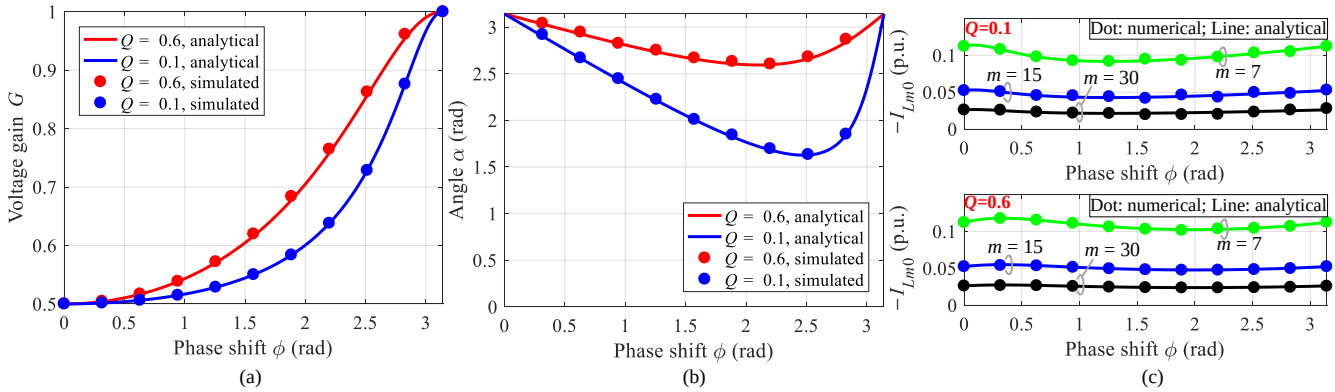


Fig. 8. Simulated and analytical curves of (a) the voltage gain G, (b) angle α (c), and the initial magnetizing current i_{Lm0} for the reverse operation.

$$\begin{cases} i_{Lr}(\theta) = -r_1 \sin\theta \\ u_{Cr1}(\theta) = -r_1 \cos\theta + G \\ i_{Lm}(\theta) = G\theta \,/\, m + I_{Lm0} \end{cases} \tag{6}$$

where $r_1 = G - V_{Cr10}$.

Stage 2 ($\theta \in [\pi-\phi, \alpha]$, see Fig. 2(b), Fig. 5 and Fig. 6): At $\theta = \pi-\phi$, the switch S_6 is turned off, and thus the negative current i_s charges/discharges C_{oss5}-C_{oss7} such that S_7 achieves ZVS-on subsequently. During this stage, the secondary resonant tank voltage u_{cd} equals to half of the secondary port voltage, i.e., $u_{cd} = nV_s/2$; this stage corresponds to the half-bridge mode. Thus, the inductor current i_{Lr} decreases sinusoidally. The normalized mathematic equations for the resonant tank can be expressed as

$$\begin{cases} i_{Lr}(\theta) = -i_{Lr}(\pi-\phi)\cos(\theta+\phi) + r_2 \sin(\theta+\phi) \\ u_{Cr1}(\theta) = i_{Lr}(\pi-\phi)\sin(\theta+\phi) + r_2 \cos(\theta+\phi) + G \,/\, 2 \\ i_{Lm}(\theta) = G(\theta+\phi-\pi) \,/\, (2m) + i_{Lm}(\pi-\phi) \end{cases} \tag{7}$$

where $r_2 = G \,/\, 2 - u_{Cr1}(\pi-\phi)$.

Stage 3 ($\theta \in [\alpha, \pi]$, see Fig. 2(b), Fig. 5 and Fig. 6): The inductor current i_{Lr} decreases to 0 at $\theta = \alpha$, and the antiparallel diode of S_1 turns off with ZCS. Due to the unidirectionality of diodes, reverse resonance is not possible. Thus, both the resonant inductor current i_{Lr} and the resonant capacitor voltage u_{Cr} are prevented from changing. However, the magnetizing inductor is excited by u_{ab}, and therefore i_{Lm} increases linearly, i.e.,

$$\begin{cases} i_{Lr}(\theta) = i_{Lr}(\alpha) \\ u_{Cr1}(\theta) = u_{Cr1}(\alpha) \\ i_{Lm}(\theta) = G(\theta-\alpha) \,/\, (2m) + i_{Lm}(\alpha) \end{cases} \tag{8}$$

During this stage, the secondary resonant tank voltage u_{cd} is still equal to half of the secondary port voltage, i.e., $u_{cd} = nV_s/2$. Therefore, the converter is still operating in the half-bridge mode.

From $\theta = \pi$, the second half-cycle begins and the antiparallel diode of S_2 starts to conduct; thus C_{r1} in series with the primary source V_p is connected in parallel with the resonant capacitor C_{r2}. The equivalent resonant capacitance is still $2C_r$, but the resonant tank voltage $u_{ab} = u_{Cr1} - V_p$, as shown in Figs. 5 and 6.

III. Characteristics

A. Voltage Gain

1) Forward Operation

In the forward mode, the proposed topology operates as an LLC resonant converter. It is impossible to directly derive the analytical solutions. Therefore, numerical analysis is first used to find the solutions, as shown in Fig. 7. It can be observed that the voltage gain range is always from 0.5 to 1 regardless of the quality factor Q and the inductances ratio m. Furthermore, the influence of m on both the gain G and the angle α is negligible, especially at heavy loads (high Q). Therefore, it is justified to let m tend to infinity so that the analytical solutions for G and α can be obtained, i.e.,

$$\begin{cases} G = \dfrac{1}{4(1-\cos\phi)}\left(\begin{array}{l} 2-(2+\pi Q)\cos\phi - 3\pi Q \\ +\sqrt{K_1 + 4\pi Q[(3\pi Q+2)\cos\phi - 2]} \end{array}\right) \\ \alpha = \arccos\left(\dfrac{\begin{array}{l}(4-\pi^2Q^2)\sin^2\phi - [3\pi Q+2+(\pi Q-2) \\ \times\cos\phi]\sqrt{K_1 + 4\pi Q[(3\pi Q+2)\cos\phi - 2]}\end{array}}{2\left(\begin{array}{l}(\pi Q-2)(3\pi Q+2)\cos\phi \\ +\pi Q(5\pi Q+4)+4\end{array}\right)}\right) \end{cases} \quad (9)$$

where $K_1 = [3\pi Q + 2 - (\pi Q + 2)\cos\phi]^2$.

The analytical results for G and α are also shown in Fig. 7(a) and (b). One can see that the error between the analytical and numerical results is negligible. Substituting (9) into (3)-(5) yields the analytical expression for the initial magnetizing current

$$I_{Lm0} = -\frac{1}{4m(1-\cos\alpha)}\left(\begin{array}{l} 2M[2\alpha - \phi + m\sin(\alpha-\phi)] \\ +m(2M-\pi Q-2)\sin\alpha \end{array}\right) \quad (10)$$

Then, the numerical and analytical results for $-I_{Lm0}$ in different cases are plotted in Fig. 7(c). As can be seen, (10) can be used to predict I_{Lm0} with insignificant relative errors. In addition, one can also see that the variations of I_{Lm0} with respect to the phase shift ϕ (or gain G) and the quality factor Q (or power level) are small. The inductances ratio m is the dominant factor which determines I_{Lm0}.

2) Reverse Operation

In the reverse mode, the proposed topology operates as a series resonant converter. Thus, we can directly derive the analytical solutions

$$\begin{cases} G = \dfrac{4\pi Q}{\sqrt{K_2 + 8\pi Q\sin^2\phi} - (2-\pi Q)\cos\phi + 3\pi Q - 2} \\ \alpha = \arccos\left(\dfrac{\begin{array}{l}(4-\pi^2Q^2)\sin^2\phi - [3\pi Q+2+(\pi Q+2) \\ \times\cos\phi]\sqrt{K_2 + 8\pi Q\sin^2\phi}\end{array}}{2\left(\begin{array}{l}(\pi Q+2)(3\pi Q+2)\cos\phi \\ +\pi Q(5\pi Q+8)+4\end{array}\right)}\right) \\ I_{Lm0} = -\dfrac{2\pi-\phi}{4m}G \end{cases} \quad (11)$$

where $K_2 = [3\pi Q + 2 + (\pi Q + 2)\cos\phi]^2$.

The curves for G and α in the reverse operation can be plotted with (11), as shown in Fig. 8. Similarly to the characteristics in the forward operation, the gain range in the reverse operation is also from 0.5 to 1, regardless of the power quality Q (or power P). The difference from the forward operation is that the gain curves in the reverse operation are completely independent of the inductors ratio m. In addition, it can be seen from Fig. 8 that the variation of current I_{Lm0} is also very small when the phase shift ϕ (gain G) or the quality factor Q (power P) changes. The current I_{Lm0} is mainly affected by the inductors ratio m.

The comparison between Fig. 7(c) and Fig. 8(c) shows that the difference of current I_{Lm0} in the forward and reverse operation conditions is small as well. This is beneficial to the selection of m for achieving ZVS in both power flow directions.

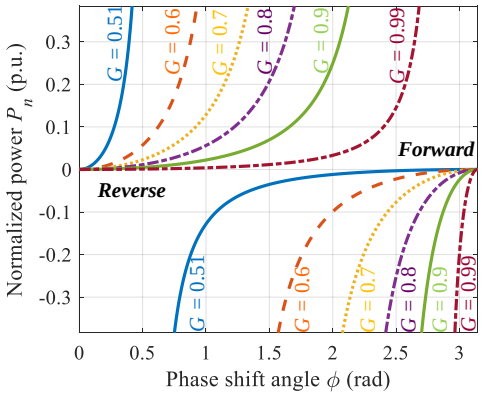


Fig. 9. Characteristics of the transferred power with respect to the phase shift angle ϕ for the forward and reverse power flow directions.

B. Power and Control Scheme

From (9) and (11), the normalized power can be derived for both power flow directions:

$$P_n = \frac{2G}{\pi[G(3+\cos\phi)-2]} \times \begin{cases} (1-G)(1-\cos\phi), & \text{Forward} \\ (1-2G)(1+\cos\phi), & \text{Reverse} \end{cases} \quad (12)$$

Then the characteristics of the power P_n versus the phase shift angle ϕ can be plotted, as shown in Fig. 9. It can be seen that the power is monotonically increasing with respect to the phase shift angle ϕ for both the forward ($P_n > 0$) and reverse ($P_n < 0$) power flow directions. For the voltage gain G in both power flow directions, it is also monotonically increasing with respect to ϕ, as illustrated in Fig. 7 and Fig. 8. Thus, it is possible to use only one PI controller to regulate the power flow in two directions. In the meanwhile, it can be seen from Fig. 9 that the power curves become sharp when the voltage gain G is close to 0.5 or 1. In order to achieve precise power flow control for the bidirectional converter, high performance DSP is required. In this research, the DSP TMS320F28075 with a system clock of 120 MHz is used to implement the control of the proposed converter. The switching frequency f_s is fixed at 100 kHz. The gate signals are generated from the ePWM module operating in the up-and-down count mode. Thus, the period value of the ePWM counter is TBPRD = 120MHz/100kHz/2 = 600. The sharpest power curve occurs when G is closed to 1 or 0.5, as shown in Fig. 9. The normalized full power P_n = 0.385; in the case of G = 0.99 and operating in the reverse mode, the phase shift range for full power range is from 0.94π to π, which corresponds to 600 × (π – 0.94π) / π = 36 steps. Therefore, the power control resolution in the worst scenario is 1000 W/ 36 steps= 27.8 W per step. It represents 27.8 W / 1000 W= 2.78% of the full power. It is acceptable in this research. However, if higher power control resolution is needed, then the HRPWM module in DSP could be used. For example, if a micro edge positioner (MEP) step size of 150 ps is chosen, then an equivalent system clock of 6.7GHz can be achieved. Thus, the power resolution in the worst scenario can be 100 MHz/6.7GHz × 27.8 W/step = 0.42 W/step, which represents 0.42 W/ 1000 W = 0.042% of the full power.

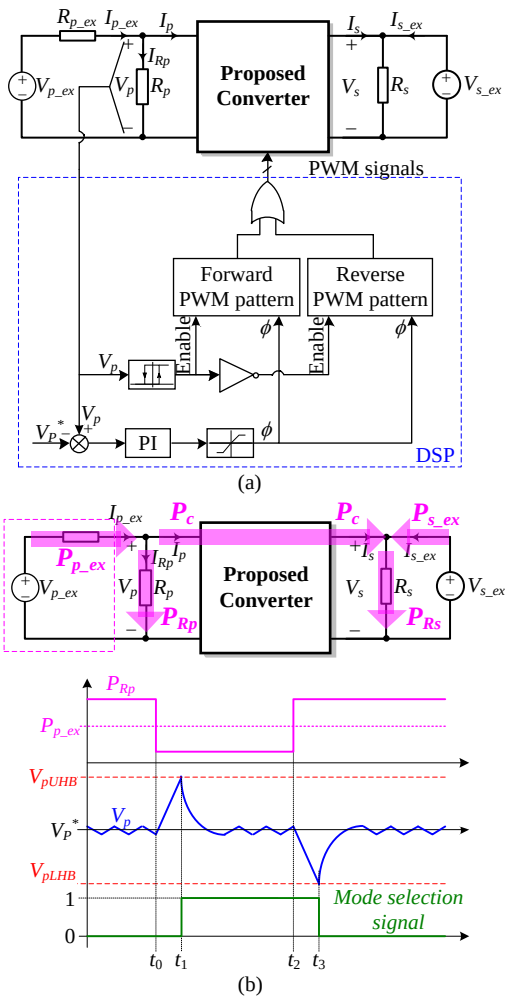


Fig. 10. (a) Experimental setup and control block diagram; (b) theoretical primary-side voltage waveform at operation mode transitions.

The experimental setup and control block diagram are shown in Fig. 10(a). Both the primary and secondary terminals are connected in parallel with a voltage source and a load such that bidirectional power flow operation can be enabled for the proposed converter. By controlling the phase shift angle ϕ, the primary bus voltage can be regulated to its reference V_p^* if the system's power flow direction and the converter's power conversion direction (i.e., forward or reverse mode) are the same.

For the proposed dc-dc converter, the switching patterns in two power flow directions are different. Therefore, a decision algorithm of power flow direction is required to select the power conversion mode (i.e., either forward mode or reverse mode) of the bidirectional dc-dc converter. In this paper, a digital hysteresis comparator based on the primary-side voltage V_p is adopted to determine the forward or reverse operation of the converter. The theoretical waveforms of the experimental setup are shown in Fig. 10(b). Normally, the primary side voltage V_p is regulated to its reference V_p^* when the steady state is reached. Thus, the primary-side external voltage source V_{p_ex} in series with the resistor R_{p_ex} can be seen as a constant power source: $P_{p\_ex} = V_p^*(V_{p\_ex} - V_p^*)/R_{p\_ex}$. Before t_0, the power P_{Rp} is greater than P_{p_ex}, and the converter operates in the reverse mode ($P_c < 0$). At t_0, the resistor R_p is increased and P_{Rp} becomes smaller than P_{p_ex}, but the converter still operates in the reverse mode; thus the primary-side voltage V_p drastically increases because power is transferred to the primary-side capacitor from two sides: the converter side and the primary side. At t_1, V_p reaches the upper hysteresis band V_{pUHB}. Then the forward PWM pattern is enabled and the converter begins to operate in the forward mode with the closed-loop control. Subsequently, the primary-side voltage V_p can be regulated to the reference V_p^*. For the transition from the forward mode to the reverse mode within $[t_2, t_3]$, the operation principle is similar and therefore is not repeated.

C. Soft-Switching

As mentioned in Section II, in the forward mode, S_1–S_2 and S_7–S_8 can achieve ZVS-on, and the anti-parallel diodes of S_3–S_6 turn off with ZCS; in the reverse mode, S_3–S_8 can achieve ZVS-on, and the anti-parallel diodes of S_1–S_2 operate under ZCS. In practice, however, the realization of ZVS requires enough charges to fully charge/discharge the output capacitances of power MOSFETs. Due to the symmetry of circuit and modulation, only the commutations during the half switching cycle $\theta \in [0, \pi]$ are analyzed in this paper. For the proposed converter operating in both power flow directions, there are four ZVS mechanisms, as shown in Fig. 11. In order to quantify the required amount of charges for each commutation mode, detailed state analysis for the half switching cycle $\theta \in [0, \pi]$ is presented in Table I, where C_{oss12} denotes the output capacitance of S_1 and S_2, $C_{oss3\text{-}6}$ represents the output capacitance of S_3–S_6, and C_{oss78} is the output capacitance of S_7 and S_8. The value of u_{cd} at $\theta = 0$ is denoted as V_{cd0}, and in the forward operation it can be obtained by

$$V_{cd0} = \frac{m}{m+1}(V_{Cr10} - V_p) = \frac{mV_p(\pi Q - 2)}{4(m+1)} \quad (13)$$

In the forward operation, the ZVS-on of S_1 depends on the current I_{Lm0}, whereas the ZVS-on of S_8 is determined by i_s during the deadtime interval between S_2 and S_8, which can be designed long enough. This implies that that the ZVS condition of S_1 is more strict. In the reverse operation, the ZVS-on of S_3 and S_7 depends on the currents I_{Lm0} and $i_s(\pi\text{-}\phi)$, respectively. The inductors ratio m has a direct impact on the peak magnetizing current I_{Lm0}, and therefore determines the ZVS realizations of S_1–S_2 (in the forward operation) and S_3–S_6 (in the reverse operation). In the meanwhile, it can be seen from Table I that the required minimum charges for S_1–S_2 (in the forward operation) and S_3–S_6 (in the reverse operation) are

$$\begin{cases} q_{reqI} = 2V_pC_{oss12}, & \text{Forward} \\ q_{reqIII} = \max\{2V_sC_{oss3\text{-}6}, V_s(C_{oss3\text{-}6} + 0.5C_{oss78})\}, & \text{Reverse} \end{cases}, \quad (14)$$

respectively.

The current I_{Lm0} can be assumed to be constant during the deadtime interval t_d which is short compared to the switching period.

In order to achieve ZVS, the conditions in (15) should be satisfied

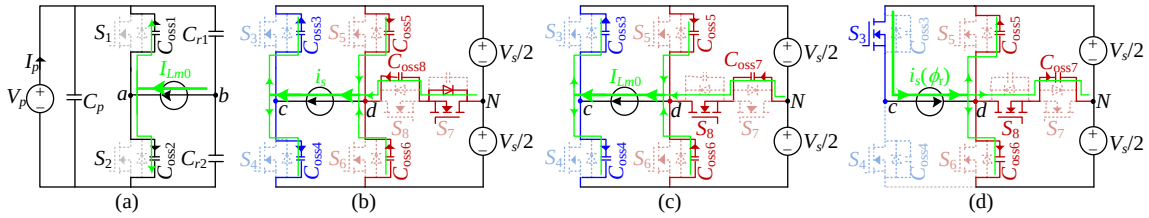


Fig. 11. Mechanisms of ZVS in both power flow directions (cf. Fig. 2). (a) Commutation I: ZVS-on of S_1 in the forward operation; (b) Commutation II: ZVS-on of S_8 in the forward operation; (c) Commutation III: ZVS-on of S_3 and S_6 in the reverse operation; (d) Commutation IV: ZVS-on of S_7 in the reverse operation.

TABLE I
REQUIRED MINIMUM CHARGE TO ACHIEVE ZVS FOR DIFFERENT SWITCH LEGS

Operation mode	Commutation mode	Current to achieve ZVS	Charged/discharged capacitor		Initial voltage	Final voltage	Absolute charge variation of a capacitor	Charge variation of a HB/T-type leg	Minimum charge q_{req} for ZVS-ON of all switches
Forward	I (cf. Fig. 11(a))	I_{Lm0}	HB leg	C_{oss1}	V_p	0	V_pC_{oss12}	$2V_pC_{oss12}$	$\boldsymbol{q_{reqI} = 2V_pC_{oss12}}$
				C_{oss2}	0	V_p	V_pC_{oss12}		
	II (cf. Fig. 11(b))	i_s	HB leg	C_{oss3}	$0.5V_s - 0.6V_{cd0}$	0	$(0.5V_s–0.6V_{cd0})C_{oss3\text{-}6}$	$(V_s–1.2V_{cd0})C_{oss3\text{-}6}$	$\boldsymbol{q_{reqII} = \max\{(V_s–1.2V_{cd0})C_{oss3\text{-}6}, –V_{cd0}(0.8C_{oss3\text{-}6}+0.4C_{oss78})\}}$
				C_{oss4}	$0.5V_s + 0.6V_{cd0}$	V_s	$(0.5V_s–0.6V_{cd0})C_{oss3\text{-}6}$		
			T-type leg	C_{oss5}	$0.5V_s + 0.4V_{cd0}$	$0.5V_s$	$– 0.4V_{cd0}C_{oss3\text{-}6}$	$– V_{cd0}$ $(0.8C_{oss3\text{-}6}+0.4C_{oss78})$	
				C_{oss6}	$0.5V_s – 0.4V_{cd0}$	$0.5V_s$	$– 0.4V_{cd0}C_{oss3\text{-}6}$		
				C_{oss7}	0	0	0		
				C_{oss8}	$0.4V_{cd0}$	0	$– 0.4V_{cd0}C_{oss78}$		
Reverse	III (cf. Fig. 11(c))	I_{Lm0}	HB leg	C_{oss3}	V_s	0	$V_sC_{oss3\text{-}6}$	$2V_sC_{oss3\text{-}6}$	$\boldsymbol{q_{reqIII} = \max\{2V_sC_{oss3\text{-}6}, V_s(C_{oss3\text{-}6}+0.5C_{oss78})\}}$
				C_{oss4}	0	V_s	$V_sC_{oss3\text{-}6}$		
			T-type leg	C_{oss5}	$0.5V_s$	V_s	$0.5V_sC_{oss3\text{-}6}$	$V_s(C_{oss3\text{-}6}$ $+0.5C_{oss78})$	
				C_{oss6}	$0.5V_s$	0	$0.5V_sC_{oss3\text{-}6}$		
				C_{oss7}	0	$0.5V_s$	$0.5V_sC_{oss78}$		
				C_{oss8}	0	0	0		
	IV (cf. Fig. 11(d))	$i_s(\pi\text{-}\phi)$	HB leg	C_{oss3}	0	0	0	0	$\boldsymbol{q_{reqIV} = V_s(C_{oss3\text{-}6}+0.5C_{oss78})}$
				C_{oss4}	V_s	V_s	0		
			T-type leg	C_{oss5}	V_s	$0.5V_s$	$0.5V_sC_{oss3\text{-}6}$	$V_s(C_{oss3\text{-}6}$ $+0.5C_{oss78})$	
				C_{oss6}	0	$0.5V_s$	$0.5V_sC_{oss3\text{-}6}$		
				C_{oss7}	$0.5V_s$	0	$0.5V_sC_{oss78}$		
				C_{oss8}	0	0	0		

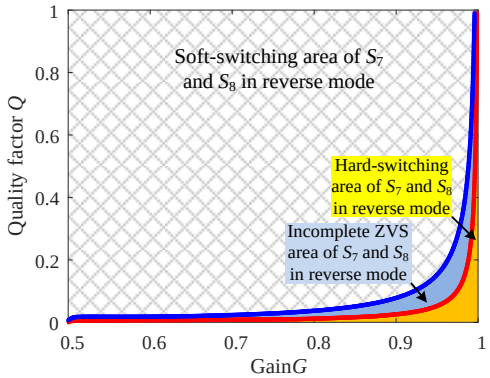


Fig. 12. Hard-switching and incomplete ZVS areas of S_7 and S_8 in the reverse operation.

$$\begin{cases} \left|I_{Lm0}\right| t_d = -I_{Lm0}t_d > q_{reqI}, & \text{forward mode} \\ \left|I_{Lm0}\right| t_d = -I_{Lm0}t_d > q_{reqIII}, & \text{reverse mode} \end{cases} \quad (15)$$

Then, from (10), (11), (14) and (15), the selection criterion for the inductors ratio m can be obtained, i.e.,

$$m < \min\left\{ \frac{2(\phi-2\alpha)t_dV_s \,/\, Z_r}{\left(\begin{array}{l} t_d(2G-\pi Q-2)\sin\alpha \\ -4q_{reqI}(1-\cos\alpha) \\ +2Gt_d\sin(\alpha-\phi) \end{array}\right)}, \frac{(2\pi-\phi)t_dV_s}{4q_{reqIII}Z_r} \right\} \quad (16)$$

where α can be derived by (10) and (11).

As illustrated in Table I, the ZVS realization of S_7 and S_8 in the reverse operation relies on the currents $i_s(\pi\text{-}\phi)$ which can be expressed as

$$i_s(\pi-\phi) = -\frac{V_p}{Z_r}[I_{Lm0} + G(\pi-\phi)\,/\,m + r_1\sin\phi] \quad (17)$$

From the analysis on commutation mode IV in Table I, the required charge to achieve a complete ZVS for S_7 is

$$q_{reqIV} = V_s(C_{oss3\text{-}6} + 0.5C_{oss78}) \quad (18)$$

Then, the ZVS condition for S_7 and S_8 can be derived

$$\left|i_s(\pi-\phi)\right| t_d = -i_s(\pi-\phi)t_d > q_{reqIV} \quad (19)$$

Assume that all output capacitors have the same value C_{oss}, and then (18) can be rewritten as

$$q_{reqIV} = 1.5V_sC_{oss} \quad (20)$$

Based on (17), (19) and (20), the hard-switching ($–i_s(\pi\text{-}\phi) < 0$) and incomplete ZVS ($0 < –i_s(\pi\text{-}\phi) < q_{reqIV}/t_d$) regions for S_7 and S_8 can be derived at $m = 7$, as shown in Fig. 12. As can be seen, the hard-switching and incomplete ZVS regions are small compared to the complete ZVS area. It is worth noting that the voltage stress of S_7 and S_8 is only $0.5V_s$. Therefore, the capacitive switching-on energy loss is $0.5C_{oss}(0.5V_s)^2 = 0.125C_{oss}V_s^2$, which is relatively small even when operating in the hard-switching region.

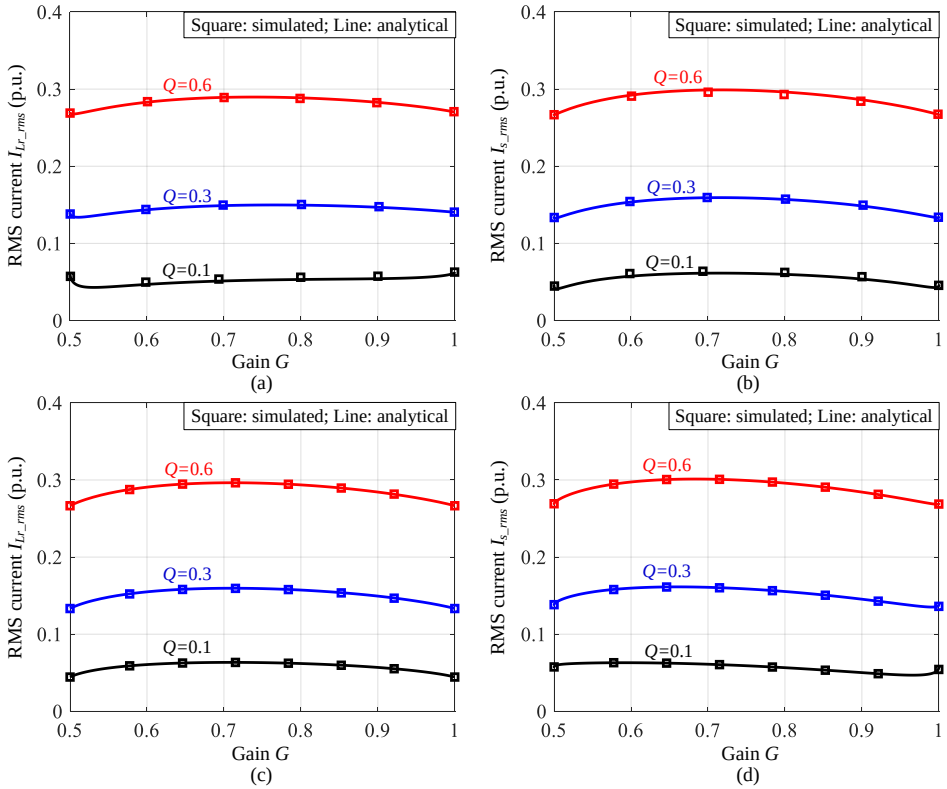


Fig. 13. Analytical and simulated RMS currents with respect to the voltage gain for different quality factors (power levels) (a) RMS characteristics of the resonant current in the forward operation; (b) RMS characteristics of the secondary transformer current (referred to the primary side) in the forward operation; (c) RMS characteristics of the resonant current in the reverse operation; (d) RMS characteristics of the secondary transformer current (referred to the primary side) in the reverse operation.

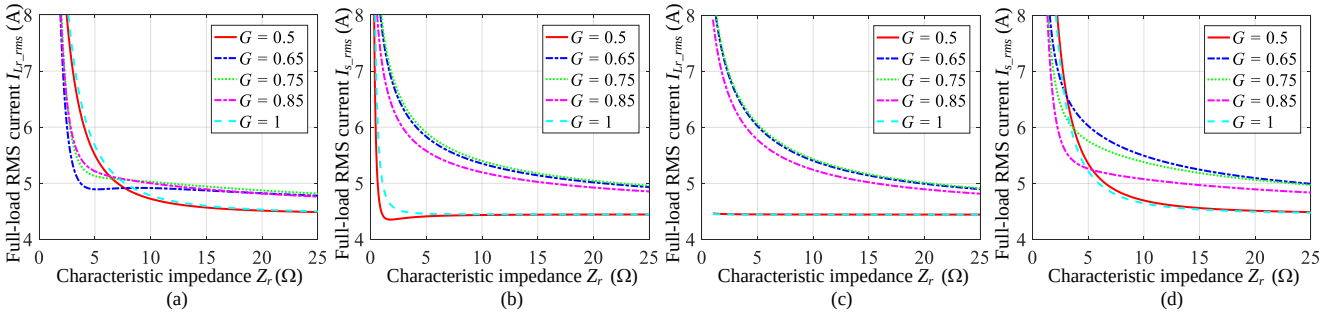


Fig. 14. Full-load RMS current curves with respect to the characteristic impedance Z_r in different gain cases. (a) RMS characteristics of the resonant current in the forward operation; (b) RMS characteristics of the secondary transformer current (referred to the primary side) in the forward operation; (c) RMS characteristics of the resonant current in the reverse operation; (d) RMS characteristics of the secondary transformer current (referred to the primary side) in the reverse operation.

D. Root-Mean-Square Currents

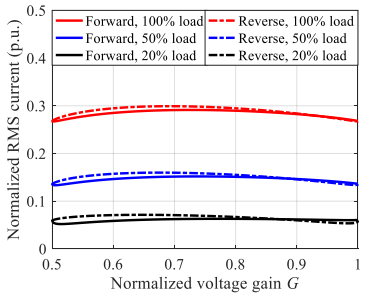
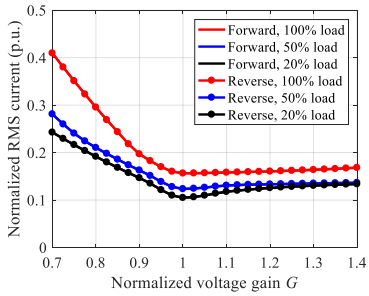
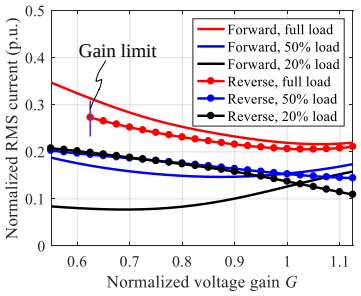
The analytical and simulated RMS current curves with respect to the voltage gain for different quality factors are plotted in Fig. 13. As can be seen, the analytical results coincide pretty well with the simulations. In addition, the obtained results show that both the primary and the secondary transformer RMS currents do not significantly vary with respect to the voltage gain G. This means that the conduction losses can be always kept relatively low over a wide voltage gain range.

When the transferred power is specified, the characteristic impedance Z_r has a significant impact on the RMS current characteristics. The full-load (1 kW) case is considered herein, and Fig. 14 shows the full-load RMS current curves. As can be observed, the full-load RMS currents decrease with respect to the increase of the characteristic impedance Z_r except for some special cases, i.e., G = 0.5 and G = 1 in Fig. 14(b) and (c). Therefore, from the point of view of minimizing conduction losses, the characteristic impedance Z_r should be designed as large as possible. Also, when the resonant frequency is specified, a larger Z_r means a larger L_r, which is beneficial to the ZVS realization and the short-circuit current suppression. However, on the other hand, a larger Z_r also leads to a larger ac voltage ripple and a higher voltage peak for the resonant capacitor. Therefore, a trade-off should be made in practice.

E. Topology Comparison

Table II presents a comparison among the proposed bidirectional resonant dc-dc converter, the dual-magnetizing-inductor (DMI) bidirectional LLC topology [22], and the bidirectional CLLLC topology [7], [21]. As can be noticed, the proposed topology uses the same number of switches as the

TABLE II
COMPARISON AMONG THREE BIDIRECTIONAL RESONANT DC-DC CONVERTER TOPOLOGIES

		Proposed topology	DMI bidirectional LLC topology in [22]		Bidirectional CLLLC topology in [7], [21]
Number of switches		8	8		8
Number of capacitors		2	1		2
Number of transformer		1	1		1
Number of inductors		Resonant inductor ×1 Magnetizing inductor (transformer) ×1	Resonant inductor ×1 Magnetizing inductor (transformer) ×1 Additional magnetizing inductor ×1		Resonant inductor ×2 Magnetizing inductor (transformer) × 1
Voltage stress of switches		6 *switches*: input/output bus voltage 2 *switches*: half of the bus voltage	8 *switches*: input/output bus voltage		8 *switches*: input/output bus voltage
Normalized RMS current flowing through transformer at different operating conditions					
Frequency variation range		Fixed-frequency	Moderate		Wide
ZVS range	**Forward**	S_1-S_2, S_7-S_8: full-range ZVS-on; S_3-S_6: full-range ZCS-off;	$G \geq 1$	S_1-S_4: full-range ZVS-on; S_5-S_8: full-range ZCS-off;	S_1-S_4: full-range ZVS-on; S_5-S_8: full-range ZCS-off;
			$G < 1$	S_1-S_4: partially ZCS-on and partially hard-switching; S_5-S_8: full-range ZVS-on	
	Reverse	S_1-S_2, full-range ZCS-off; S_3-S_6: full-range ZVS-on; S_7-S_8: almost full-range ZVS except a small range (cf. Fig. 12).	$G \geq 1$	S_1-S_4: full-range ZVS-on; S_5-S_8: partially ZCS-on and partially hard-switching;	S_1-S_4: full-range ZCS-off; S_5-S_8: full-range ZVS-on;
			$G < 1$	S_1-S_4: full-range ZCS-off; S_5-S_8: full-range ZVS-on;	

other two topologies. But the numbers of inductors are different: the topologies in [22] and [21] requires an external magnetizing inductor and an additional resonant inductor, respectively. For the voltage stress of switches, two of the eight switches in the proposed topology withstand only half of the input/output bus voltage. This is different from other two topologies where all the eight switches have to withstand the full input/output bus voltage.

Since all the three topologies in Table II have multiple resonant elements, and their primary and secondary switches do not share the same current stress, the RMS current flowing through the transformer is used as the comparison criteria. It should be noted that the parameters in [22] and [7] are used to derive the normalized RMS currents for the DMI bidirectional LLC converter and the CLLLC topology, respectively. In order to have a relatively wide operating voltage gain in both the forward and reverse power flow directions, the parameters of the CLLLC topology have to be designed asymmetrically in [7]. Therefore, there is a significant difference between forward and reverse RMS currents. As can be seen from the three figures in Table II, the proposed topology has the smallest RMS current variation with respect to the voltage gain G. Particularly, when the load becomes light, the RMS current of the proposed topology proportionally decreases in the whole gain range; whereas the light-load RMS currents of the other two topologies are still kept high because of the high circulating current. In order to have a wide gain range, the two bidirectional topologies in [22] and [7] have to use a small magnetizing inductance which in turn causes a high circulating current (reactive power) inside the converter. The impact of circulating current on the RMS current and efficiency is particularly high at light loads. Therefore, the measured light-load efficiency performance in [7] is poor. However, for the proposed converter, the switching frequency is fixed and the magnetizing inductance has no impact on the gain range. Therefore, the magnetizing inductance can be designed possibly large on the premise of achieving ZVS. It should be noted that both the RMS current and the conduction losses of primary switches in the proposed topology can be halved if the half-bridge is replaced with a full-bridge on the primary side.

Another disadvantage of the bidirectional CLLLC converter is that the switching frequency range is wide (e.g., 40kHz to 200 kHz) when a wide gain range is needed. Thus, the optimal design of passive components becomes a challenge. The proposed converter can achieve full-range ZVS except a small range for S_7-S_8 in the reverse operation. However, for the DMI bidirectional LLC converter, its soft-switching range is relatively narrow, as illustrated in Table II. Theoretically the bidirectional CLLLC resonant converter can achieve full-range soft-switching; in practice, however, when the switching

frequency becomes high, the peak magnetizing current will be decreased which may be unable to fully charge/discharge the output capacitors of MOSFETs and causes incomplete ZVS transitions.

IV. Experimental Verifications

A 1-kW converter prototype has been built, as shown in Fig. 15. The detailed prototype parameters are listed in Table III. For the reverse diode characteristics SiC MOSFETs, the diode forward voltage is high when the gate-source voltage u_{gs} is zero. In order to reduce the conductions losses, the synchronous rectification is adopted in both power flow directions.

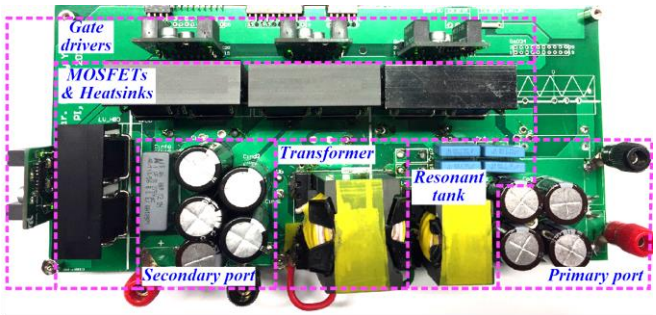
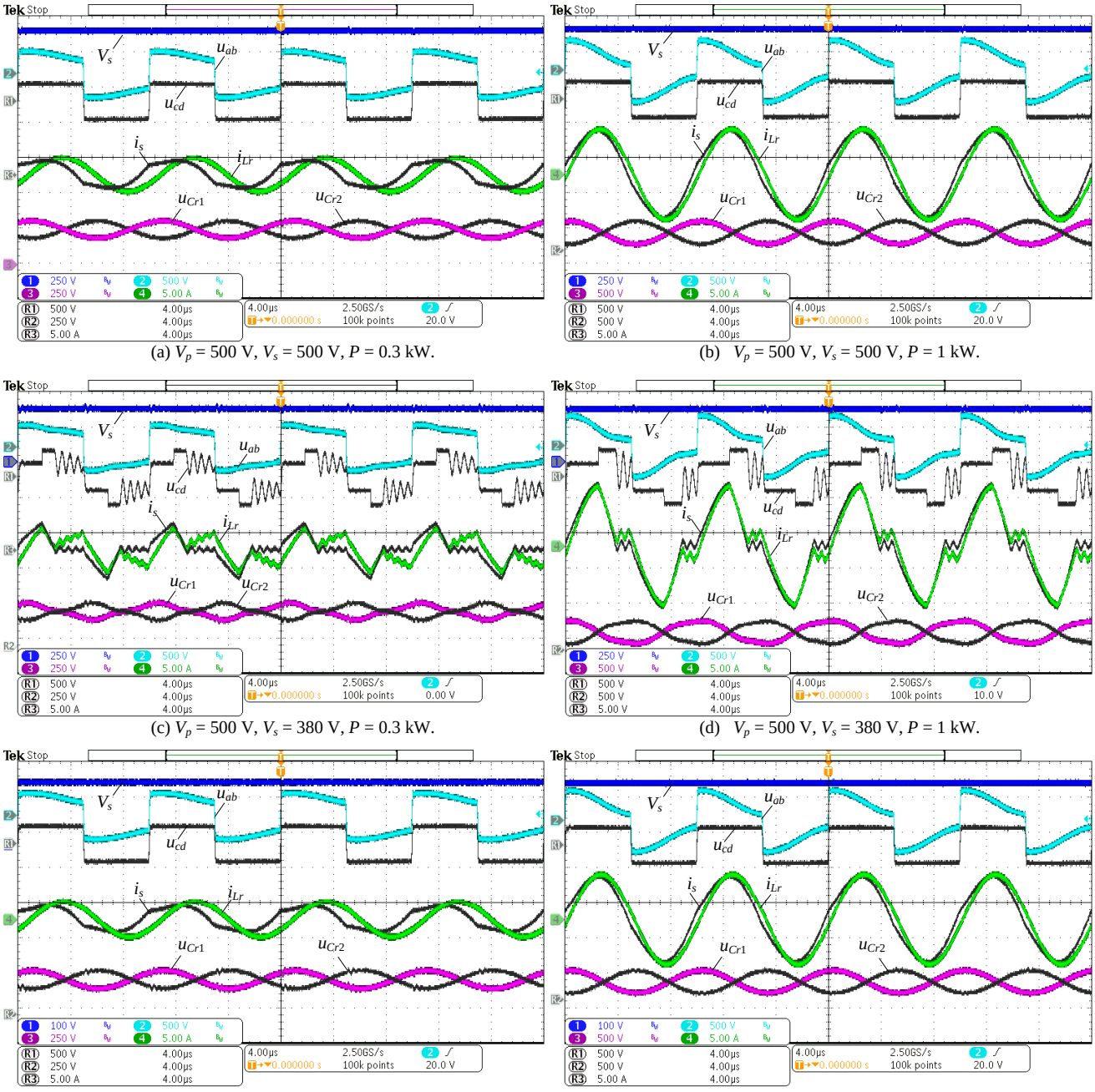


Fig. 15. Photo of the built converter prototype.



(a) V_p = 500 V, V_s = 500 V, P = 0.3 kW.

(b) V_p = 500 V, V_s = 500 V, P = 1 kW.

(c) V_p = 500 V, V_s = 380 V, P = 0.3 kW.

(d) V_p = 500 V, V_s = 380 V, P = 1 kW.

(e) V_p = 500 V, V_s = 250 V, P = 0.3 kW.

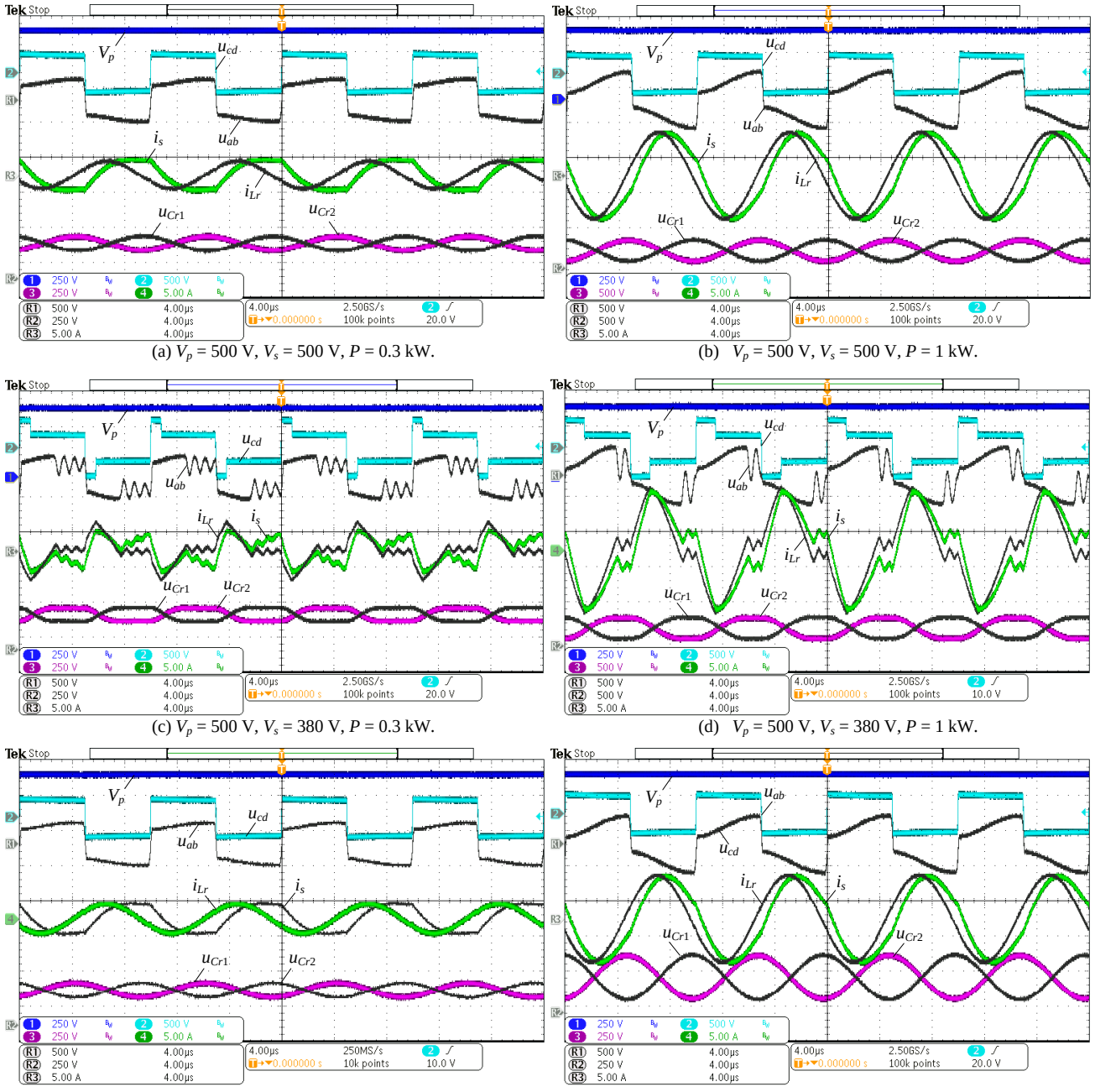
(f) V_p = 500 V, V_s = 250 V, P = 1 kW.

Fig. 16. Steady-state operating waveform in the forward power flow direction.

TABLE III
CONVERTER PARAMETER

Description	Symbol	Parameter
Primary voltage	V_p	500 V
Secondary voltage	V_s	250-500 V
Rated power	P	1 kW
Switching frequency	f_s	100 kHz
Resonant frequency	f_r	100 kHz
Power switches	S_1–S_8	C3M0120090D
Transformer turns ratio	n	1
Magnetizing inductance	L_m	270 μH
Resonant Inductor	L_r	38.4 μH
Resonant capacitors	C_{r1}, C_{r2}	33 nF, film capacitor

The forward steady-state operation of the proposed converter is tested for different secondary voltages and different power levels, as shown in Fig. 16. As can be seen, all the waveforms coincide with the theoretical analysis in Section II except for the high-frequency oscillations during the idle time, which is caused by the parasitic intrawinding capacitance of the transformer and the output capacitance of MOSFETs. At the two boundaries of the secondary voltage range, i.e., V_s = 250 V and V_s = 500 V, the secondary switches form a half-bridge and a full-bridge rectifier, respectively. Thus, the resonant voltages and current are pure sinusoidal waveforms. When the secondary voltage V_s is between the two boundaries, the phase shift ϕ is



(a) V_p = 500 V, V_s = 500 V, P = 0.3 kW.

(b) V_p = 500 V, V_s = 500 V, P = 1 kW.

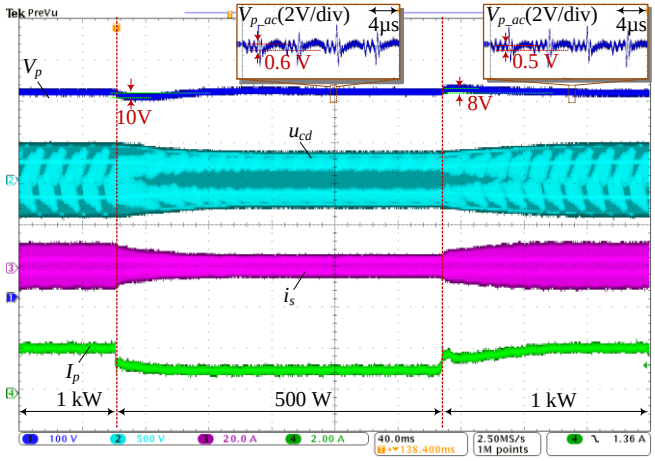
(c) V_p = 500 V, V_s = 380 V, P = 0.3 kW.

(d) V_p = 500 V, V_s = 380 V, P = 1 kW.

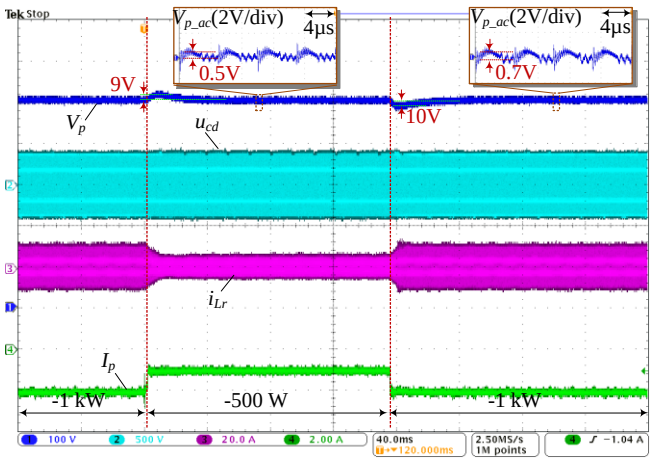
(e) V_p = 500 V, V_s = 250 V, P = 0.3 kW.

(f) V_p = 500 V, V_s = 250 V, P = 1 kW.

Fig. 17. Steady-state operating waveform in the reverse power flow direction.

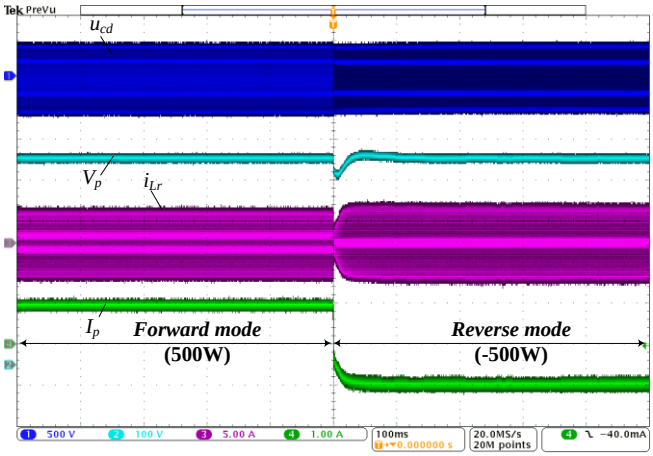


(a) Forward operation

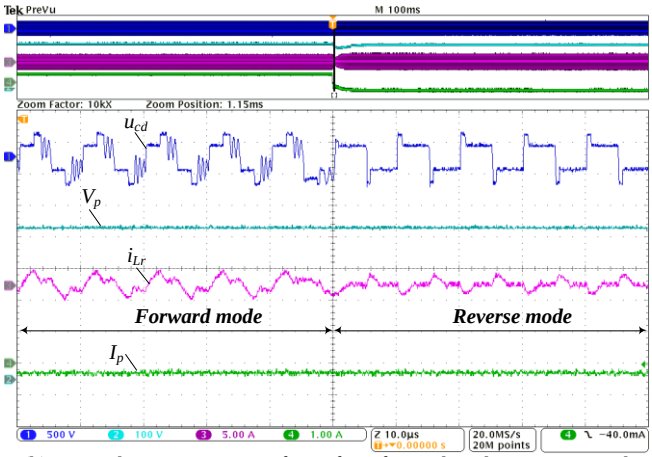


(b) Reverse operation

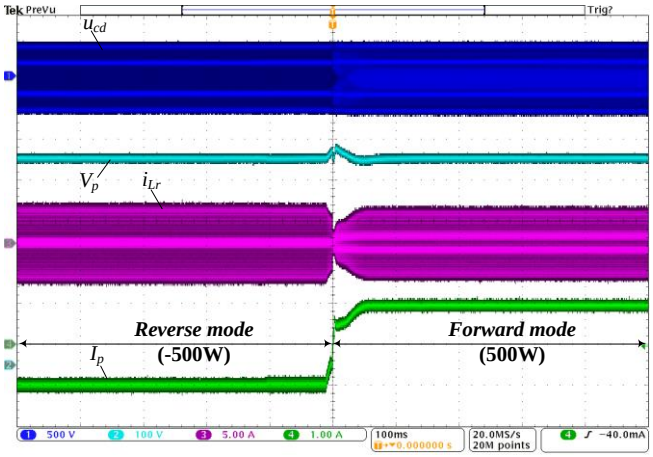
Fig. 18. Dynamic experimental waveforms for both power flow directions.



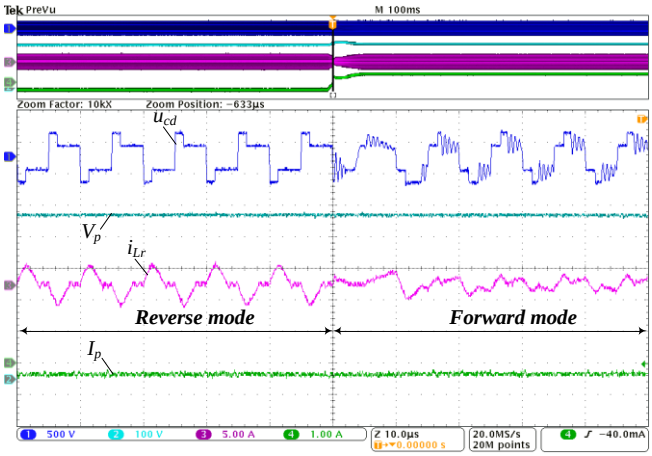
(a) Forward mode to reverse mode



(b) Zoomed-in transition waveforms from forward mode to reverse mode



(c) Reverse mode to forward mode

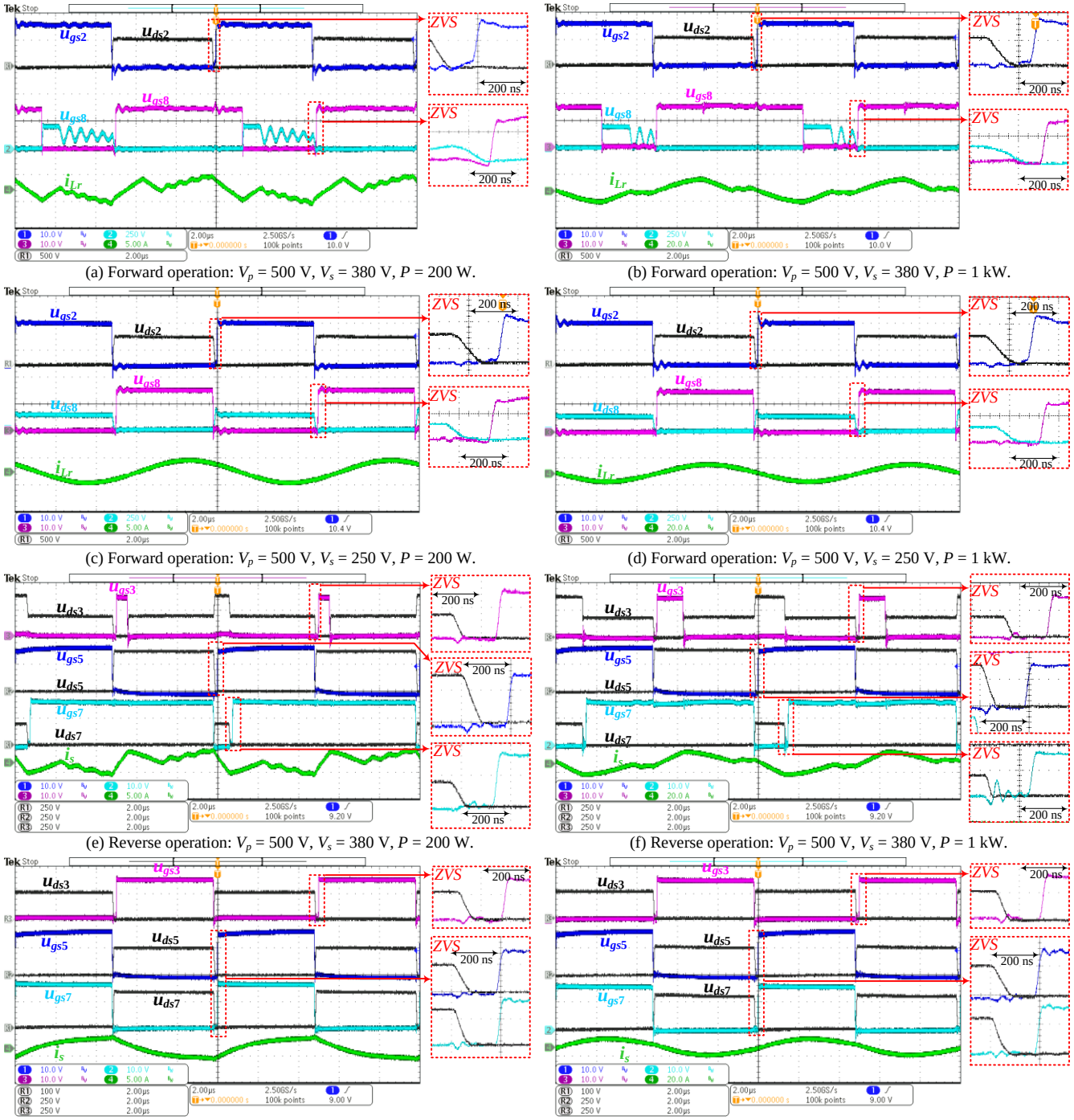


(d) Zoomed-in transition waveforms from reverse mode to forward mode

Fig. 19. Mode transition between forward and reverse modes.

between 0 and π, and the secondary switches constitute a hybrid-bridge rectifier. In this case, the resonant capacitor voltages (u_{Cr1} and u_{Cr2}) and the resonant current (i_{Lr}) are piecewise. One can also see that for the same transferred power, the peak values of the resonant current i_{Lr} and the secondary current i_s do not remarkably vary with respect to the change of the secondary voltage. Therefore, the conduction losses can also be kept relatively low in spite of a wide voltage gain range.

The steady-state operating waveforms of the proposed converter in the reverse operation are measured for different voltages and power levels, as shown in Fig. 17. It can be seen that the experimental results show a good agreement with the theoretical analysis. The secondary switches can form a hybrid-bridge inverter to cope with the secondary voltage variation such that the RMS currents can be kept relatively low.



(a) Forward operation: V_p = 500 V, V_s = 380 V, P = 200 W.

(b) Forward operation: V_p = 500 V, V_s = 380 V, P = 1 kW.

(c) Forward operation: V_p = 500 V, V_s = 250 V, P = 200 W.

(d) Forward operation: V_p = 500 V, V_s = 250 V, P = 1 kW.

(e) Reverse operation: V_p = 500 V, V_s = 380 V, P = 200 W.

(f) Reverse operation: V_p = 500 V, V_s = 380 V, P = 1 kW.

(g) Reverser operation: V_p = 500 V, V_s = 250 V, P = 200 W.

(h) Reverse operation: V_p = 500 V, V_s = 250 V, P = 1 kW.

Fig. 20. Soft-switching waveforms.

In order to verify the converter dynamic performance with the control scheme in Fig. 10, both the primary and secondary bus terminals are connected in parallel with a resistor (load) and a nonideal unidirectional dc voltage source (i.e., a voltage source in series with a resistor and a diode). Thus, both the primary and secondary port can release (by the voltage source) and absorb (by the resistor) power. With the closed-loop control, the dynamic experimental waveforms for both power flow directions are shown in Fig. 18. The given voltage reference V_p^* is equal to 500 V. As can be seen, the primary voltage V_p can be regulated to its reference when the load changes. Also, the observed maximum voltage overshoot is around 10 V which is 2% of the primary voltage V_p = 500 V. For the AC voltage ripple of V_p, i.e., V_{p_ac}, the measured maximum value is approximately 0.7 V which represents 0.14% of 500 V.

The mode transition performance is tested under V_p^* = 500 V, V_s = 380 V and P = ± 500 W, as shown in Fig. 19. It can be observed that automatic and fast mode switch can be achieved for the proposed converter with the hysteresis control. When V_p increases to the upper limit V_{pH} (520 V) or decreases to the lower limit V_{pL} (480 V), the indictor of power flow direction is changed. Then, the switching pattern and the resonant-tank

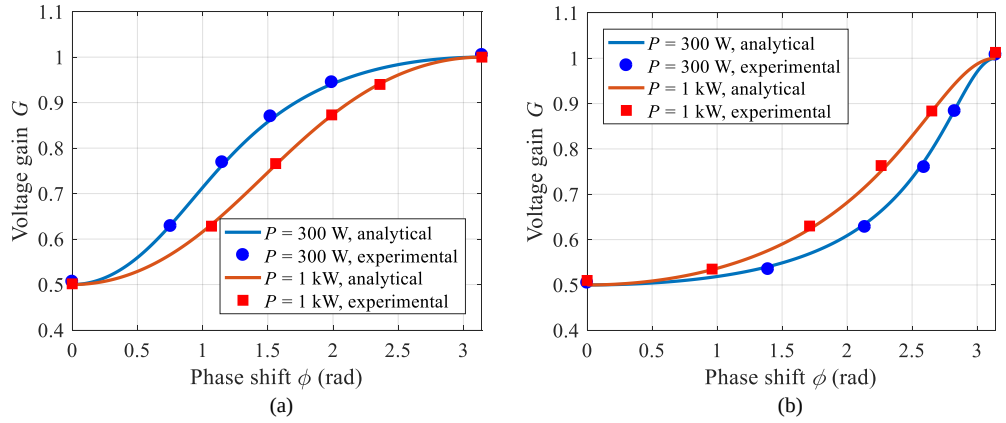


Fig. 21. Comparison between the experimental and analytical gain characteristic: (a) in the forward operation; (b) in the reverse operation.

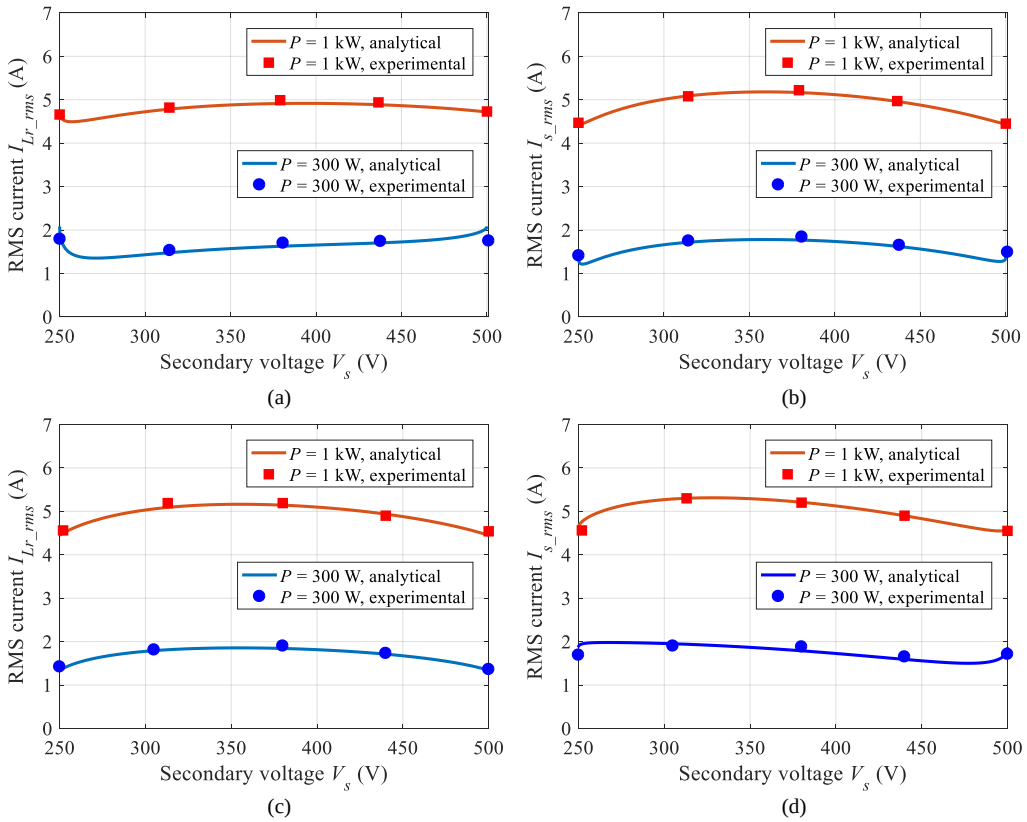


Fig. 22. Comparison between the experimental and analytical rms currents: (a) RMS current I_{Lr_rms} in the forward operation; (b) RMS current I_{s_rms} in the forward operation; (c) RMS current I_{Lr_rms} in the reverse operation; (d) RMS current I_{s_rms} in the reverse operation.

waveforms are switched between the two operating modes, as shown in Fig. 19(b) and (d). As results, the primary-side voltage V_p can be subsequently regulated to the reference V_p* = 500 V and the primary-side current I_p switches between +1A and -1A, indicating that the transferred power P_c transits between +500 W and -500 W.

Fig. 20 presents the soft-switching waveforms in different power and voltage conditions. Due to the symmetry of topology and modulation, only the ZVS waveforms of S_2 and S_8 in the forward operation (Fig. 20 (a)-(d)) and those of S_3, S_5 and S_7 in the reverse operation (Fig. 20 (e)-(h)) are shown in this paper. As one can observed, before the gate driving voltage applies, the corresponding drain-strain voltage have been fallen to zero which implies that ZVS is achieved. Thus, the switching loss is significantly minimized.

The measured gain characteristics in both the forward and reverse power flow directions are compared with the analytical results, as shown in Fig. 21. It can be observed that a good agreement is achieved between the theoretical analysis and experimental results. In addition, one can also see that regardless of the power transfer direction and the power level, a wide gain range of [0.5, 1] can be achieved.

The measured RMS currents in different operating conditions are presented in Fig. 22 to verify the correctness of the derived RMS equations in Table IV. It can be seen that the experimental data matches pretty well with the analytical results. Moreover, Fig. 22 also demonstrates that the variations of RMS currents in the proposed converter are small with respect to a wide secondary voltage range.

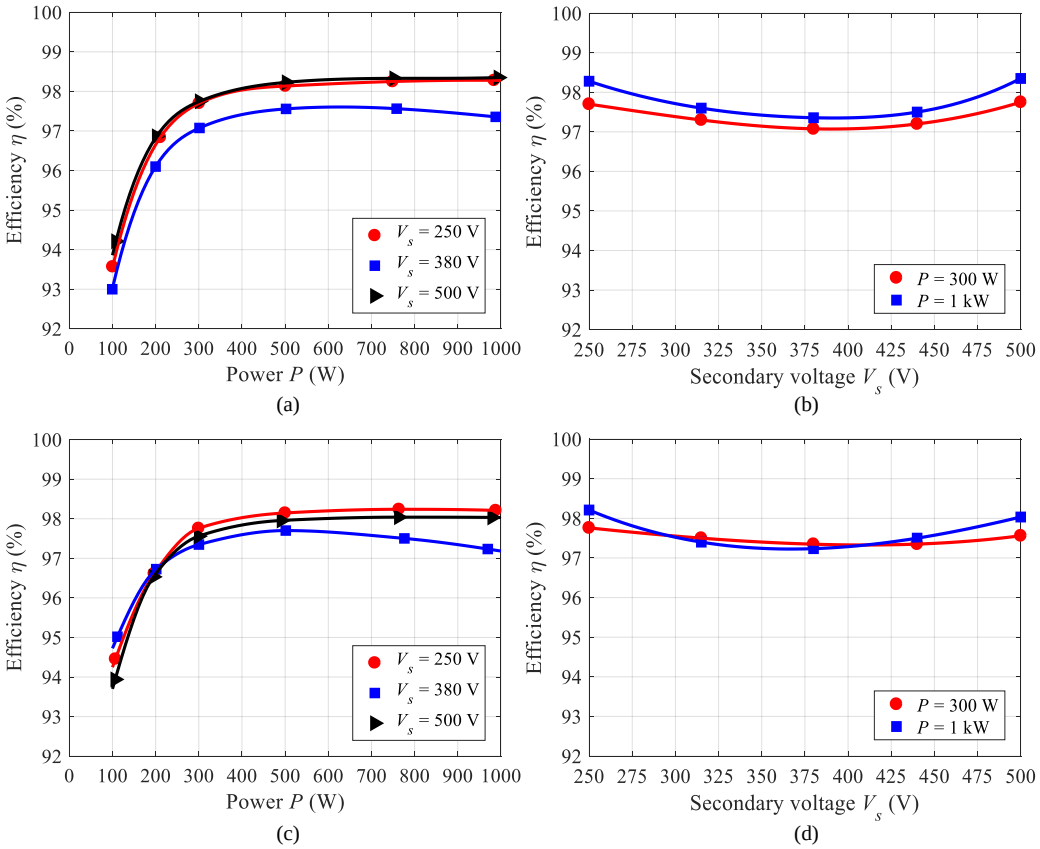


Fig. 23. Measured efficiency curves. (a) forward efficiency with respect to the transferred power at different secondary voltages; (b) forward efficiency with respect to the secondary voltage at different power levels; (c) reverse-mode efficiency with respect to the transferred power at different secondary voltages; (d) reverse-mode efficiency with respect to the secondary voltage at different power levels.

Fig. 23 shows the measured efficiency curves in different operating conditions. As can be seen, high efficiency can be achieved from light loads to the full load, and the peak efficiency reaches 98.3% and 98.2% in the forward and reverse power flow directions, respectively. As analyzed in Section III-C, the proposed bidirectional dc-dc converter can achieve soft-switching. Also, SiC MOSFETs are used to build the converter prototype. Thus, the switching losses are negligible. It is the conduction loss that dominates the total power losses. From Figs. 13 and 22, it can be seen that the RMS currents firstly rise and then fall with respect to the increase of the voltage gain. Thus, the converter has the highest conduction loss and the lowest efficiency in the middle area of the operating voltage range. However, it can be also noticed from Figs. 13 and 22 that the variation of the RMS currents with respect to the voltage gain is small. Therefore, the efficiency performance is kept good in the whole voltage range (efficiency difference is less than 1%, cf. Fig. 23(b) and (d)).

V. Conclusion

In this paper, a new bidirectional resonant dc-dc converter with fixed-frequency phase-shift control is proposed and explored. The operation principles and key characteristics, i.e., the voltage gain, power flow, soft-switching and RMS currents, are detailed. The feasibility of all proposals and the correctness of the theoretical analyses are validated with simulations and experimental results obtained from the built 1-kW converter prototype. A wide gain range from 0.5 to 1 can be achieved for both power flow directions. A significant feature of the proposed converter is that both the forward and reverse RMS currents are kept low in spite of the voltage gain variation. In addition, soft-switching can be achieved for switches, which minimizes the switching losses. Therefore, high-efficiency power conversion can be achieved in the whole operating range.

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