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Performance Evaluation of the Single-Phase Split-Source Inverter Using an Alternative DC-AC Configuration

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***Abstract*—This paper investigates and evaluates the performance of a single-phase split-source inverter (SSI), where an alternative unidirectional dc-ac configuration is used. Such configuration is utilized in order to use two common-cathode diodes in a single-device instead of using two separate diodes, resulting in minimum parasitic inductance in the commutation paths. In this paper, the analysis and modulation of the single-phase SSI using this alternative configuration is discussed, and the analysis of the low frequency component in the dc side is introduced. Moreover, the features behind employing the triangular, the trailing-edge sawtooth, and the leading-edge sawtooth carriers with the single-phase SSI are discussed, and the differences among these carriers are highlighted. In order to highlight the performance of the proposed SSI, a comparative study is conducted with the two-stage architecture and the single-phase quasi-Z-source inverter (qZSI). The introduced analysis is enhanced with simulation results using MATLAB/PLECS models, where a *1-kVA* single-phase SSI is designed and simulated. Finally, the designed *1-kVA* single-phase SSI is implemented experimentally and tested at different operating points, i.e. at different voltage gains, and a maximum efficiency of 95.5% has been obtained.**

***Index Terms*—Discontinuous conduction, Impedance-based inverter, low frequency, Quasi-Z-source inverter, Renewable energy sources, Sawtooth carrier, Single-phase, Single-stage, Split-source inverter, Triangular carrier, Two-stage, Voltage source inverter, Z-source inverter.**

I. Introduction

SINGLE-STAGE dc-ac power conversion systems has undergone a fast evolution during the last few years to replace the conventional two-stage architecture, which includes a front-end dc-dc boost converter (BC) and an output voltage source inverter (VSI) [1], [2]. This evolution has grown up as a way to improve the overall system performance, in terms of reducing its size and complexity [3], [4]. Most of these single-stage topologies and their different modulation schemes have been reviewed in [1], [5], [6]. Among these different single-stage options, the three-phase split-source inverter (SSI) has recently been proposed in [7] as an alternative solution to the commonly used Z-source inverter (ZSI), in order to overcome some of its demerits, like the discontinuity of the input dc current and the dc-link voltage and the high voltage stresses at higher overall voltage gains. This SSI benefits from the following merits:

- continuous dc-link voltage. Hence, it is possible to use high frequency decoupling capacitors across the inverters legs in order to minimize the voltage spikes across the different switches due to the layout parasitic inductances;
- continuous input dc current;
- lower switch voltage stresses for higher overall voltage gains;
- lower passive component-count;
- using only additional input diodes (i.e. no need for additional active switches combined with additional gate drive circuitry compared to the standard VSI);
- using the same standard modulation schemes as the VSI for its basic operation;
- using the same switching states as the VSI (i.e. it does not require extra states to achieve the boosting).

On the other hand, it suffers from the following demerits:

- like the VSI, a sufficient dead band time should be generated;
- higher voltage stresses at lower voltage gains;
- higher current stresses at higher voltage gains;
- unequal current distribution among the different switches;
- high frequency commutations of the input diodes.

Several research activities have considered the SSI, where its three-level operation for three-phase systems using the flying capacitor structure has been investigated in [8], [9]. On the other hand, the authors in [10] discussed the same operation using the diode-clamped structure, showing the possibility of connecting the input dc source to the positive point of the dc-link. Moreover, its closed-loop control in grid-connected mode for renewable energy sources has been discussed in [11], in which the authors have proposed a decoupled control scheme to separately control the SSI dc and ac sides.

The single-phase operation of the SSI has been introduced in [12], [13], where the latter proposes the use of two MOSFETs working in synchronous rectification mode at the fundamental frequency instead of the two input diodes. The use of additional MOSFETs cancels the high frequency commutations of

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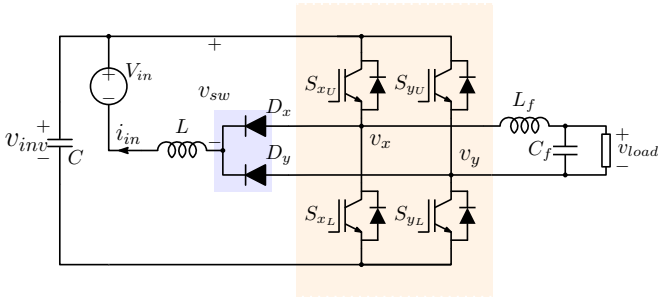


Fig. 1. An alternative configuration of the single-phase split-source inverter (SSI) with an output LC filter, in which two common-cathode diodes in a single-device or two separate diodes can be used.

the input diodes, allows a bidirectional power flow capability, which is not mandatory in several applications, and improves the efficiency due to the low ON resistance. Moreover, additional gate drive circuitry and control signals should be considered, leading to higher complexity and converter volume. On the other hand, the authors in [14] introduce a similar topology to the single-phase SSI, in which two coupled inductors are utilized in order to achieve higher voltage gain due to the system parasitics and the required high duty cycle. It is worth to note that the SSI can achieve a theoretical voltage gain of infinity, but a maximum gain of 4 to 5 can be achieved experimentally like the conventional two-stage architecture. Meanwhile, higher voltage gains can be obtained using means of coupled inductors as in [14].

This paper studies and evaluates the performance of the single-phase SSI, including a dc side low frequency component analysis. In this study, the single-phase SSI modulation using the triangular, the trailing-edge sawtooth, and the leading-edge sawtooth carriers is discussed, and their features are highlighted. Furthermore, the single-phase SSI is compared with the two-stage architecture using a BC-fed single-phase full-bridge VSI and the quasi-Z-source inverter (qZSI).

The work and analysis carried out in this paper utilize an alternative unidirectional single-phase SSI configuration as shown in Fig. 1. In this configuration, the input dc source is connected to the positive point of the dc-link and the diodes are reversed as discussed in [10] for the three-phase three-level diode-clamped SSI. Such configuration with the single-phase operation gives the possibility of using two common-cathode diodes in a single device as an alternative solution to the two separate diodes, i.e. it is possible to use a common-cathode dual-diode package or two separate diodes. The merit behind the common-cathode package is to achieve less parasitic inductance in the commutation path of these diodes, resulting in less voltage spikes across the different switches and enhancing the performance of the SSI. It is worth to note that using MOSFETs as discussed in [13] with the proposed configuration in Fig. 1 does not require any extra isolated gate drives.

The rest of this paper is organized as follows: Section II discusses the operation, modulation, and mathematical derivation of the single-phase SSI configuration shown in Fig. 1. Moreover, the high frequency commutations of the input diodes and influence of carrier signal on improving the system

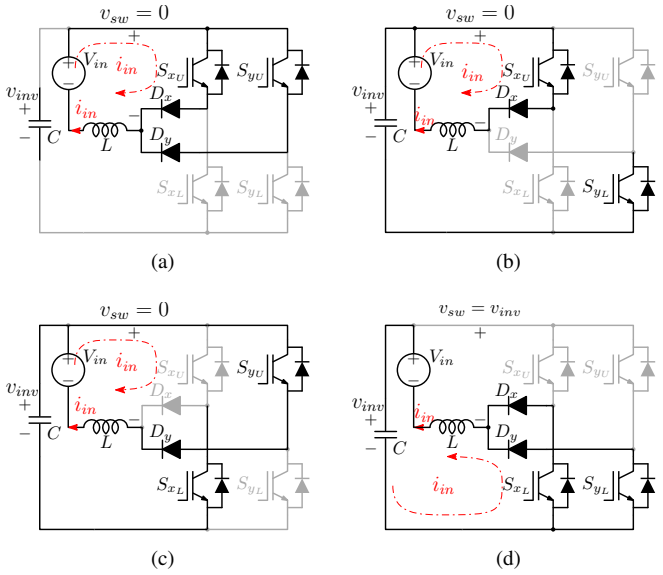


Fig. 2. Different switching states of the alternative single-phase SSI configuration. In each state, "1" indicates that the upper switch is ON. (a) zero state "11"; (b) active state "10"; (c) active state "01"; (d) zero state "00", where L is charging during the first three states and discharging during the last one.

performance are explained and analyzed. Section III compares this single-phase SSI with the two-stage architecture and the single-phase qZSI, in terms of number of required elements, input inductance requirements, and voltage and current stresses. Then, a 1-kVA single-phase SSI is designed and simulated using MATLAB/PLECS models in Section IV. Then, the designed 1-kVA single-phase SSI is implemented experimentally in Section V to validate and verify the reported analysis and simulation results. Finally, conclusions are drawn in Section VI.

II. Analysis of the Single-Phase SSI

This section shows the operation, modulation, and mathematical derivation of the single-phase SSI, considering the configuration shown in Fig. 1. Furthermore, it shows the problem of the SSI input diodes of having high frequency commutations, and studies the effect of utilizing different carrier signals, highlighting their effects on the output ac side.

A. Operation and Modulation

The utilized single-phase SSI configuration, shown in Fig. 1, has a similar operation as the three-phase one proposed in [7]. This single-phase SSI uses the standard B4-bridge and considers its standard four switching states to achieve the boosting operation within the inversion one. The inductor (L) charges when at least one of the upper switches, i.e. S_{x_U} and S_{y_U}, is ON. This corresponds to three different switching states as shown in Fig. 2(a), Fig. 2(b), and Fig. 2(c), where L is charging during the two active states and one of the two zero states, when the two upper switches are simultaneously ON. Meanwhile, it uses the remaining zero state shown in Fig. 2(d), when the lower switches are simultaneously ON, to discharge L and charge the capacitor C.

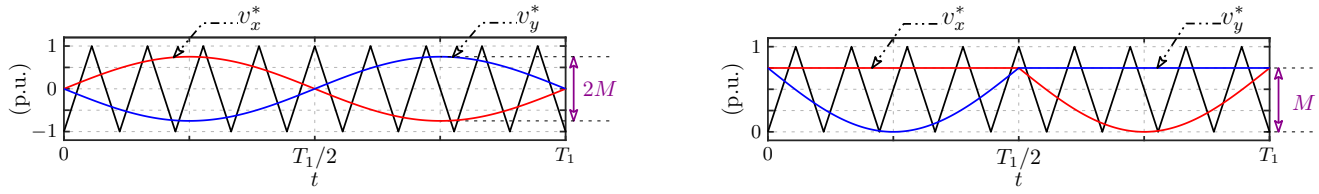


Fig. 3. Alternative single-phase split-source inverter (SSI) modulation schemes for one fundamental cycle of time T_1. (a) sinusoidal pulse width modulation (SPWM) scheme reference signals; (b) modified SPWM (MSPWM) scheme reference signals, where $M = 0.75$ and the modulation-to-fundamental frequency ratio $M_f = 9$.

Such operation can be achieved using the standard sinusoidal pulse width modulation (SPWM) shown in Fig. 3(a), which is a common three-level modulation technique used for the single-phase VSI. Thus, according to Fig. 2 and Fig. 3(a), L charges when the envelope defined by $max(v_x^*, v_y^*)$ is higher than the carrier signal. When this condition is not satisfied, L discharges through the antiparallel diodes of the lower switches into C. This envelope, defined by $max(v_x^*, v_y^*)$ in Fig. 3(a), is continuously oscillating, resulting in an oscillating duty cycle of charging and discharging L, i.e. it increases the low frequency component at the dc side voltage and current. Moreover, it gives high voltage stresses as discussed in [7] for the SPWM used with the three-phase SSI. Thus, the SPWM scheme, shown in Fig. 3(a), is modified as shown in Fig. 3(b), where the modified SPWM (MSPWM) scheme is introduced to have a constant duty cycle of charging and discharging L, and lower voltage stresses by fixing the minimum value of the reference signals at the minimum value of the carrier signal. It is worth to note that the commonly used two-level modulation schemes with the single-phase VSI are not applicable for the single-phase SSI as it does not achieve the required proper operation as discussed before. Moreover, the SPWM has been shown to illustrate the basic operation of the single-phase SSI, but its usage results in a high volume of L due to the increased low frequency component.

B. Mathematical Derivation

The same procedure followed before with the three-phase SSI in [7] is outlined here using the single-phase SSI to derive all the equations needed to properly design the converter using the MSPWM scheme.

According to Fig. 3(b), L charges with a duty cycle $D = M$. Thus, the normalized average dc-link voltage V_{inv}/V_{in} and the normalized output fundamental peak voltage V_φ/V_{in} can be calculated by

$$\frac{V_{inv}}{V_{in}} = \frac{1}{1-M}, \tag{1}$$

$$\frac{V_\varphi}{V_{in}} = \frac{M}{1-M}, \tag{2}$$

where V_{in} is the input dc voltage.

Note that when M is constant, there is a low frequency component in the input current coming out from the low frequency component in the dc-link voltage, which is normal in the single-phase systems [15]–[18]. Such low frequency component in the input current can effectively be mitigated in any closed-loop system as in [19]–[21]. Furthermore, the low frequency component in the dc-link voltage can be mitigated by means of decoupling circuits as discussed in [22].

In order to properly design the dc side passive elements, i.e. proper sizing of L and C, in an open-loop case, the low frequency component in the dc side should be considered with the high frequency one. This low frequency component, which is two times the fundamental frequency (f_1), is due to the output power fluctuation.

1) High Frequency Component: Due to the volt-second balance in the inductor at steady-state, the high frequency peak-to-peak inductor current ripple (ΔI_{L_h}) can be calculated as

$$\Delta I_{L_h} = \frac{M \cdot V_{in}}{f_s \cdot L}, \tag{3}$$

where f_s is the switching frequency. On the other hand, due to the charge balance in the capacitor at steady-state, the high frequency peak-to-peak dc-link voltage ripple (ΔV_{inv_h}) is given by

$$\Delta V_{inv_h} = \frac{(1-M) \cdot I_{in}}{f_s \cdot C}. \tag{4}$$

2) Low Frequency Component: According to [13], the low frequency peak-to-peak dc-link voltage ripple (ΔV_{inv_l}), assuming a constant inductor current, can be estimated by

$$\Delta V_{inv_l} = \frac{2M \cdot I_\varphi}{3\pi^2 \cdot f_1 \cdot C}, \tag{5}$$

where I_φ is the output fundamental peak current.

The low frequency peak-to-peak inductor current ripple (ΔI_{L_l}), which is proportional with the low frequency component in the dc-link voltage (ΔV_{inv_l}), can be estimated by

$$\begin{aligned} \Delta I_{L_l} &= \frac{(1-M) \cdot \Delta V_{inv_l}}{\sqrt{16\pi^2 f_1^2 \cdot L^2 + R_{eq}^2}} \\ &= \frac{2M \cdot (1-M) \cdot I_\varphi}{3\pi^2 \cdot f_1 \cdot C\sqrt{16\pi^2 f_1^2 \cdot L^2 + R_{eq}^2}}, \end{aligned} \tag{6}$$

where R_{eq} is the estimated equivalent series resistance in the discharging loop of L, which includes the internal resistances of the dc source, the equivalent series resistance of the dc-link capacitor, and the MOSFETs and the diodes ON resistances.

Notably, R_{eq} can be neglected for large values of L, i.e. when $(X_L = 4\pi f_1 L) >> R_{eq}$. Therefore, a simplified form of (6) can be obtained

$$\Delta I_{L_l} = \frac{M \cdot (1-M) \cdot I_\varphi}{6\pi^3 \cdot f_1^2 \cdot C \cdot L}, \tag{7}$$

Finally, combining the low and the high frequency components for L and C, their values can be calculated from

$$\Delta I_L = \frac{M \cdot V_{in}}{f_s \cdot L} + \frac{2M \cdot (1-M) \cdot I_\varphi}{3\pi^2 \cdot f_1 \cdot C\sqrt{16\pi^2 f_1^2 \cdot L^2 + R_{eq}^2}}, \tag{8}$$

$$\Delta V_{inv} = \frac{(1-M) \cdot I_{in}}{f_s \cdot C} + \frac{2M \cdot I_\varphi}{3\pi^2 \cdot f_1 \cdot C}, \tag{9}$$

where ΔV_{inv} and ΔI_L are the peak-to-peak dc-link voltage and inductor current ripples respectively, including the low and high frequency components, i.e. $\Delta V_{inv} = \Delta V_{inv_l} + \Delta V_{inv_h}$ and $\Delta I_L = \Delta I_{L_l} + \Delta I_{L_h}$.

C. Modulation Using Triangular and Sawtooth Carriers

As mentioned before, the SSI suffers from the high frequency commutation problem of its input diodes. For the single-phase SSI shown in Fig. 1, each of the two input diodes is continuously conducting with different current values for half of the fundamental period, while the other one is continuously commutating during this period. This can be clarified considering one switching cycle as shown in Fig. 4(a), where this figure shows the transitions between three different states during one switching cycle using the triangular carrier.

According to Fig. 4(a) and Fig. 2, D_x is always conducting, while D_y is commutating. Fig. 4(a) shows that D_y turns OFF twice in each switching cycle. The first turning OFF instant in Fig. 4(a) occurs during the charging period with different current values as it depends on the intersection point of the oscillating lower envelope, defined by $(min(v_x^*, v_y^*))$, with the carrier signal. Meanwhile, the second turning OFF instant Fig. 4(a) occurs at the end of the discharging period with a constant current value equal to half of the inductor current minimum value as it depends on the intersection point of the constant upper envelope, defined by $(max(v_x^*, v_y^*))$, with the carrier signal.

These high frequency commutations of the input diodes represent additional losses due to the reverse recovery losses of these diodes. Moreover, the reverse recovery current of these input diodes represents additional conduction losses in the other switches. It is worth to note that this commutating current in the diodes corresponds to the commutating current in the switches. Hence, reducing this current results in lower switching losses.

According to the prior discussions, it is expected that the sawtooth carrier will result in one diode commutation per switching cycle as shown in Fig. 4(b) and Fig. 4(c). These figures show that D_y turns OFF once in each switching cycle. Hence, the sawtooth carriers reduce the number of the input diodes commutations by half. Comparing between Fig. 4(b) and Fig. 4(c) shows that the leading-edge sawtooth carrier results in the lowest possible turning OFF current of the commutating diode (i.e. D_y in this case), as it turns OFF at the end of the discharging period, in which the input current reaches its lowest value. Thus, using the leading-edge sawtooth carrier achieves the diodes commutations at half of the inductor current minimum value (i.e. $0.5min(i_{in})$) and

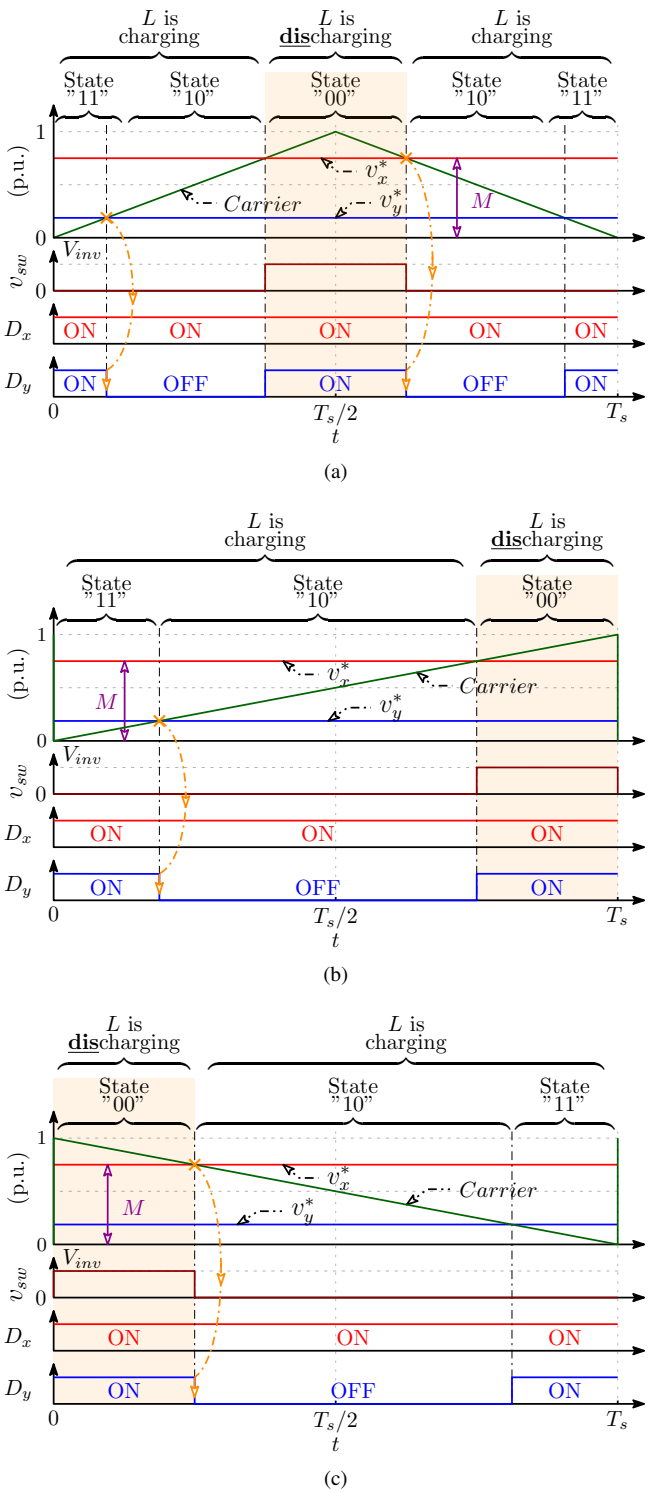


Fig. 4. One switching cycle of the modified sinusoidal pulse width modulation (MSPWM) scheme using different carriers. (a) using the triangular carrier; (b) using the trailing-edge sawtooth carrier; (c) using the leading-edge sawtooth carrier, where $M = 0.75$ and $M_f = 300$.

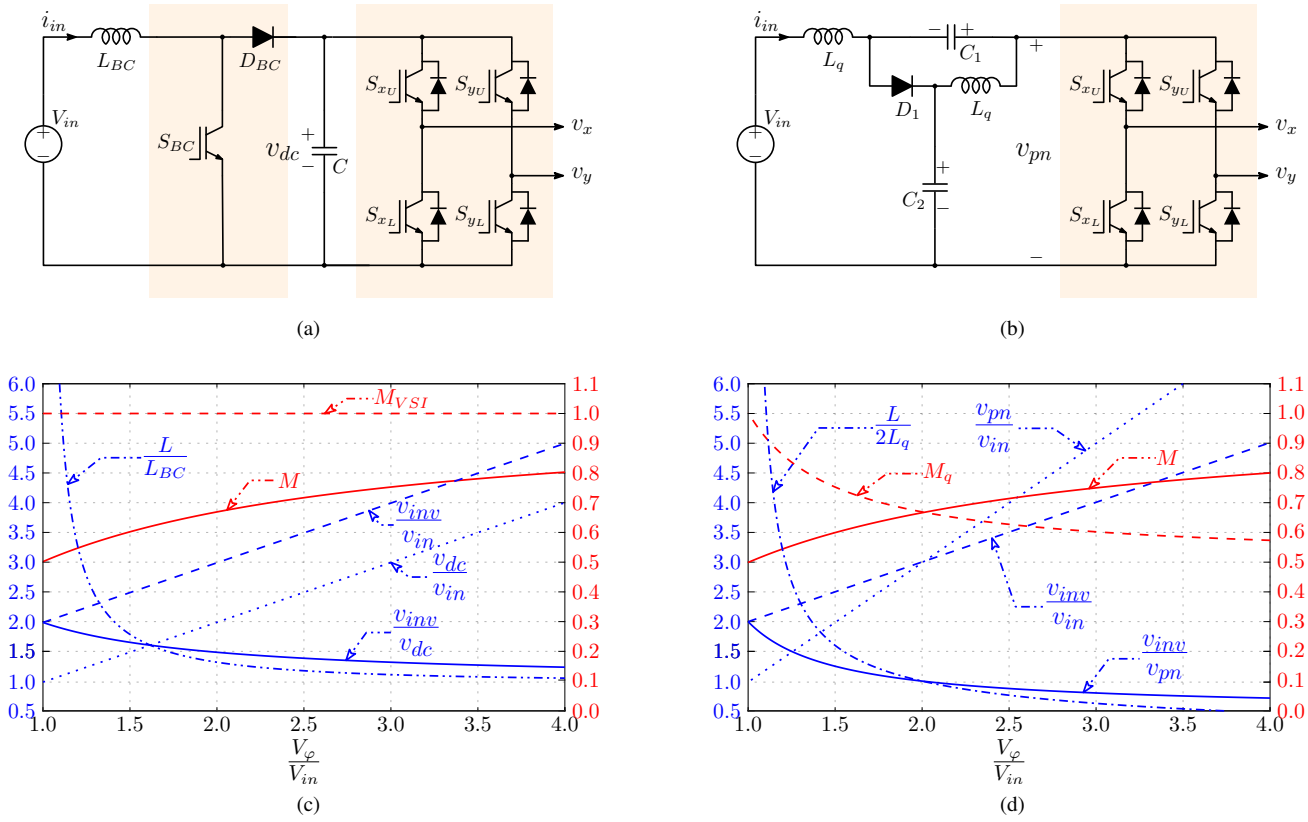


Fig. 5. Topologies used in the comparative study with the single-phase SSI and the resultant comparative graphs. (a) two-stage architecture based on a boost converter-fed single-phase full-bridge VSI; (b) single-stage single-phase qZSI; (c) resultant comparative plot between the single-phase SSI and the two-stage architecture; (d) resultant comparative plot between the single-phase SSI and the single-phase qZSI.

TABLE I
COMPARISON BETWEEN THE SINGLE-PHASE SSI, THE TWO-STAGE ARCHITECTURE, AND THE SINGLE-PHASE Q-ZSI

	Single-phase SSI	Two-stage architecture	Single-phase qZSI
Circuit diagram	Fig. 1	Fig. 5(a)	Fig. 5(b)
Number of active switches	4	5	4
Number of diodes	$2^{(1)}$	1	1
Number of inductors	1	1	2
Number of capacitors	1	1	2
Number of B4-bridge switching states	4	$4^{(2)}$	$5^{(3)}$
THD of the output voltage	Low at high voltage gains	Lowest	Low at low voltage gains
Output filter requirements	Low at high voltage gains	Lowest	Low at low voltage gains
Active switches maximum current	2 X $(I_{in} + 0.5\Delta I_L + I_\varphi)$, 2 X (I_φ)	1 X $(I_{in} + 0.5\Delta I_L)$, 4 X (I_φ)	4 X $(I_{in} + 0.5\Delta I_L + I_\varphi)$
Diode(s) maximum current	$I_{in} + 0.5\Delta I_L$		$2I_{in} + \Delta I_L$

(1) Single-device comprises two common-cathode diodes.
(2) The boosting is achieved using the BC (i.e. additional control signal is sent to the BC).
(3) An additional switching state is used in order to achieve the boosting capability.

reduces the input diodes commutations by half if the same switching frequency is used. Furthermore, using the leading-edge sawtooth carrier in a discontinuous conduction mode (DCM) of the inductor current results in zero commutating current of these input diodes as the minimum value of the inductor current in this case equal to zero.

Hence, the following features exist as a consequence of using the sawtooth carrier instead of the triangular carrier:

- reduced number of commutations of the input diodes by half;
- lowest possible commutation current of the input diodes using the leading-edge sawtooth carrier;
- higher output filter requirements as the differential output voltage is not the same.

For the last feature, the switching frequency of the sawtooth carriers should be doubled in order to maintain similar differ-

ential output voltage and use similar output filter. Finally, the use of the leading-edge sawtooth carrier is expected to result in a slight increase in the efficiency due to the diodes commutation at the lowest possible commutation current, while the reduction of the commutations by half has a negligible effect.

III. Comparative Study

It is of paramount importance to compare the performance of the single-phase SSI with respect to the standard two-stage architecture shown in Fig. 5(a) and the single-phase single-stage qZSI shown in Fig. 5(b), where the latter is considered as the commonly used single-stage solution. Hence, this section introduces this comparative study. Note that the two-stage architecture shown in Fig. 5(a) has two control parameters: the boost converter duty cycle (D_{BC}) and the VSI modulation index (M_{VSI}). Meanwhile, the single-phase qZSI shown in Fig. 5(b) has a single control parameter, which is the modulation index (M_q). Those two configurations are considered to evaluate the performance of the single-phase SSI in terms of number of required active switches, inductors, capacitors, and diodes. Moreover, the variation of several parameters for these three topologies versus V_φ/V_{in} variation are considered as well. These parameters include the inductance requirements, modulation index variation that gives an indication of the total harmonic distortion (THD) of the output voltage, and voltage stresses across the different switches.

The two-stage architecture shown in Fig. 5(a) comprises a BC to boost the low input voltage in order to meet the load requirements, then an inversion stage is utilized, which is implemented using a single-phase full-bridge VSI. This two-stage architecture requires one inductor L_{BC}, one capacitor, one active switch, one diode, and the B4-bridge to achieve the boosting and the inversion operation for a unidirectional power conversion operation. On the other hand, the single-phase qZSI shown in Fig. 5(b) achieves the same operation without any additional active switches, as it uses only the standard B4-bridge and one diode, in addition to two inductors and two capacitors. Table I summarizes this numerical comparison and shows the maximum current in the different switches.

Fig. 5(c) and Fig. 5(d) show the obtained results when comparing the proposed single-phase SSI with the two-stage architecture and the single-phase qZSI respectively. These figures show the variation of several parameters versus the variation of V_φ/V_{in}, where, for each topology, the modulation index, the maximum voltage across the bridge, the input inductance requirements are considered.

Note that in Fig. 5(c), M_{VSI} is fixed to 1 and D_{BC} is used to control the output voltage, which results in the lowest possible THD of the output voltage, leading to reduced output filter requirements. The single-phase SSI achieves low voltage stresses, input inductance requirements, and THD of the output voltage with the increase of V_φ/V_{in} (i.e. for low input voltages), but these parameters are still relatively higher than the two-stage architecture. On the other hand, Fig. 5(d) shows that the the single-phase SSI achieves lower voltage stresses, input inductance requirements, and THD of the output voltage compared to the single-phase qZSI for $V_\varphi/V_{in} > 2$. Note that the qZSI in Fig. 5(d) uses two shoot-through states per switching cycle, which increases the switching losses but decreases its inductance requirements, i.e. if one shoot-through pulse is used per switching cycle, its inductance requirements will be doubled. Furthermore, the inductance requirements are based on the high frequency component only, assuming that the closed-loop control is utilized to mitigate the effect of the low frequency one.

It is worth to note that the SSI is still expected to have a good performance compared to the qZSI when $V_\varphi/V_{in} < 2$ due to the following reasons. Firstly, unlike qZSI, the dc-link voltage in SSI topology is continuous. The generated discontinuous dc-link voltage in the qZSI prevents the use of high frequency decoupling capacitors across each phase-leg in order to limit the voltage spikes across the different switches due to the layout parasitic inductance. Furthermore, it might be mandatory to use snubber circuits to protect these switches. The second reason is the added shoot-through state, which represents extra switching losses.

IV. Simulation Results

In this section, a 1-kVA single-phase SSI is designed and simulated in order to verify the analysis and discussions. This single-phase SSI is designed to be fed from an input dc source, whose voltage ranges from $80\ V$ to $120\ V$, while the output RMS voltage is maintained constant at $110\ V$. Moreover, the fundamental and the switching frequencies have been set to $50\ Hz$ and $50\ kHz$ respectively. Table II summarizes the parameters of this 1-kVA single-phase SSI. Note that L has been designed using (8) so that $\Delta I_L \approx 137\%$ of I_{in} as a maximum value at full load when $V_{in} = 120\ V$, which corresponds to $\Delta I_{L_h} \approx 55\%$ of I_{in}. Meanwhile, C has been designed using (9) so that $\Delta V_{inv} \approx 2.5\%$ of V_{inv} as a maximum value at full load when $V_{in} = 80\ V$. R_{eq} is assumed to be $300\ m\Omega$ to match the employed components in the experimental validation. Table II shows the peak-to-peak inductor current and dc-link voltage ripples at different input voltages, corresponding to the selected L and C values.

The 1-kVA single-phase SSI has been simulated using a MATLAB/PLECS model, where the used parameters in the model are taken from the specifications listed in Table II, and an output LC filter of $1\ mH$ and $10\ \mu F$ has been used. This inverter is feeding a resistive load (R_{load}) of $12.5\ \Omega$ and its modulation-to-fundamental frequency ratio M_f equals to 1000. The obtained simulation results for input voltage of $80\ V$ and $120\ V$ are depicted in Fig. 6, and the output voltage v_{xy}, the load voltage (v_{load}), the load current (i_{load}), the dc-link voltage (v_{inv}), the inductor current (i_{in}), and the diode D_x current (i_{D_x}) are shown using the leading-edge sawtooth carrier. Note that in Fig. 6, V_{inv} is lower than its equivalent theoretical value shown in Table II and this deviation is higher for $V_{in} = 80\ V$ due to the higher voltage drop in the converter resistances, which is estimated from the experimental components.

Fig. 7 shows the spectrum of the output voltage (v_{xy}) for the single-phase SSI using the triangular and sawtooth carriers, considering two input voltages, i.e. two voltage gains. These

TABLE II
SPECIFICATIONS AND DESIGNED PARAMETERS OF A 1-kVA SINGLE-PHASE SSI

V_{in} (V)	I_{in} (A)	$V_{\varphi_{RMS}}$ (V)	$I_{\varphi_{RMS}}$ (A)	f_1 (Hz)	f_s (kHz)	M Eq.	M (p.u.)	V_{inv} Eq.	V_{inv} (V)	Required L Eq.	Required L (mH)	Required C Eq.	Required C (mF)	ΔI_L (A)	ΔV_{inv} (V)
80	12.5	110	11	50	50	(2)	0.6604	(1)	235.6	(8)	0.3	(9)	2	9.3	6
120	8.3						0.5649		275.8					11.4	5.6

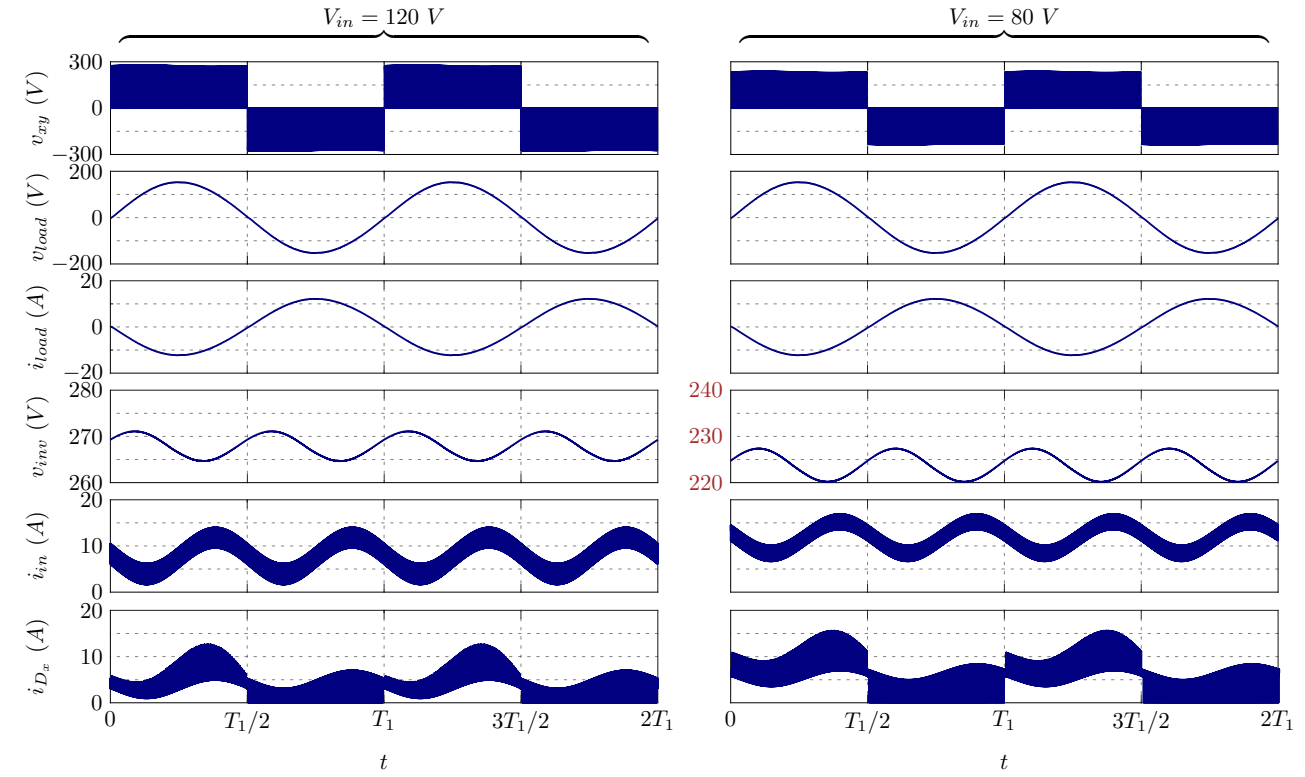


Fig. 6. Simulation results of the 1-kVA single-phase SSI using leading-edge sawtooth carrier for two fundamental cycles, considering $V_{in} = 120\ V$ and $80\ V$. From top to bottom: output voltage (v_{xy}), load voltage (v_{load}), load current (i_{load}), dc-link voltage (v_{inv}), inductor current (i_{in}), and diode D_x current (i_{D_x}).

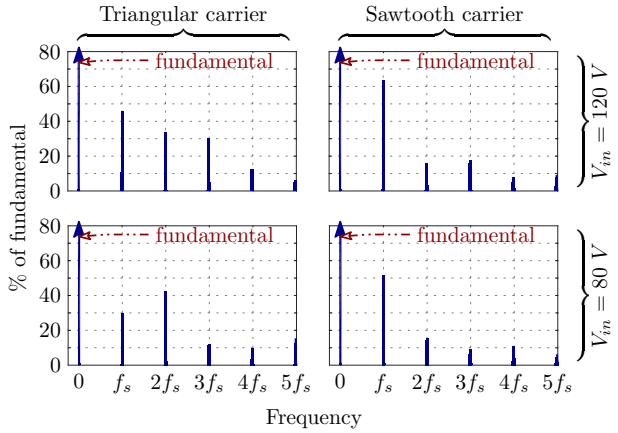


Fig. 7. Simulated output voltage (v_{xy}) spectrum of the 1-kVA single-phase SSI using the triangular and the leading edge sawtooth carriers, considering two different input voltages: $80\ V$ and $120\ V$.

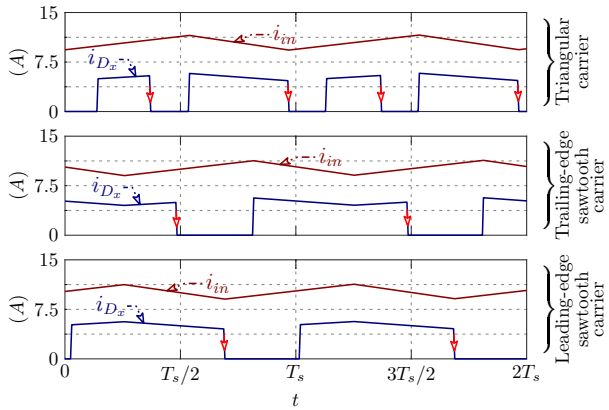
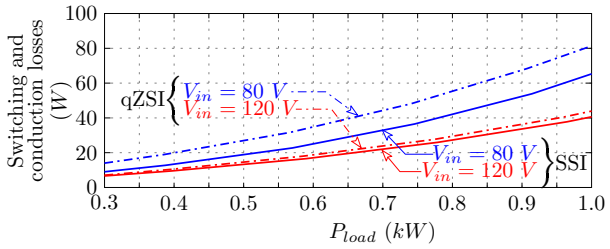
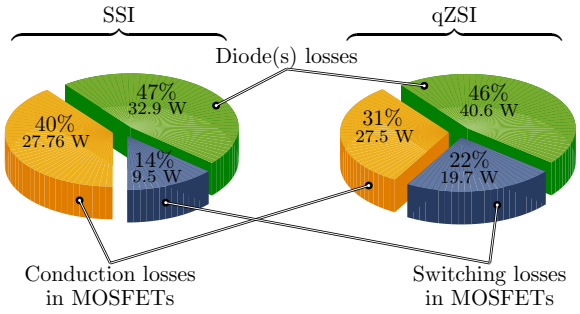


Fig. 8. Simulated currents in D_x (i_{D_x}) and L (i_{in}) when $V_{in} = 120\ V$ using different carriers for two switching cycles, showing the commutation instants of D_x.

spectrums show that using the sawtooth carrier at any voltage gain, the energy is high at f_s. On the other hand, using the triangular carrier with higher voltage gains, i.e. higher values of M, the energy is getting to be higher at $2f_s$. It is worth to note that these spectrums are different from the conventional VSI spectrums due to the employed biasing in the modulating signals shown in Fig. 3(b), in which the minimum vale of the



(a)



(b)

Fig. 9. Simulated switching and conduction losses of the SSI and the qZSI using PLECS, where the qZSI is utilizing two shoot-through pulses per switching cycle. (a) losses variation with the load power considering two different input voltages: $80\ V$ and $120\ V$; (b) losses distribution among the different switches at full-load when the input voltage is equal to $80\ V$.

reference signals are always fixed to zero.

Fig. 8 shows the simulated currents in D_x (i_{D_x}) and L (i_{in}) using different carriers for two switching cycles. This figure elucidates and confirms the previous discussions, where the sawtooth carriers introduce one commutation of the diode per switching cycle, unlike the triangular one that introduces two commutations per switching cycle. Moreover, the leading-edge sawtooth carrier introduces this commutation at the end of the discharging period, in which the diode commutates always at half of the minimum inductor current (i.e. the lowest possible current value for commutation).

The switching and conduction losses of the single-phase SSI have been evaluated using PLECS and Fig. 9(a) shows the total losses variation versus the load power using the leading-edge sawtooth carrier, where the used devices are C2M0040120D and C2D10120D, and the losses are shown for $V_{in} = 80\ V$ and $120\ V$. Moreover, Fig. 9(b) shows the distribution of these losses among the different switches at full-load, in which the losses in the input diodes represents almost half of the total losses. Thus, if these diodes are replaced by MOSFETs as discussed in [13], the efficiency will increase. In addition to that, the switching and conduction losses of the single-phase qZSI have been evaluated as well utilizing the same devices and two shoot-through pulses per switching cycle, and the total losses variation versus the load power is shown in Fig. 9(a), while the distribution of these losses among the different switches at full-load is shown in Fig. 9(b). These figures shows that the qZSI has higher losses compared to the SSI with the increase of the overall gain. Furthermore, it shows that the switching losses in the qZSI is higher due to the added shoot-through state, which is employed twice per switching cycle. Meanwhile, if this state is employed once per switching cycle, the required inductance will be higher. On the other hand, the qZSI diode has higher losses due to the higher current stresses in it. Note that, the used values of the qZSI impedance network in the PLECS model are as follows: $L_q = 150\ \mu H$ and $C_1 = C_2 = 4\ mF$. Moreover, the qZSI PLECS model uses the two diodes in C2D10120D and connect them in parallel to meet the higher current stresses.

TABLE III
PARAMETERS AND SPECIFICATIONS OF THE EXPERIMENTAL 1-kVA SINGLE-PHASE SSI

V_{in}	80:120 (V)	$V_{\varphi_{RMS}}$	110 (V)
f_1	50 (Hz)	f_s	50 (kHz)
L	0.3 (mH)	C	2 (mF)
L_f	1 (mH)	C_f	9.4 (μF)
$S_{x,y}$	C2M0040120D	$D_{x,y}$	C2D10120D
Core of L	Powder core 77617A7	Core of L_f	Powder core 77442A7

V. EXPERIMENTAL RESULTS

In this section, the prior designed 1-kVA single-phase SSI is implemented experimentally in order to verify the simulation results and evaluate its efficiency. This 1-kVA single-phase SSI prototype is shown in Fig. 10 and its parameters are shown in Table III, which have been taken from the simulated one. The used switches in this prototype are: four Cree C2M0040120D MOSFETs and one Cree C2D10120D common-cathode diode.

Fig. 11 shows the obtained experimental results of the single-phase SSI at full-load using the leading-edge sawtooth carrier, in which the input voltage (V_{in}) has been set to $120\ V$ in Fig. 11(a) and $80\ V$ in Fig. 11(b). In this figure, the dc-link voltage (v_{inv}), the load voltage (v_{load}), the load current (i_{load}), and the inductor current (i_{in}) are shown. This figure verify the prior obtained simulation results and verify the reported analysis.

Note that the reactive power capability of the single-phase SSI is the same as the two-stage architecture as the principle of operation of both is similar. In order to verify this issue, Fig. 12 shows the same measurements shown before when $V_{in} = 80\ V$ considering a highly inductive load, whose power factor is equal to 0.5. In Fig. 12, the load current is limited in order not to exceed the rated current of the employed inductive load.

This prototype has been tested to figure out the maximum possible gain that can be achieved. Fig. 13 shows the voltage gain variation versus the modulation index, which is calculated theoretically using (1) and validated experimentally for five points. This figure confirms the prior discussions that the SSI, like the two-stage architecture, can experimentally achieve a maximum voltage gain from 4 to 5.

The efficiency of the single-phase SSI prototype is measured using the leading-edge sawtooth carrier for different input voltages, and the obtained results are introduced in Fig. 14,

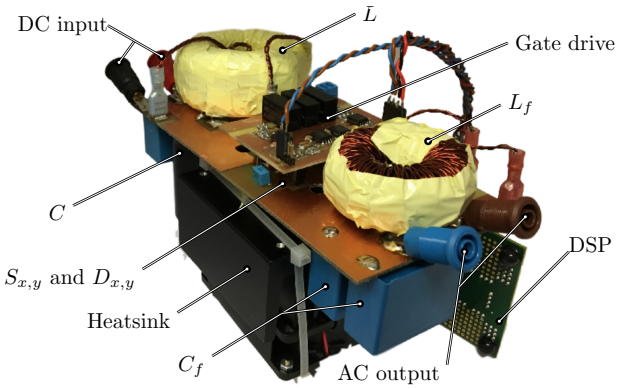


Fig. 10. Experimental prototype of a $1\text{-}kVA$ single-phase SSI.

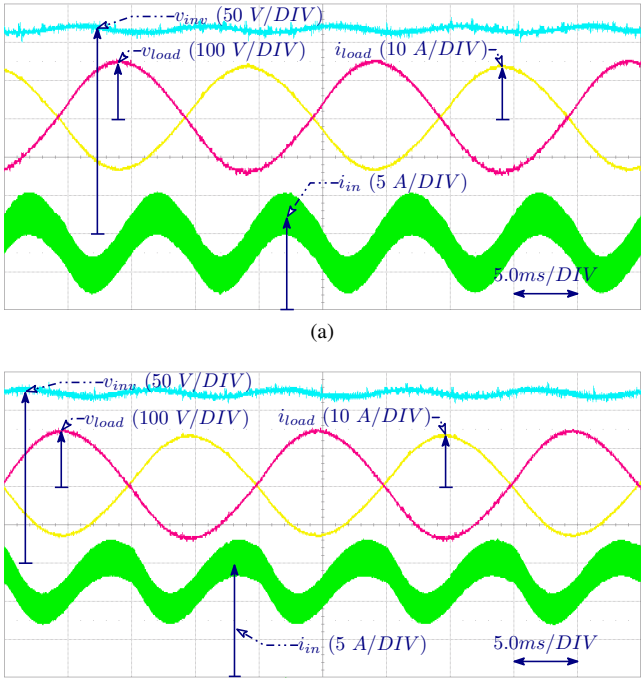


Fig. 11. Experimental results of the $1\text{-}kVA$ single-phase SSI at full-load, considering two different input voltages (V_{in}), where the load voltage (v_{load}), the load current (i_{load}), the dc-link voltage (V_{inv}), and the input current (i_{in}) using the leading edge sawtooth carrier are shown in each result. (a) $V_{in} = 120\ V$; (b) $V_{in} = 80\ V$.

where these efficiency measurements include the output filter losses. These measurements have been achieved using KinetiQ PPA5530 power analyzer. This figure shows that a maximum efficiency of 95.5% has been achieved. Moreover, it confirms the prior obtained results from PLECS. In this figure, four different input voltages have been considered, where three of them are in the designed operating range of the prototype and an extra one, which is the $60\ V$ is out of the designed range. The latter point has been selected as a higher gain point and it has been tested up to the current limits of the prototype. This figure confirms that the SSI has lower efficiency at higher voltage gains due to the higher conduction losses.

Finally, Fig. 15 shows the measured efficiency using the prior introduced carrier signals, where $V_{in} = 100\ V$, which

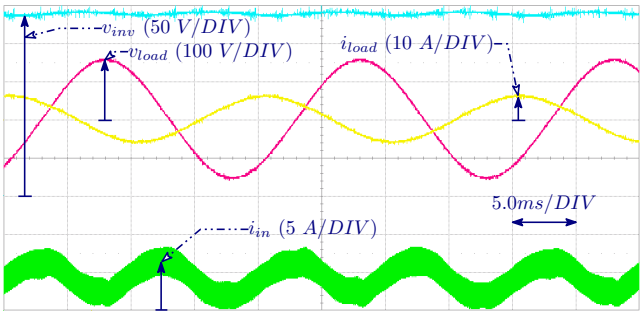


Fig. 12. Experimental results of the $1\text{-}kVA$ single-phase SSI when $V_{in} = 80\ V$ considering an inductive load, whose power factor is equal to 0.5, where the load resistance is equal to $10\ \Omega$. The load voltage (v_{load}), the load current (i_{load}), the dc-link voltage (V_{inv}), and the input current (i_{in}) using the leading edge sawtooth carrier are shown.

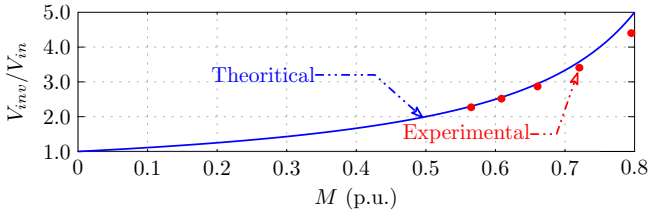


Fig. 13. Theoretical voltage gain using (1) and experimental voltage gain using the $1\text{-}kVA$ single-phase SSI prototype variation versus the modulation index.

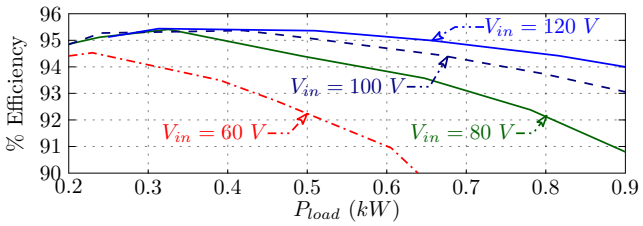


Fig. 14. Measured experimental efficiency of the $1\text{-}kVA$ single-phase SSI using the leading-edge sawtooth carrier for different input voltages.

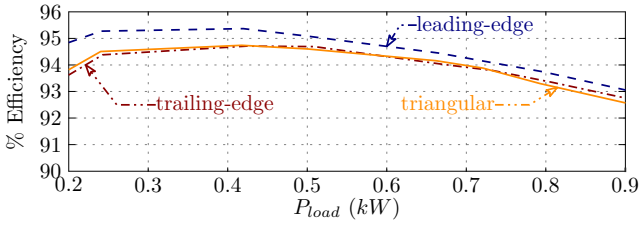


Fig. 15. Measured experimental efficiency of the $1\text{-}kVA$ single-phase SSI using the leading-edge sawtooth, the trailing-edge sawtooth, and the triangular carriers when $V_{in} = 100\ V$.

confirms that the leading-edge sawtooth carrier achieves the highest efficiency due to the diode commutation at the lowest possible currents. Meanwhile, the others achieve similar efficiency as both makes the diodes commutations at different current values. Note that the diodes commutations are associated with the switches commutations.

VI. Conclusion

The single-phase operation of the split-source inverters (SSIs), considering the unidirectional dc-ac operation, has

been studied in this paper and an alternative configuration has been utilized, in which it is possible to use a common-cathode dual-diode package instead of two separate diodes to minimize the parasitic inductance in the commutation path of these diodes. Moreover, the high frequency commutation problem of these input diodes has been investigated and different carriers have been studied. Among the triangular, the trailing-edge sawtooth, and the leading-edge sawtooth carriers, the latter achieves one commutation of the input diodes at the lowest possible current value, which equals half of the minimum input current. Meanwhile, to maintain similar differential output voltage and use similar output filter, the switching frequency of the sawtooth carriers should be doubled, resulting in having the same number of high frequency commutations of the input diodes as the triangular one, increased number of bridge commutations, and reduced input inductance. Furthermore, using the leading-edge sawtooth carrier, it is possible to obtain zero commutating current of these input diodes in the discontinuous conduction mode (DCM) of the inductor current.

The performance of the single-phase SSI has been evaluated by comparing it to the standard two-stage architecture and the single-phase quasi-Z-source inverter (qZSI). This is followed in order to figure out the single-phase SSI features in the different operating points. This topology has been analyzed using MATLAB/PLECS models, considering a $1\text{-}kVA$ system, and its switching and conduction losses have been evaluated using PLECS.

Finally, the designed $1\text{-}kVA$ single-phase SSI has been implemented experimentally to verify the reported analysis, and a maximum experimental efficiency of 95.5% has been obtained.

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