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Power Cycling Test Methods for Reliability Assessment of Power Device Modules in Respect to Temperature Stress

Ui-Min Choi, *Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*, and Søren Jørgensen

***Abstract*—Power cycling test is one of the important tasks to investigate the reliability performance of power device modules in respect to temperature stress. From this, it is able to predict the lifetime of a component in power converters. In this paper, representative power cycling test circuits, measurement circuits of wear-out failure indicators as well as measurement strategies for different power cycling test circuits are discussed in order to provide the current state of knowledge of this topic by organizing and evaluating current literature. In the first section of this paper, the structure of a conventional power device module and its related wear-out failure mechanisms with degradation indicators are discussed. Then, representative power cycling test circuits are introduced. Furthermore, on-state collector–emitter voltage ($V_{\mathrm{CE\_ON}}$) and forward voltage (V_F) measurement circuits for wear-out condition monitoring of power device modules during power cycling test are presented. Finally, different junction temperature measurement strategies for monitoring of solder joint degradation are explained.**

***Index Terms*—Failure mechanism, insulated gate bipolar transistor (IGBT), power cycling (PC) test, power device module, reliability, wear-out failure.**

I. Introduction

POWER electronic systems (PESs) play an important role in many applications for efficient power generation, distribution, and consumption and also for energy control in order to achieve high system performance efficiently [1]–[3]. On the other hand, power electronic subsystems are one of major failure sources in last generation products [3]. Examples of field experiences in photovoltaic and wind power systems show that power electronic converters are one of the most critical parts in terms of failure rate, lifetime, and maintenance cost [4]–[7].

As PESs have gradually gained an important status in the power infrastructure, the reliability of PESs is becoming a serious issue [3], [4]. Therefore, recent research endeavors to improve the reliability of PESs to comply with more stringent constraints on cost, safety, and availability in various applications. Especially, the reliability assessment and lifetime prediction of reliability critical components such as power device modules and capacitors in PESs are the major concern [8]–[14].

The power cycling (PC) test is an important and efficient method to assess the reliability performance of power device modules related to packaging technology, in respect to temperature stress [15]–[17]. From the PC test, failure mechanisms of the power device modules due to temperature stress can be studied [18]–[20]. Furthermore, new device packaging materials and designs can be evaluated [17], [21]–[23]. Finally, last but not least, a lifetime model in respect to the temperature stress can be developed based on the PC test results [24]–[26], [91] and it can be used for design for reliability by estimating the lifetime of power device modules under given mission profiles of real converter applications [11], [13], [27]–[30].

In recent PC test, some advanced features are demanded such as realistic operation of a device under test (DUT) during the PC test and online monitoring of wear-out status of the DUT. In order to meet these needs, several advanced test circuits and monitoring circuits of the DUT have been proposed and they will be discussed in this paper. Online monitoring of the failure indicators of the DUT such as on-state collector emitter voltage ($V_{\mathrm{CE\_ON}}$) and junction temperature (T_j) gives benefits when PC test is performed. First of all, PC test does not need to be stopped in order to measure the failure indicators. This process is very inconvenient and time consuming. Furthermore, the PC test can be finished properly before the catastrophic failure occurs, which enables to do physical failure analysis of the DUT. Finally, it helps to better understand wear-out characteristics and also define wear-out failure mechanisms before the analysis of the DUT.

Most of the existing papers are focusing on the test results and there is a lack of detailed information on PC test methods even though they are performed in different ways and PC test methods may be able to affect test results.

In [31], different PC test methods have been introduced. However, this paper is more focusing on the introduction of schematics of PC test circuits and test results. There is no information about the operating principle of PC test circuits, monitoring methods for failure indicators, test procedures, etc.

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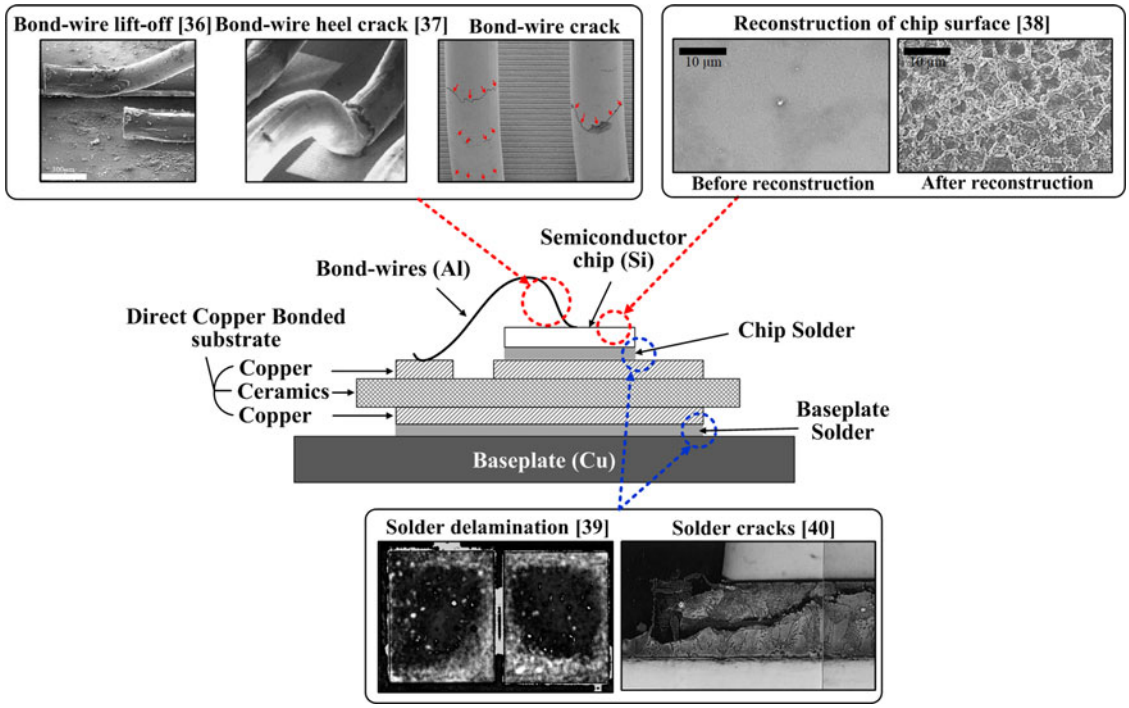

Fig. 1. Structure of a standard IGBT module and dominant package-related failure mechanisms.

Therefore, overviews about PC test, that are more concentrated not only on test circuits but also on the monitoring circuits and measurement strategies for failure indicators, are still needed in order to provide the current state of knowledge of this topic by organizing and evaluating the current literature.

In this paper, representative PC test circuits, measurement circuits for wear-out failure indicators, and measurement strategies for different PC test circuits are discussed and evaluated. In the first section of this paper, the structure of a conventional power device module and the related wear-out failure mechanisms with degradation indicators are discussed. Then, the PC test circuits are presented by dividing into DC and AC PC test circuits.

Furthermore, on-state collector–emitter voltage ($V_{\mathrm{CE\_ON}}$) and forward voltage (V_F) measurement circuits for wear-out condition monitoring of DUT are presented. Finally, different junction temperature measurement strategies for solder joint degradation monitoring are explained.

II. Power Device Module

In practical applications, power devices are used in a form of package such as discrete devices and modules in order to provide electrical connection between one or more semiconductor chips and circuits and also in order to reduce costs in high power applications by connecting several chips with internal insulation of the individual components. Furthermore, the power device module can dissipate the heat generated during chip operation to cooling systems with electrical insulation and can also protect the semiconductor chip from harmful ambient influences [32].

Typically, there are two types of power device modules depending on their packaging technologies: press-pack and wire-bonded power device modules. The press-pack technology improves the connection of chips by the direct press-pack contacting. Therefore, it has an improved reliability, higher power density, and better cooling capability. However, the cost for this technology is higher compared with the conventional wire-bonded power device modules. Therefore, the wire-bonded power device modules are still the most widely used in PESs [33], [34]. In this paper, all explanations are based on the wire-bonded insulated gate bipolar transistor (IGBT) module, which is the most widely used of their kind [8].

A. Structure of Standard Power Device Modules

Fig. 1 shows the structure of a standard IGBT module [15], [32]. A direct copper bonded (DCB) substrate is soldered to a base-plate. The DCB provides electrical insulation between power components and cooling systems. Furthermore, it conducts a current via copper tracks and provides also good thermal connection to the cooling systems. In the lower power range, the power device modules without the base-plate are more frequently used, while in medium and high power ranges, power device modules have almost all the base-plate. The base-plate provides thermal capacity and helps for the thermal spreading by increasing the contact area to a heat-sink. Power devices such as IGBTs and diodes are soldered to the DCB. Bond wires are commonly used in order to connect the emitter of the silicon chips to the substrate and in order to connect the substrate to the terminals. Finally, it is covered by a silicone gel or epoxy resin for insulation [35].

B. Failure Mechanisms and Damage Indicators

Failure mechanisms of the power device module are generally divided into two categories: device-related failure mechanism

TABLE I
COEFFICIENT OF THERMAL EXPANSION (CTE) OF DIFFERENT MATERIALS IN IGBT MODULE [15], [37]

Material	Properties	CTE (10^{-6} K^{-1})
$A1_2O_3$	Ceramic	6.8
AlN	Ceramic	4.7
Al	Metal	23.5
Cu	Metal	17.5
Si	Semiconductor	2.6
Solder (SnAg(96.5/3.5))	Alloy	28

and packaging-related failure mechanisms [37]. Most of the failures related to devices are due to over-stress conditions and therefore they are out of the scope of this paper, which is about the PC tests for the wear-out failure.

The packaging-related failure mechanisms occur mainly due to the thermo-mechanical stress experienced by various materials in the power device module. As shown in Fig. 1, the power device module consists of various materials and they have different Coefficient of Thermal Expansions (CTEs) as listed in Table I. The CTE mismatch under the temperature variation applies thermo mechanical stress to the packaging materials and finally leads to wear-out failures [37]. One of the largest CTE mismatches is between the power device chip (silicon), and bond-wires (aluminum), chip surface metallization (aluminum).

The repeated temperature variation in the power device module due to the periodical commutation of power switching device, converter load variation, and ambient temperature change leads to wear-out failure of bond-wires such as bond-wire lift-off and bond-wire crack or reconstruction of aluminum surface metallization [15], [36]–[38], [41], [42]. The failure of a single or small number of bond-wires alters the current distribution in power devices and accelerates the wear-out failure of the remaining bond-wires. Finally, it leads to open-circuit failure or catastrophic failures of power devices such as thermal runaway and chip destruction.

The reconstruction of aluminum surface metallization leads to the increase of the metal sheet resistance due to rough metallization surface, nonuniform current distribution, and weakness of the connection between metallization layer and bond-wire [43].

The bond-wire fatigue and reconstruction of the aluminum surface metallization increase the ohmic resistance $(R_{\rm int})$ and it appears as an increase in the on-state collector–emitter voltage $(V_{\rm CE\_ON})$ of transistors or forward voltage (V_F) of diodes because the measured $V_{\rm CE\_ON}$ or V_F can be given as [44]

$$V_{\rm CE\_ON} = V_{\rm CE\_Chip} + R_{\rm int} \cdot I_C. \quad (1)$$

where $V_{\rm CE\_Chip}$ is the real on-state collector–emitter voltage of the chip, $R_{\rm int}$ is the equivalent resistance of the interconnections elements, and I_C is the collector current. Typically, in the case of reconstruction of aluminum surface metallization, the steady increase of $V_{\rm CE\_ON}$ is observed. On the other hand, the sharp step increase of $V_{\rm CE\_ON}$ can be seen by bond-wire fatigue. Therefore, bond-wire fatigue can be monitored by measuring

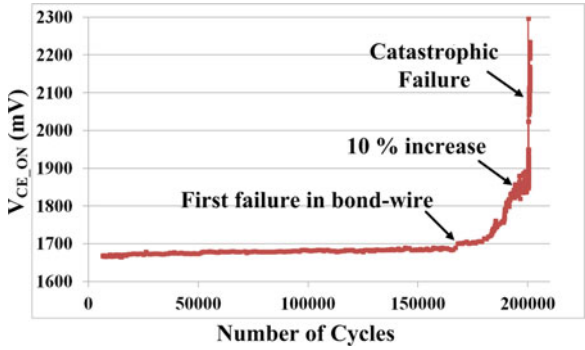

Fig. 2. Variation of $V_{\rm CE\_ON}$ due to bond-wire crack under the power cycling test [56].

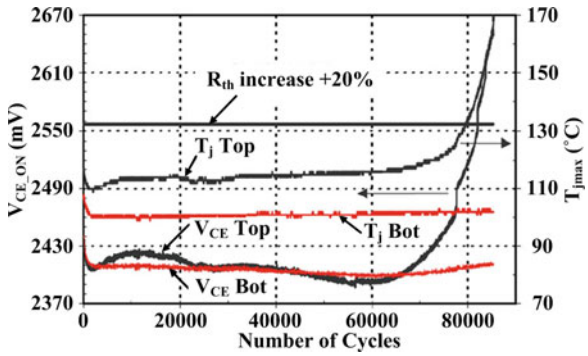

Fig. 3. Variation of $T_{j\max}$ due to solder joint fatigue [15].

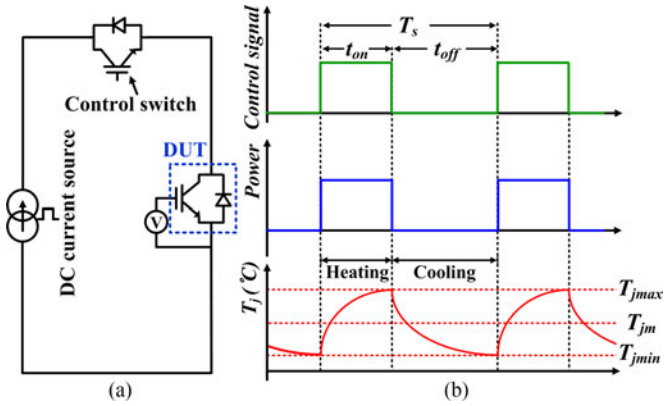

Fig. 4. Conventional DC power cycling test (a) configuration of DC power cycling test (b) control signal of control switch, injected power, and temperature profile applied to device under test.

$V_{\rm CE\_ON}$ and V_F. Generally, 5–20% increase of $V_{\rm CE\_ON}$ and V_F is the end-of-life criterion [15].

Fig. 2 shows the change of $V_{\rm CE\_ON}$ of IGBTs due to bond-wire cracks.

The other dominant failure mechanism is solder joint fatigue. There are two solder joints in the standard IGBT module between chip and DCB substrate and between DCB substrate and base-plate. Due to the CTE mismatch with temperature variation, the thermo-mechanical stresses are applied to the solder joints and cause the degradation of the solder interface such as cracks and delamination. The solder joint fatigue increases the

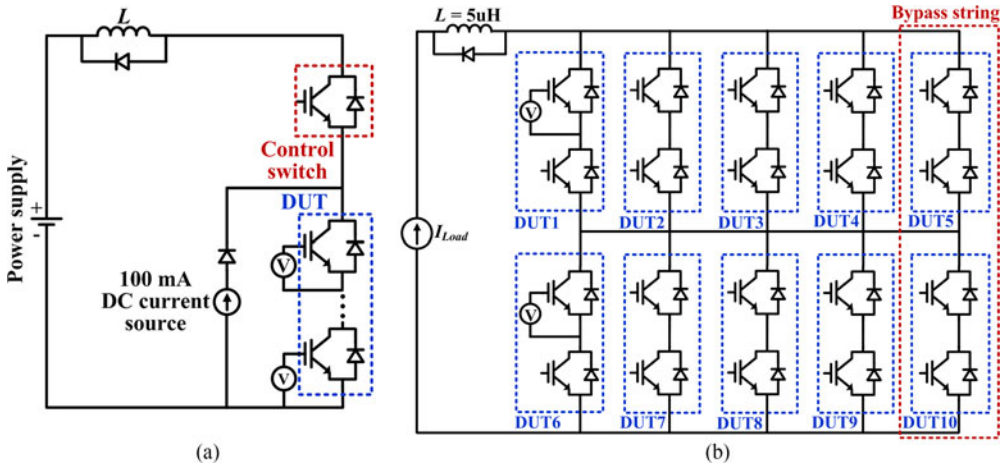

Fig. 5. Extended configurations of DC power cycling test (a) in [50] (b) in [51].

thermal impedance of IGBT modules. Consequently, the junction temperature of power semiconductor devices may increase and it could accelerate other failure modes such as bond-wire fatigue [37], [45]. Furthermore, the junction temperature increase could induce hot spots and thermal runaway in the affected areas of the power devices [46]. The thermal impedance $R_{\mathrm{th}(j-c)}$ is typically used as a failure indicator for solder joint fatigue. $R_{\mathrm{th}(j-c)}$ can be obtained from junction temperature and case (or heat-sink) temperature as

$$R_{\mathrm{th}(j-c)} = \frac{T_j - T_c}{P_{\mathrm{loss}}}. \tag{2}$$

where $R_{\mathrm{th}(j-c)}$ is the junction to case thermal impedance, T_j is the junction temperature, T_c is the case temperature, and P_{loss} is the power loss. Therefore, the thermal impedance change due to solder joint fatigue can be monitored by measuring the junction temperature during PC test. Typically, 20% increase of thermal impedance is the end-of-life criterion.

Fig. 3 shows the junction temperature variation of an IGBT due to solder joint fatigue.

III. Configuration of Power Cycling Test Circuits

A. DC Power Cycling Test Circuits

1) Conventional DC Power Cycling Test Circuit [15], [18], [47]–[51]: Most PC tests have been performed with DC PC test setups due to their simplicity.

Fig. 4(a) shows the basic configuration of DC PC test circuit for explaining the operating principle. In this test system, the DUT is always turned on by applying constant DC voltage (typically 15 V) to the gate of DUT and an injection of load pulse with constant DC current is controlled by turning on and off the control switch. If the load pulse is applied to the DUT by turning on the control switch, the junction temperature of DUT starts to increase by the conduction loss. If the junction temperature is reached to the desired condition, the applied power is disconnected by turning off the control switch and the junction temperature of DUT is decreased by the external cooling system. This period (T_s) is defined as cycle as shown in Fig. 4(b) and it is repeated until the DUT fails. The duration and amplitude of the current pulse are varied in order to obtain the desired temperature stress conditions such as junction temperature swing $\triangle T_j$ $(T_{j\max} - T_{j\min})$, mean junction temperature T_{jm}, and load pulse duration time t_{on}.

Fig. 5 shows some extended configurations of the DC PC test circuit. In the test circuit shown in Fig. 5(a), 100 mA is continuously applied to DUT for junction temperature estimation by measuring the on-state collector emitter voltage $(V_{\mathrm{CE\_ON}})$ when the load pulse is disconnected. Different junction temperature estimation strategies for the PC tests will be considered later in Section V.

One of the main advantages of this test setup is that it is possible to perform the PC tests of many power device modules simultaneously as shown in Fig. 5(b). However, in such test, the tested module is not operated under realistic electrical conditions. There are no switching of the DUT, dynamic loss, and no high DC-link voltage. Furthermore, a high current may be required in order to apply high $\triangle T_j$ in a short cycle period because the temperature is increased by only conduction loss, which might overload the bond-wires and could affect test results. Otherwise, long cycle period (T_s), which leads to long PC test time may be needed if the high current is not injected. Nevertheless, this method is still the most widely used due to the simplicity of the structure and convenience for the monitoring of failure indicators.

2) DC Power Cycling Test Circuit With Saturation Mode of DUT: In order to complement the disadvantages of the conventional DC PC test setup, a DC PC test circuit with saturation mode of the DUT is proposed. Similar approach is used for an analysis of a thermal impedance of power MOSFETs [52], [53] and also for active loads [54], [55]. This principle can be applied for the DC PC test circuit to achieve wanted power losses in the DUT effectively.

Fig. 6 shows the configuration of DC PC test circuit with the saturation mode of the DUT. In this system, the DUT is operated in saturation mode and thus it acts like constant current source. The desired collector current (I_C) can be produced by adjusting the gate–emitter voltage (V_{GS}) with required minimum collector

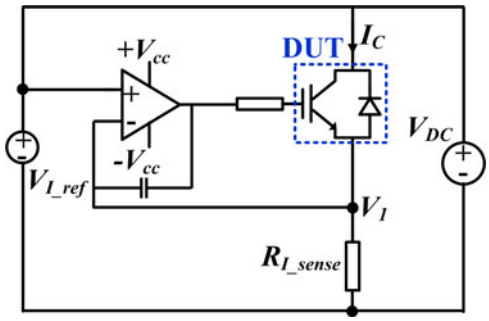

Fig. 6. DC power cycling test circuit with saturation mode of DUT.

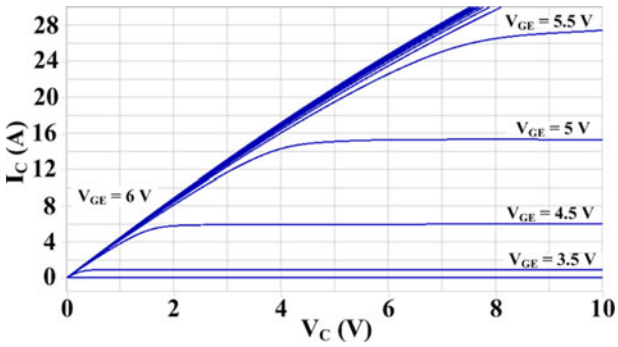

Fig. 7. *I–V* characteristic of DUT under different V_{GE}.

voltage (V_C). If V_C is above the required minimum value under the given V_{GS}, I_C is not affected by the V_C value.

Fig. 7 shows the *I–V* characteristics of the DUT under different gate–emitter voltages. For example, if 6 A is needed for the PC test, V_{GE} should be 4.5 V when V_C is above 2.5 V.

V_{GE} of the DUT is controlled by the op-amp integrator for producing desired I_C where the current sensing voltage V_1, which is $(R_{I\_\mathrm{sense}} \cdot I_C)$ is compared with current reference voltage (V_{I_ref}), which is chosen by $(R_{I\_\mathrm{sense}} \cdot I_{\mathrm{ref}})$. At the initial state, V_{I_ref} is larger than $V_1 = 0$ and therefore V_{GE} starts to increase by the op-amp integrator and produce the current I_C under the applied V_C. As V_{GE} increases, I_C increases and makes the voltage drop in R_{I_sense}, which is V_1. V_{GE} is regulated to a constant value in order to generate the desired I_C if V_1 becomes the same value with V_{I_ref} and it means that I_C is controlled to I_{ref}. Consequently, the desired current for the PC test can be obtained by adjusting V_{I_ref} and V_{DC} can also be adjusted to obtain the wanted power dissipation to create the desired temperature stresses under the set current level by V_{I_ref}. Then, if the junction temperature is reached to the desired $T_{j\max}$, the DUT is turned off as conventional DC PC test by changing the V_{I_ref} value to 0. This test circuit has the additional control parameter V_{DC} for generating power losses compared with conventional DC PC test. Therefore, it has more variety to realize the PC test conditions and thus high current may be not necessary.

Fig. 8 shows the extended PC test circuit for half-bridge power device modules. The lower IGBT has the same current controller with the circuit in Fig. 6. The upper IGBT has a feedback loop by the op-amp integrator which makes sure that both IGBT have the half of V_{DC} across two IGBTs while current is flowing so

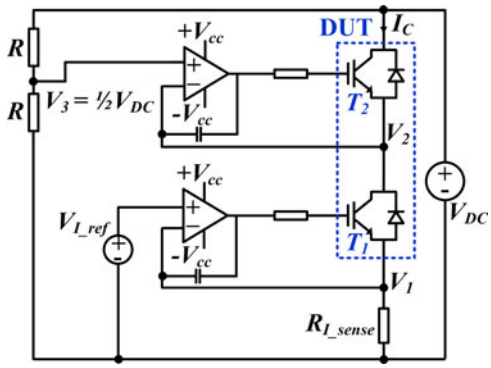

Fig. 8. Configuration of the DC power cycling test setup with saturation mode of DUT for half-bridge power device module.

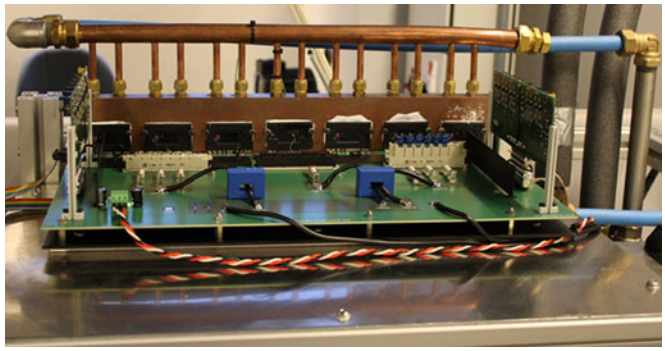

Fig. 9. Prototype of the DC power cycling test setup with saturation mode of power IGBT modules.

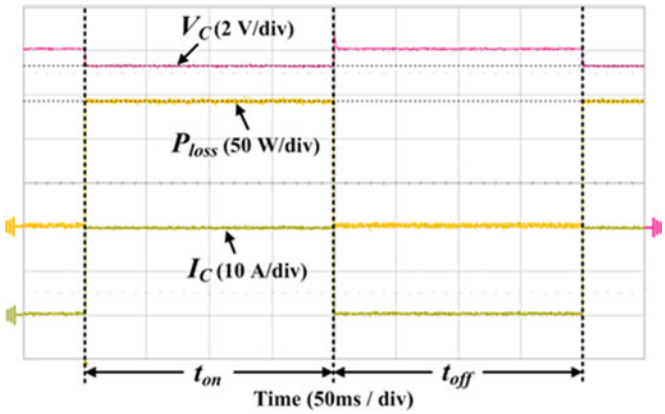

Fig. 10. Experimental result of the DC power cycling test with saturation mode of the DUT when $V_{\mathrm{DC}} = 8$ V, $I_{\mathrm{ref}} = 20$ A, $R_{I\_\mathrm{sense}} = 0.04\,\Omega$, $V_{I\_\mathrm{ref}} = 0.8$ V, and t_{on}, $t_{\mathrm{off}} = 2$ s.

that both IGBTs dissipate the same power during the PC test for the same temperature stress.

Fig. 9 shows the prototype of the DC PC test circuit with saturation mode of three-phase power IGBT modules.

Fig. 10 shows the experimental result of the DC PC test circuit with the saturation mode of the DUT when $I_{\mathrm{ref}} = 20$ A, $V_{\mathrm{DC}} = 8$ V, $R_{I\_\mathrm{sense}} = 0.04\,\Omega$, and $V_{I\_\mathrm{ref}} = 0.8$ V. As shown in the result, I_C is controlled to 20 A and 7.2 V of V_C is applied to the DUT and thus 144 W of the power loss is generated in the DUT when it is turned on for 2 s. Then, it is turned off for 2 s in

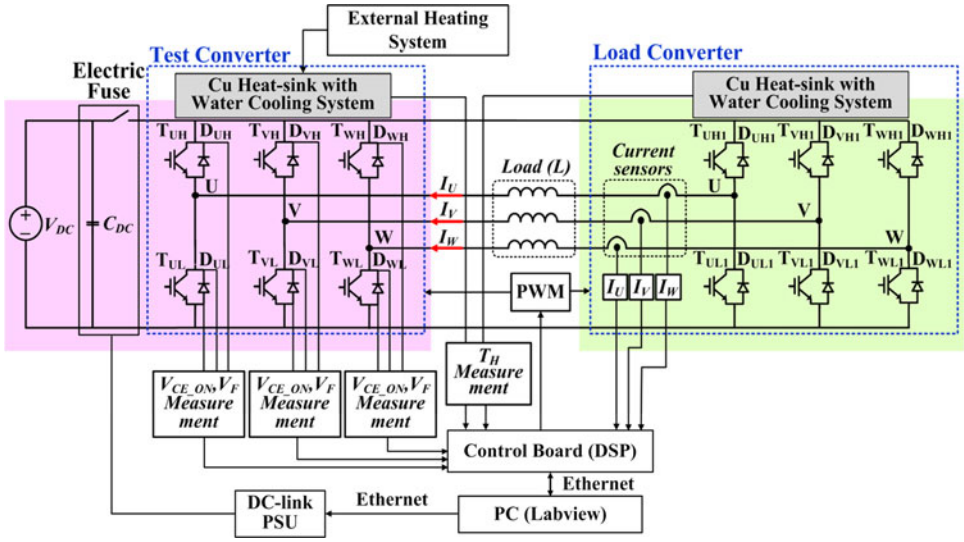

Fig. 11. Configuration of the AC power cycling test setup [56], [57].

order to generate temperature swing. The both I_C and $V_{\rm DC}$ can be varied in order to generate different power losses depending on desired temperature stresses for the PC test.

B. AC Power Cycling Test Circuit Close to Real Converter Applications [18], [56]–[59]

As power device modules play a key role in the reliability of PESs, there is an increasing demand to perform the PC test close to real applications in order to minimize the uncertainty, which may be able to come from test conditions and to affect the test results.

In [60]–[62], the PC test is performed under converter operation with real inductive loads or motors. However, the PC test with real loads is not cost-effective because real loads consume large power during a long test period. In addition, in the case of PC test with only small load inductors, there are limitations to emulate the various operating conditions such as power factor, modulation index, etc. In order to complement disadvantages mentioned above, a new configuration has been proposed.

Fig. 11 shows the configuration of an advanced AC PC test setup proposed in [56]. This test setup mainly consists of three parts; test converter board, load converter board, and control board. The outputs of an IGBT module under test of the test converter are connected with the outputs of an IGBT module of the load converter through small load inductors (L) and they share common DC source ($V_{\rm DC}$). The on-state collector–emitter voltages ($V_{\rm CE\_ON}$) of the IGBTs and forward voltages (V_F) of the diodes are measured in real time in order to determine the wear-out condition of the IGBT module under test. For the load converter, an IGBT module, which has a higher rated power than the tested module, is used in order to reduce the effect of the thermal stresses on the load IGBT module during PC tests. By using the higher rated power module, the load converter can run for a long time even though the tested IGBT modules are changed after a certain number of PC tests. A water cooling system and external temperature controllable heating system are used to change the heat-sink temperature depending on desired test conditions and to keep the heat-sink temperature as a constant during the PC test.

This system is controlled such as three single-phase half-bridge converters as shown in Fig. 12. In the phase-U, for example, the test converter generates the output voltage ($V_{U\_\rm ref\_test}$) that fulfills the required test conditions such as magnitude, output frequency with a determined switching frequency by an open-loop voltage controller.

The load converter produces the output voltage ($V_{U\_\rm ref\_load}$) by a closed-loop current controller in order to generate the current with the desired magnitude, frequency, and power factor for the PC test. The output current (I_U) is generated by the difference of the output voltages (V_L) between the test and load converters as shown in Fig. 13, which is applied to the inductor. It means that the voltage is applied across the inductor during a short period. Therefore, small inductors are sufficient as loads in order to obtain an acceptable low current ripple. The controls for the other phases are the same as explained above, but there is only 120° and 240° shifting in phase angle to simulate a three-phase converter system.

In this topology, there are only power losses by the tested and load IGBT modules and small load inductors. Although, the rated output currents are generated, the power consumption by the test setup can be kept very low. Therefore, it is a cost-effective solution. However, this topology has some disadvantage such as complexity of structure and control and difficulty in monitoring of failure indicators in real time. It is also relatively expensive to build the test system.

Fig. 14 shows a prototype of the PC test setup based on the configuration shown in Fig. 11.

In this system, a 600 V, 30 A, three-phase transfer-molded power IGBT module is used for the test converter. A 1200 V, 75 A, three-phase IGBT module is used for the load converter, and 0.5 mH inductors are used for the loads.

Depending on target modules for the test, the topology of the test setup can be modified. For example, if the target power

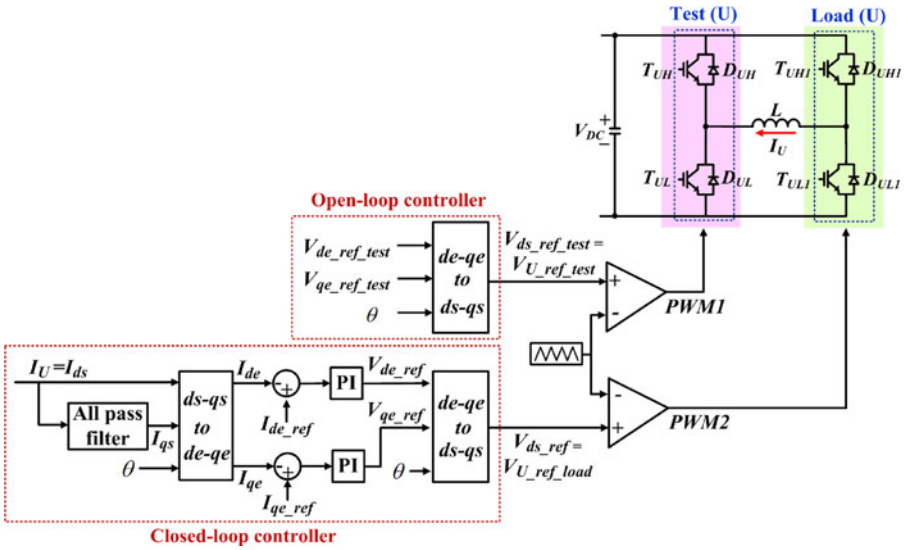

Fig. 12. Control block diagram of the AC power cycling test circuit [56].

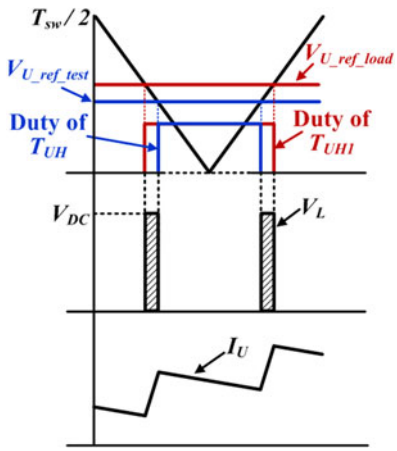

Fig. 13. Reference voltages for load and test converters and corresponding inductor voltage and output current [56].

device module consists of a single leg, the PC test setup can be designed as a single-phase converter system as shown in Fig. 15(a) [18]. If the rated power of the target module is high, it is difficult to find power device modules, which have higher rated power than the target module for the load converter. In this case, the topology can be altered as shown in Fig. 15(b) for a single-phase system [58] and for three-phase system as shown in Fig. 15(c), where two load modules are operated by the same gate signal so that the half of load current flows in each load module [59].

Typically, in the PC test, high $\triangle T_j$ (40 °C∼100 °C) and $T_{\rm jm}$ (60 °C∼120 °C) are applied to the DUT in order to obtain test results in a reasonable test time [16], [31].

There are two ways to apply the temperature stress to DUT in the AC PC test method. Sinusoidal output current leads to $\triangle T_j$ in DUT but it is difficult to get a high $\triangle T_j$ with high output frequency. Therefore, sinusoidal current with low output frequencies, less than ten hertz, is applied to DUT as shown in Fig. 16(a). By changing the output frequency, magnitudes of output current and voltage, and heat-sink temperature, different $\triangle T_j$ and $T_{\rm jm}$ can be achieved. In this method, high $\triangle T_j$ can be obtained in a relatively short cycle period [56]. The other way is that the regulated sinusoidal output current with high frequency such as 100 Hz is applied to DUT for a certain period of time. If the junction temperature is reached to the required maximum temperature for desired $\triangle T_j$, the injection of output current is stopped similar to the conventional DC PC test.

Then, the junction temperature is decreased by external cooling system as shown in Fig. 16(b) [18]. In this method, high $\triangle T_j$ can be obtained in a relatively long cycle period. By changing the magnitude of output current, power injection time, switching frequency, heat-sink temperature, etc., different $\triangle T_j$ and $T_{\rm jm}$ can be achieved. Between them, a proper method can be chosen depending on the desired test conditions and target applications.

The features of presented three test circuits are summarized in Table II.

IV. $V_{\rm CE\_ON}$ and V_F Measurements Techniques

The on-state collector–emitter voltage $(V_{\rm CE\_ON})$ of IGBTs and forward voltage (V_F) of diodes are good indicators for determining the wear-out condition of power device modules in respect to bond-wire degradation, delamination of the solder joints, and chip metallization degradation. By measuring $V_{\rm CE\_ON}$ and V_F, the bond-wire fatigues of the tested module can be monitored during the accelerated PC test. Furthermore, the junction temperature of the tested module can be estimated by measuring $V_{\rm CE\_ON}$ and V_F for determining the solder joint fatigue.

A. *Offline* $V_{\rm CE\_ON}$ *and* V_F *Measurements*

Real-time monitoring of failure indicators is not simple especially for the AC PC tests because it requires high-voltage prediction, high accuracy for measurement of low values, and short transient time for measurement in circuit [51]. Therefore,

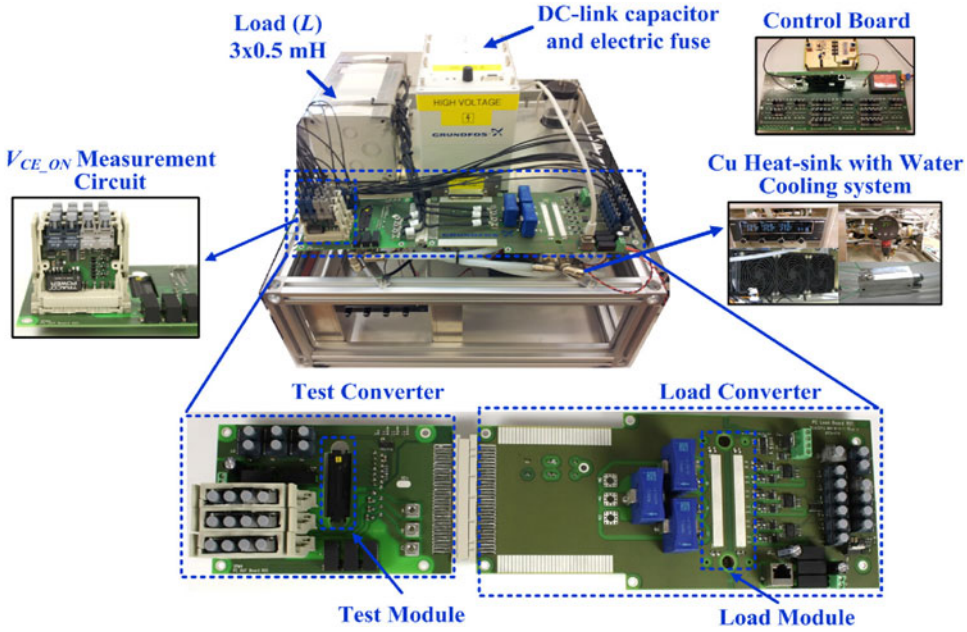

Fig. 14. Prototype of the advanced accelerated power cycling test setup [56], [57].

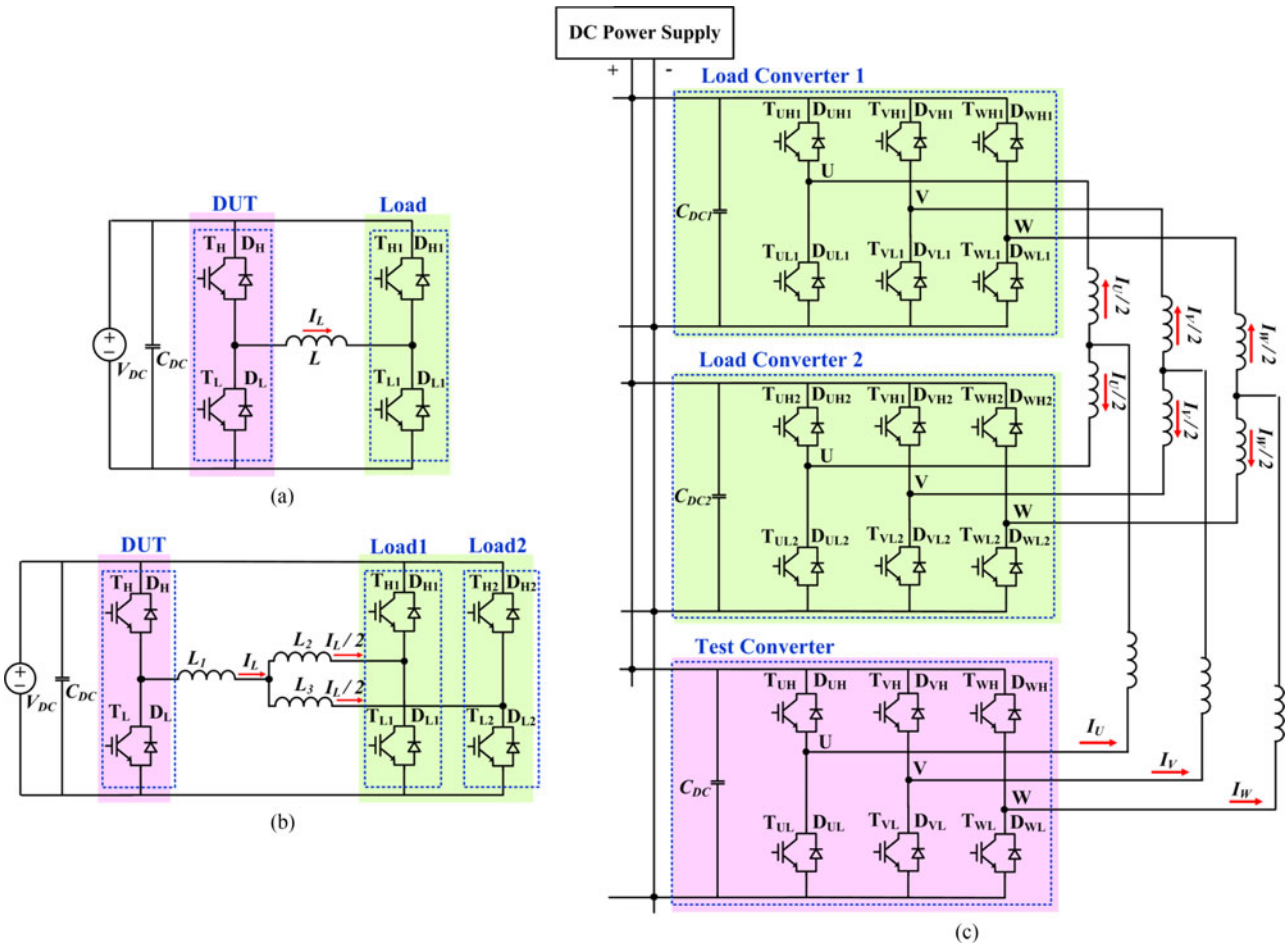

Fig. 15. Modified AC power cycling test topologies for different power device modules (a) single-phase PC test system [18], (b) single-phase PC test system for high-rated power device modules [58], and (c) three-phase PC test system for high-rated power device modules [59].

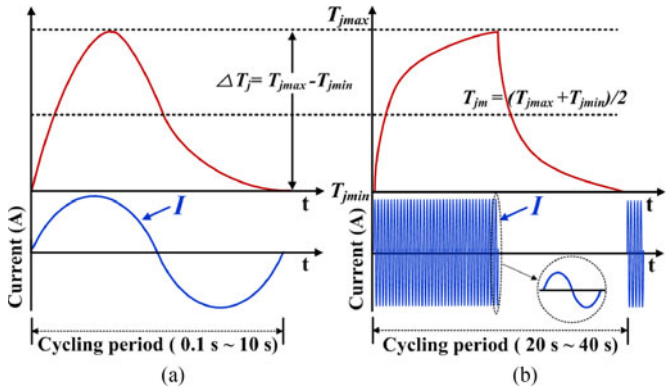

Fig. 16. Strategies to apply temperature swing to DUT (a) temperature swing by low-frequency sinusoidal current [56] and (b) temperature swing by high-frequency current injection [18].

offline measurements are used widely in the PC test. The offline measurement means that the operation of PC test circuits is stopped or the high DC voltage is disconnected if the test circuit has it and then the monitoring parameters are measured with special sequences. The offline measurement is performed in a specific period. For example, every 5000 cycles if there are no visible change in the monitoring parameters and if any changes are detected, it is reduced to 1000 cycles.

One of the main methods for offline measurement of $V_{\mathrm{CE\_ON}}$ is proposed in [63] and [64].

Fig. 17(a) shows the offline measurement method with high and small current injections. The measurement procedure is simple. For example T_{UH}, when the DUT is turned off, the high DC voltage is clamped to a certain small value by a zener diode (in this paper, 10 V) and the current by high DC-link voltage is limited by the resistors R_{H1} and R_{H2}.

For the $V_{\mathrm{CE\_ON}}$ measurement of T_{UH}, only T_{UH} is turned on after all operation is stopped. Then, the high current is injected by external current sources for the certain period (344 μs) and $V_{\mathrm{CE\_ON}}$ of T_{UH} is measured at the end of high current pulse. Then, $V_{\mathrm{CE\_ON}}$ of T_{UH} is measured at 100 mA just after high current injection is stopped and this value is used for junction temperature estimation. The delay time between two measurements should be kept short in order to keep junction temperature almost the same between two measurements.

Fig. 17(b) shows the measurement timing with current injection where red dots are the measurement point. Depending on the target device of DUT, the relay connection is changed in order to transform the circuit connection.

The other offline measurement is using reed relay for the AC PC test circuit [65].

Fig. 18(a) shows the AC PC test circuit with reed relay. In this method, the additional current source is not required. The relay is disconnected when the PC test is performed. After the test is stopped for the $V_{\mathrm{CE\_ON}}$ measurement, the relay is turned on. Then, the simple current injection switching sequence is applied to measure $V_{\mathrm{CE\_ON}}$ at high current. Fig. 18(b) shows the simple switching sequence for $V_{\mathrm{CE\_ON}}$ measurement of T_{UH} as an example.

In order to generate the current, T_H and T_{L1} are turned on (1) in the Fig. 18(b). The current level can be varied by changing the dwell time of turn-on state of T_H and T_{L1}. Then, T_{L1} is turned off so that the current flows through T_H and D_{H1} (2) in the Fig. 18(b). $V_{\mathrm{CE\_ON}}$ of T_H and the current are measured at this point. After $V_{\mathrm{CE\_ON}}$ and the current are measured, T_H is turned off in order to reduce the current to zero (3) in the Fig. 18(b). It is worth to mention that $V_{\mathrm{CE\_ON}}$ should be measured at the same current level and at the same temperature.

B. Real-Time $V_{\mathrm{CE\_ON}}$ and V_F Measurements

1) $V_{\mathrm{CE\_ON}}$ and V_F Measurements With a Parallel-Connected MOSFET [66], [67]: This circuit consists of V_{CE} clamp (V_{Z1}, R_{Z1}, AS_{C1}, R_{C1}, and V_{Z2}, R_{Z2}, AS_{C2}, R_{C2}), 100 mA current sink (AS_1, R_{TJ1} and AS_2, R_{TJ2}), and a voltage-level shifter (OA1, $\mathrm{AS}_{\mathrm{LA1}}$, R_{LA1}, R_{m1} and OA2, $\mathrm{AS}_{\mathrm{LA2}}$, R_{LA2}, R_{m2}).

The operating principle is explained by considering the $V_{\mathrm{CE\_ON}}$ measurement of T_{UH}. In this circuit, the following relations can be obtained as

$$V_{\mathrm{RC1}} = V_{\mathrm{CE}} - v_{\mathrm{ASC1}} = V_{Z1} - V_{\mathrm{SG1}}. \tag{3}$$

$$V_{\mathrm{SG1}} = V_{Z1} - V_{\mathrm{CE}} + v_{\mathrm{ASC1}}. \tag{4}$$

If T_H is turned on, AS_{C1} is turned on because V_{CE} of T_H is small and thus $V_{\mathrm{SG1}} = V_{Z1} - V_{\mathrm{CE}} + v_{\mathrm{ASC1}}$ becomes larger than threshold voltage of $\mathrm{AS}_{\mathrm{C1}}$ (V_{SGTH1}). In this case, V_{RC1} is almost equal to the on-state collector emitter voltage ($V_{\mathrm{CE\_ON}}$) of T_H because the on-state drain–source resistance (R_{DSON}) of AS_{C1} is relatively much smaller than R_{C1} ($R_{\mathrm{DSON}} = 3\,\Omega$ and $R_{C1} = 10\,\mathrm{k}\Omega$). If V_{CE} increases above the clamping voltage $V_{Z1} - V_{\mathrm{SGTH1}}$ by turning off T_H, AS_{C1} starts to be operated in the saturation region. The high voltage is applied to AS_{C1} and R_{Z1} and V_{RC1} is clamped to a certain value, which is close to $V_{Z1} - V_{\mathrm{SGTH1}}$ (10 V in this paper). Then, through the amplifier OA1, V_{RC1}, which is $V_{\mathrm{CE\_ON}}$ when T_H is turned on or clamping voltage when T_H is turned off is reproduced on the resistor R_{LA1}. The current i_{m1}, equal to $V_{\mathrm{RC1}}/R_{\mathrm{LA1}}$, is generated and conveyed by $\mathrm{AS}_{\mathrm{LA1}}$. This current makes the voltage drop in R_{m1} and this value is measured through ADC1.

This measurement principle allows transmitting $V_{\mathrm{CE\_ON}}$ information through high current value (a few dozen mA) to analog-to-digital converters (ADC1 and ADC2) of the control boards with the benefit of a high immunity transmission.

Small 100 mA current can simply be obtained by properly selecting R_{TJ1} and R_{TJ2} values depending on V_{DC} (100 mA $= V_{\mathrm{DC}}/R_{\mathrm{TJ1}}$). The current injections into T_H and T_{UL} are performed by turning on A_{S1} and A_{S2}, respectively, and $V_{\mathrm{CE\_ON}}$ under 100 mA is used for the junction temperature estimation.

2) $V_{\mathrm{CE\_ON}}$ and V_F Measurements Using Double Diodes [68], [69]: Fig. 20 shows the schematic of $V_{\mathrm{CE\_ON}}$ and V_F measurement circuit using double diodes.

Two diodes D_1 and D_2 are connected in series and they are forward-biased by the current source (I_D) when the transistor (T_H) is turned on. If T_H is turned off, D_1 blocks the high V_{CE} voltage, which comes from the DC-link to protect the measurement circuitry. Assuming diodes D_1 and D_2 have

TABLE II
SUMMARY OF POWER CYCLING TEST CIRCUITS FOR POWER DEVICE MODULES

	Power Cycling (PC) test circuits		
	Conventional DC power cycling circuit	DC power cycling circuit with saturation mode of DUT	AC power cycling circuit
Loss for temperature stress of DUT	Conduction loss	Conduction loss (adjusted by V_{DC} without changing current level)	Conduction and switching losses
Cost	Low	Low	High
Complexity	Low	Moderate	High
Controllable parameters for PC test conditions	I, T_s, V_{GE}	I, T_s, V_{GE}, V_{DC}	I, T_s, V_{GE}, V_{DC}, V_{OUT}, f_{OUT}, f_{SW}, PF
Advantages	- Simplicities in operating test circuit and measuring monitoring parameters. - Possible to test a lot of DUTs at the same time.	- More variety to realize the test condition compared with the conventional DC PC test. (No high current and no longer cycle period (T_s))	- DUT is operated under realistic electrical conditions close to real converter applications. - Variety to realize PC test conditions.
Disadvantage	- DUT is not under realistic electrical conditions. - High current is required. - Limitation to realize various test conditions.	- Not applicable for power modules that have gate drivers inside of modules. - Difficulty in applying online measurement of failure indicators during PC test.	- Complexities in operating test circuit and measuring monitoring parameters. - Relatively expensive to build test system.

I: current, T_s: cycle period, V_{GE}: gate–emitter voltage, V_{DC}: DC-link voltage, V_{OUT}: output voltage, f_{OUT}: output frequency, f_{SW}: switching frequency, and PF: power factor.

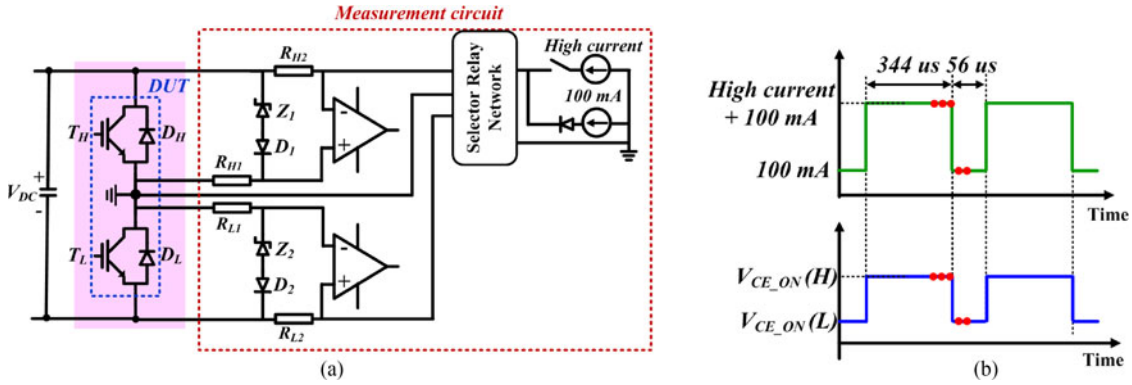

Fig. 17. Offline measurement with voltage clamping circuit using a zener diode [63], [64] (a) measurement circuit and (b) measurement points.

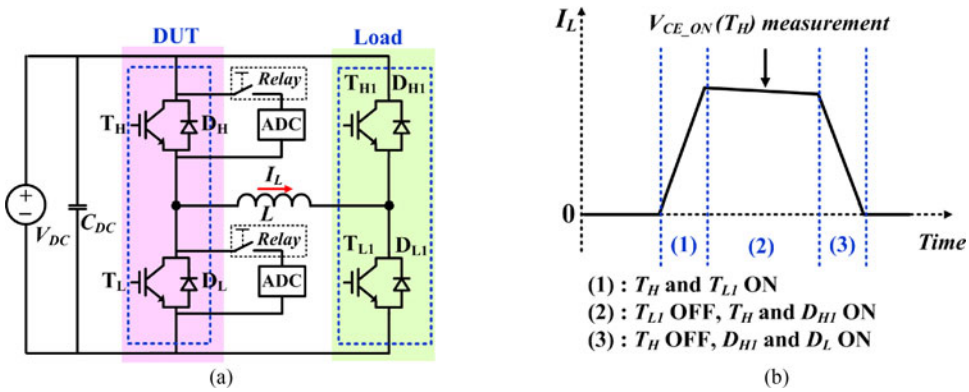

Fig. 18. Offline measurement with a reed relay [65] (a) measurement circuit and (b) switching sequence for measurement.

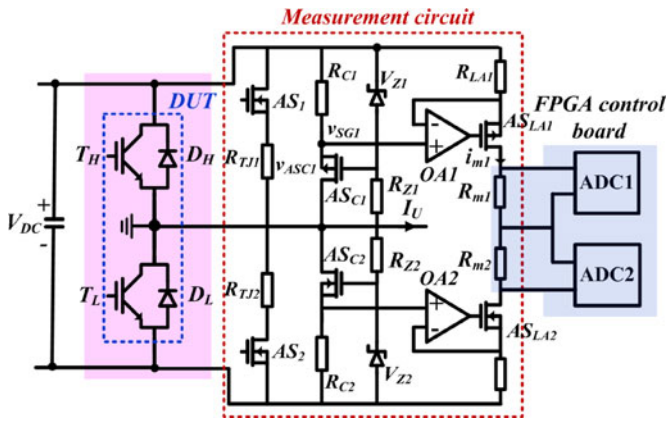

Fig. 19. Schematic of the online $V_{\mathrm{CE\_ON}}$ and V_F measurement circuit with a parallel-connected MOSFET [66].

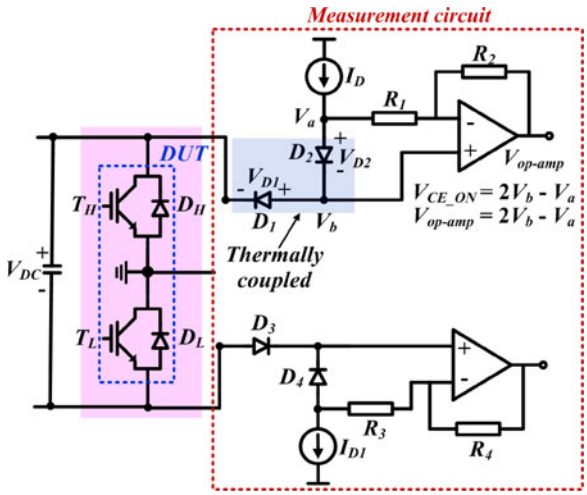

Fig. 20. Schematic of the online $V_{\mathrm{CE\_ON}}$ and V_F measurement circuit using double diodes [68].

the same characteristics, the forward voltage of D_1 and D_2 can be represented as

$$V_{D1} = V_{D2} = V_a - V_b. \tag{5}$$

For example, T_{UH}, $V_{\mathrm{CE\_ON}}$ can be expressed by the difference between the voltage potential V_b and V_{D1} as

$$V_{\mathrm{CE\_ON}} = V_b - V_{D1} = V_b - (V_a - V_b) = 2V_b - V_a. \tag{6}$$

The above-mentioned result can be realized by choosing properly the gain of amplifier. If $R_1 = R_2$, the output of amplifier can be expressed as

$$V_{\mathrm{op-amp}} = V_b - ((V_a - V_b) \cdot R_2/R_1) = 2V_b - V_a = V_{\mathrm{CE\_ON}}. \tag{7}$$

The output of the amplifier is the same with $V_{\mathrm{CE\_ON}}$ as described in (6). $V_{\mathrm{CE\_ON}}$ is measured during the positive current as a positive value and V_F is measured during the negative current as a negative value, where the current from the DUT to loads is a positive direction.

3) $V_{\mathrm{CE\_ON}}$ and V_F Measurements Using a Depletion Mode Small Signal MOSFET [70], [71], [92]: Fig. 21 shows a real-time measurement circuit of on-state collector–emitter voltages $(V_{\mathrm{CE\_ON}})$ of IGBTs and forward voltages (V_F) of diodes using a depletion mode MOSFET, which has a negative threshold voltage $(V_{\mathrm{GS}} < 0)$. In this circuit, the clamping voltage (V_{CC}) should be larger than that of $V_{\mathrm{CE\_ON}}$ and V_F and the input impedance (Z_{in}) for the measurements of $V_{\mathrm{CE\_ON}}$ and V_F should be high enough.

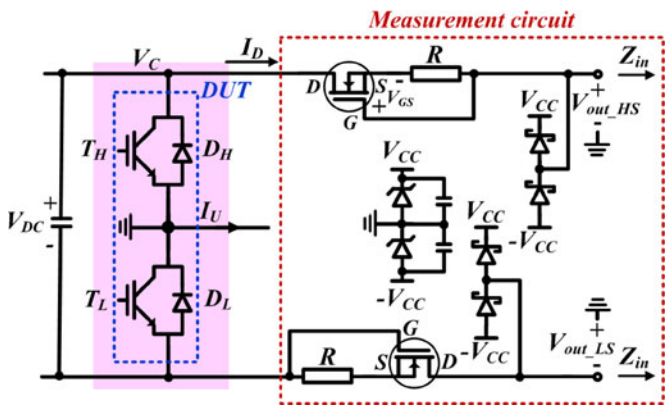

Fig. 21. Schematic of the online $V_{\mathrm{CE\_ON}}$ and V_F measurement circuit using a depletion mode MOSFET [92].

The operating principle is explained considering the $V_{\mathrm{CE\_ON}}$ measurement of T_H as an example. When T_H is tuned-on, the current I_D does not flow through the MOSFET because the collector voltage $V_C = V_{\mathrm{CE\_ON}} < V_{\mathrm{CC}}$ and Z_{in} is high. Thus, $V_{\mathrm{GS}} = 0$. Consequently, the MOSFET is turned on and $V_{\mathrm{out}} = V_{\mathrm{CE\_ON}}$. As V_C increases above the clamping voltage V_{CC} by turning off T_{UH}, I_D starts to flow and makes a voltage drop in R. As I_D increases, V_{GS} decreases and finally the MOSFET is turned off if V_{GS} becomes smaller than the threshold voltage (V_T) of the MOSFET. Therefore, the clamping voltage V_{CC} is measured at the output during this period. $V_{\mathrm{CE\_ON}}$ of T_H is measured during the positive current period as a positive value and V_F of D_H is measured during the negative current period as a negative value where the current from the DUT to load is a positive direction. The measurement of $V_{\mathrm{CE\_ON}}$ and V_F for the low side IGBT and diode can be interpreted in a similar way. $V_{\mathrm{CE\_ON}}$ and V_F are measured during the negative current period as a negative value and the positive current period as positive value, respectively.

The introduced $V_{\mathrm{CE\_ON}}$ and V_F measurements methods are summarized in Table III.

V. Junction Temperature Measurement Techniques

The junction temperature of DUT is important in order to know precise applied temperature stress such as junction temperature swing $(\triangle T_j)$, mean junction temperature (T_{jm}) when the PC test is performed. Furthermore, from the junction temperature, it is possible to monitor the thermal impedance change which is one of the main failure indicators during the PC test as mentioned in Section II-B. In this paragraph, different junction temperature measurements techniques are discussed.

TABLE III
SUMMARY OF $V_{\mathrm{CE\_ON}}$ AND V_F MEASUREMENT METHODS DURING POWER CYCLING (PC) TESTS

	Method	Advantages	Disadvantage
Offline	Voltage clamping by a zener diode [63], [64]	- Both monitoring of bond-wire fatigue and solder join fatigue are possible. - No dependence on PC test conditions.	- Additional current sources are required. - Additional selector switches and their controls are required for transformation of circuit connection. - PC test must be stopped for monitoring of failure indicators.
	Relay [65]	- Additional current sources are not required. - Very simple circuit. - No dependence on PC test conditions.	- Switching of relay for measurement is not fast enough. - Suitable only for AC PC test (possible for DC PC test if there are additional current source). - PC test must be stopped for monitoring of failure indicators.
Online	Measurement circuit with a parallel MOSFET [66], [67]	- Possible to inject low current for the junction temperature estimation. - Real-time monitoring of failure indicators is possible	- The failure of parallel connected MOSFET may lead to short-circuit of power device. - Relatively complex circuit.
	Measurement circuit with double diodes [68], [69]	- Relatively simple circuit. - Real time monitoring of failure indicators is possible	- Deviation between two diodes could lead to measurement error.
	Measurement circuit with a depletion mode small signal MOSFET [70], [71]	- Fast transient time for the measurement. - Suitable for high switching frequency operation. - Real-time monitoring of failure indicators is possible.	- For high DC-link voltage applications, small signal MOSFET should be connected in series because the maximum voltage rating of commercial depletion mode small signal MOSFET is 600 V.

A. Direct Junction Temperature Measurement Methods

For the PC test, a variety of junction temperature (T_j) measurement methods are available. Simple and correct methods are direct measurement methods such as optic fibers and infra-red (IR) cameras.

Fig. 22 shows an open IGBT module with optical fiber thermal sensors in direct contact to the die and case. This method allows measuring the junction temperature (T_j) and case temperature (T_c) at high voltage during IGBT operation under PC test [72]. However, this method has some disadvantages such as low response time of the sensor, and requirement of power device module modifications.

For the junction temperature measurement by the IR camera, the removal of dielectric insulating gel or molding compound is required. Furthermore, both die and bond-wires must be painted by black paint in order to obtain the homogenous emissivity across the surface of the die.

Fig. 23 shows the IGBT surface covered by black paint and the measurement of junction temperature by the IR camera [73]. From this method, quite correct junction temperatures can be obtained. However, this method requires modification of power device modules. Furthermore, a high resolution IR camera is relatively expensive. Finally, high-voltage operation may be unsafe due to the absence of dielectric gel or molding compound.

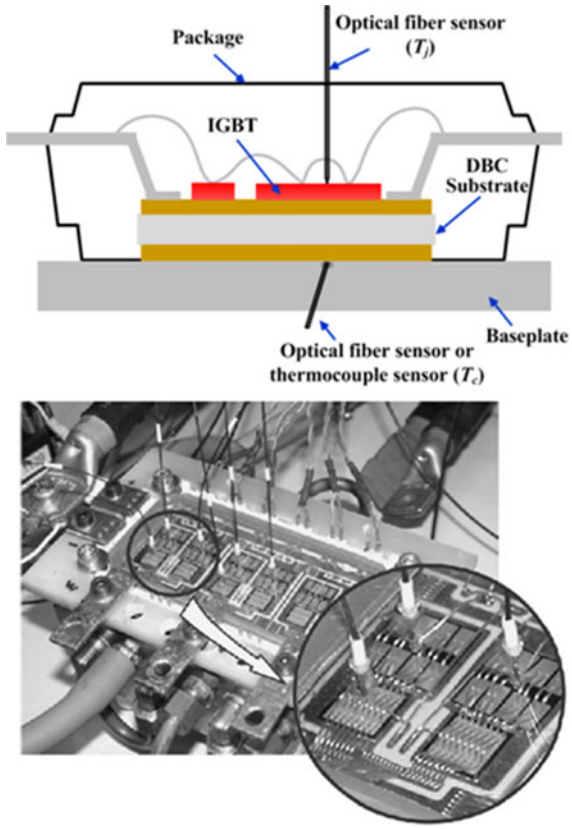

Fig. 22. Junction temperature and case temperature measurements by optic fiber sensors [72].

B. Indirect Junction Temperature Measurement Methods

1) Junction Temperature Estimation Method by $V_{\mathrm{CE\_ON}}$ at High Current [51], [66], [74]–[76]: The junction temperature (T_j) can be obtained from $V_{\mathrm{CE\_ON}}$ of IGBT or V_F of the diode because they are temperature sensitive electric parameters (TSEPs). For T_j measurement from $V_{\mathrm{CE\_ON}}$, preliminary *I–V* characterization of power devices is essential in order to obtain the dependence of temperature on $V_{\mathrm{CE\_ON}}$.

Fig. 24 shows the *I–V* characterization curves of an IGBT under different temperatures.

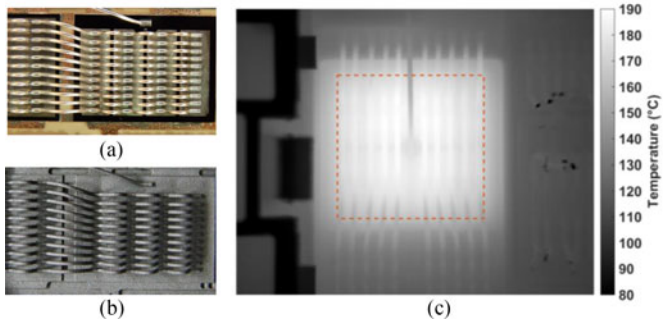

Fig. 23. Junction temperature measurement of IGBT by the IR camera (a) before painting, (b) after painting, and (c) IR image of IGBT [73].

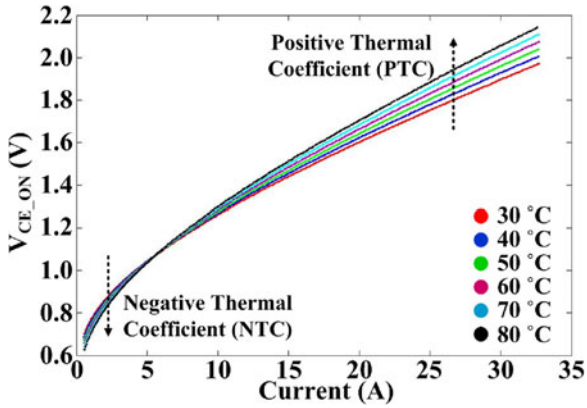

Fig. 24. *I–V* characterization curves of an IGBT.

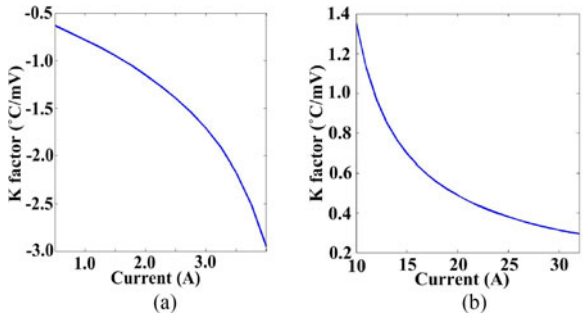

Fig. 25. *K*-factors depending on current levels (a) NTC region and (b) PTC region.

It is needed to derive $V_{\mathrm{CE\_ON}}$ as a function of temperature at a given current level in order to get T_j from the *I–V* characteristic curves. In order to derive the relation between $V_{\mathrm{CE\_ON}}$ and T_j, $V_{\mathrm{CE\_ON}}$ should be expressed as a function of the current. Then, the temperature variation can be represented as a function of $V_{\mathrm{CE\_ON}}$ at a given current by *K*-factor (*K*) as shown in Fig. 25. Based on the above-mentioned relations, T_j can be estimated from the measured current and $V_{\mathrm{CE\_ON}}$ as follows:

$$T_{j\_\mathrm{est}} = K_{(I)} \cdot \left(V_{\mathrm{CE\_}M} - V_{\mathrm{CE\_}B(I)}\right) + T_B. \tag{8}$$

where $K_{(I)}$ is the *K*-factor as a function of current, $V_{\mathrm{CE\_}M}$ is the measured on-state V_{CE} in real time, and $V_{\mathrm{CE\_}B(I)}$ is the base on-state V_{CE} as a function of current, which can be chosen among the characterization curves. T_B is the base temperature corresponding to the base on-state V_{CE}.

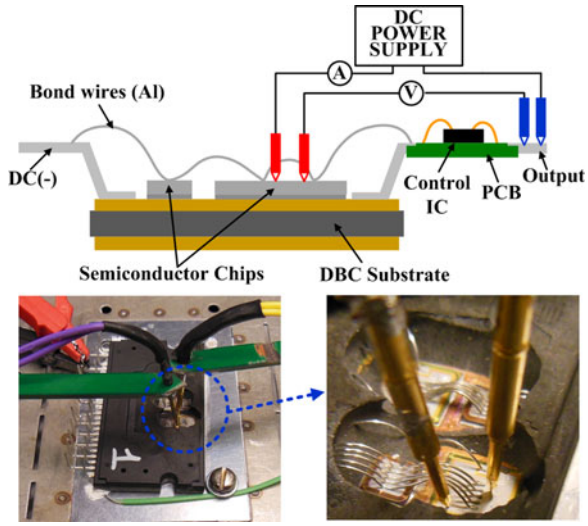

Fig. 26. Four-point probing method for the interconnection resistance measurement in an open module [56], [77].

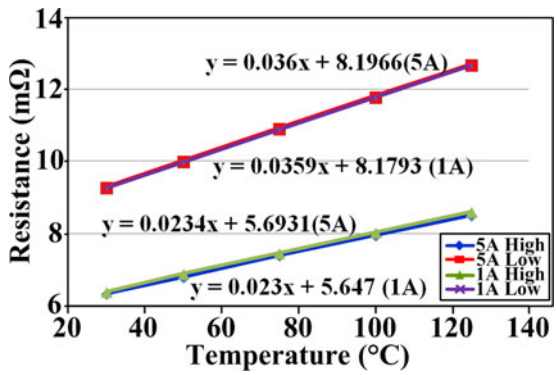

Fig. 27. Measured parasitic package resistances of high- and low-side IGBTs in an open module as a function of temperature [56], [77].

However, packaged devices do not permit to solely measure $V_{\mathrm{CE\_ON}}$ of the IGBT. The measured $V_{\mathrm{CE\_ON}}$ includes voltage drops on various interconnection elements such as bond-wires and it may cause a large temperature measurement error. This is because the *I–V* characterization of IGBT is performed under the homogeneous temperature distribution of power device modules, but power device modules have a nonhomogeneous temperature distribution during PC test and therefore, R_{int} will make different voltage drops [77].

2) Junction Temperature Estimation Method by $V_{\mathrm{CE\_ON}}$ at High Current With Compensation [56], [77]: The compensation method for the effect of R_{int} on temperature measurement has been proposed in [56] and [77]. By measuring the interconnection resistance under different temperatures using a four-point probing method as shown in Fig. 26, a resistance variation factor (RVF) has been obtained as shown in Fig. 27.

Fig. 28 shows the simplified temperatures in the power module when an AC current is applied, where T_{j_chip} is the junction temperature of the die, T_{j_est} is the estimated junction temperature using $V_{\mathrm{CE\_ON}}$ and load current, $T_{R\mathrm{int}}$ is the average temperature of interconnection materials in the modules, and T_H is the heat-sink temperature, typically kept constant during

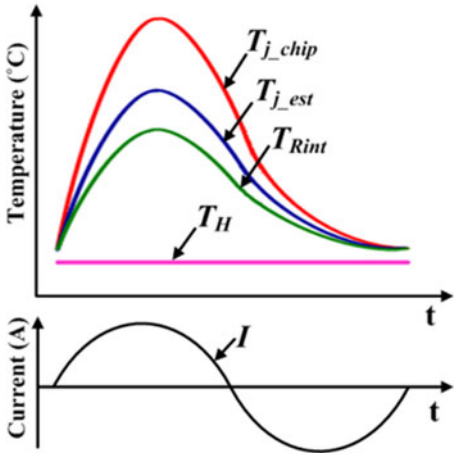

Fig. 28. Simplified temperatures in the power module when an AC current is applied [56], [77].

the PC test. The temperature difference between T_{j_chip} and $T_{R\mathrm{int}}$ makes the measurement errors $(T_{j\_\mathrm{chip}} - T_{j\_\mathrm{est}})$.

A reasonable assumption, which has been supported by the experimental observations, is that the temperature difference between T_{j_chip} and $T_{R\mathrm{int}}$ during one fundamental period of the output current has a similar trend with the temperatures as shown in Fig. 28. Therefore, it can be expressed as (9) and the resistance variation can be represented as (10). Therefore, on-state voltage compensation $V_{\mathrm{CE\_comp}}$ can be expressed as

$$T_{j\_\mathrm{chip}} - T_{R\mathrm{int}} = \alpha \cdot (T_{j\_\mathrm{est}} - T_H). \quad (9)$$

$$\Delta R_{\mathrm{int}} = \alpha \cdot (T_{j\_\mathrm{est}} - T_H) \cdot \mathrm{RVF}. \quad (10)$$

$$V_{\mathrm{CE\_comp}} = \Delta R_{\mathrm{int}} \cdot I = \alpha \cdot (T_{j\_\mathrm{est}} - T_H) \cdot \mathrm{RVF} \cdot I. \quad (11)$$

where T_H is the heat-sink temperature, α is the scaling factor, RVF is the resistance variation factor, and I is the output current. Finally, the equation for the junction temperature measurement by $V_{\mathrm{CE\_ON}}$ and load current is extended by including this factor as

$$T_{j\_\mathrm{est\_comp}} = K_{(I)} \cdot (V_{\mathrm{CE\_}M} - V_{\mathrm{CE\_}B(I)} + V_{\mathrm{CE\_comp}}) + T_B. \quad (12)$$

This method can improve the junction temperature measurement using $V_{\mathrm{CE\_ON}}$ at high current.

Fig. 29 shows the measured T_j by an IR camera and T_{j_est} before and after the compensation method is applied in the AC PC test. It can be seen from the results that the accuracy of the junction temperature estimation using $V_{\mathrm{CE\_ON}}$ at high currents is significantly improved.

A similar approach has also been published in [78], where finite element method simulation is used to find the resistance variation depending on temperatures.

This method requires efforts to find α and RVF for different kinds of power device modules. Furthermore, it requires a very accurate current sensor. In addition, the $V_{\mathrm{CE\_ON}}$ variation due to the bond-wire degradation affects the junction temperature measurement. Therefore, *I–V* characterization must be performed again to eliminate the bond-wire degradation effect.

Fig. 30 shows the online junction temperature monitoring result under the AC PC test where red arrow indicates the *I–V* recharacterization points. The estimated junction temperature T_{j_est} increases as $V_{\mathrm{CE\_ON}}$ increases. After the *I–V* recharacterization, T_{j_est} decreases to its initial value. It can be seen from the results that $V_{\mathrm{CE\_ON}}$ increases due to the bond-wire degradation.

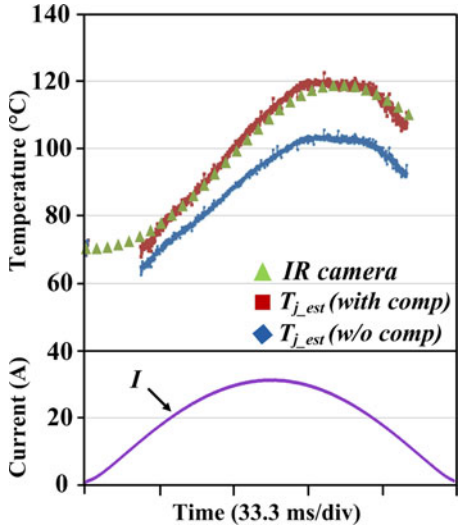

Fig. 29. Comparison of T_j measured by the IR camera and T_{j_est} before and after the compensation in the AC power cycling test ($f_{\mathrm{out}} = 3$ Hz) [56], [77].

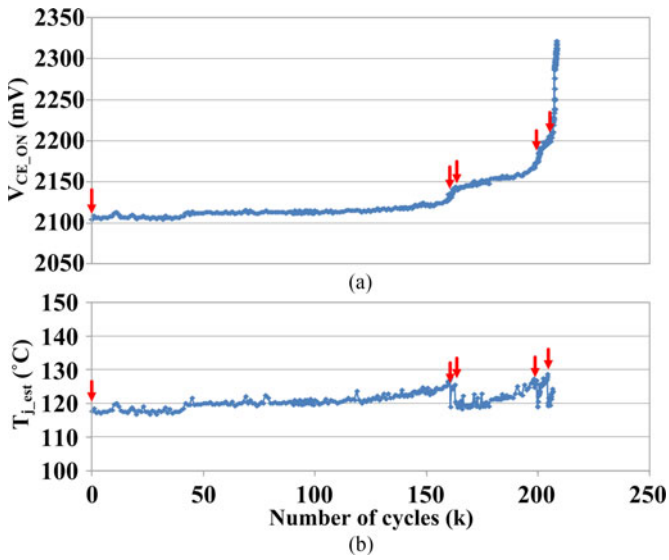

Fig. 30. Power cycling test result with junction temperature monitoring (a) on-state collector–emitter voltage ($V_{\mathrm{CE\_ON}}$) and (b) estimated junction temperature at 29 A [56].

Fig. 31 shows the change of parameters for the junction temperature estimation due to bond-wire fatigue during the PC test.

3) Junction Temperature Estimation Method by $V_{\mathrm{CE\_ON}}$ at Low Current [51], [63], [67], [79], [80]: The most commonly used method for the junction temperature estimation is $V_{\mathrm{CE\_ON}}$ at low constant sensing current generally in range of 1–100 mA. This method has the advantage that the effect of R_{int} variation on T_{j_est} can be reduced because $R_{\mathrm{int}} * I_C$ is relatively smaller than $V_{\mathrm{CE\_Chip}}$ in (1). This method requires also initial

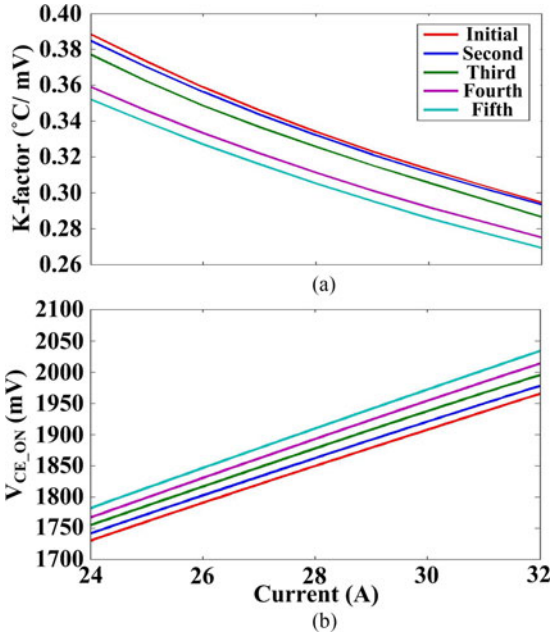

Fig. 31. Change of parameters for T_j estimation due to bond-wire fatigue during the power cycling test (a) *K*-factor (b) base $V_{\mathrm{CE\_ON}}$ as a function of current $(V_{\mathrm{CE\_}B(I)})$ at 30 °C [see (12)] [56].

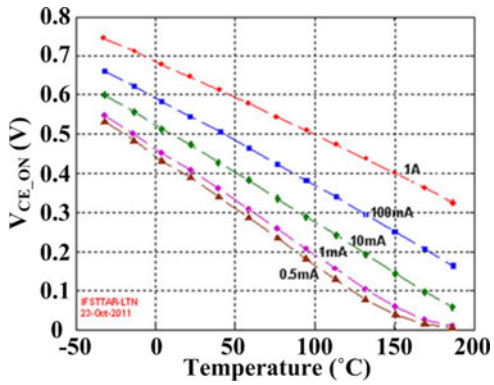

Fig. 32. $V_{\mathrm{CE\_ON}}$ of an IGBT as a function of temperature under different injected currents [79].

characterization of the DUT under different temperatures as shown in Fig. 32.

Fig. 33 shows the measurement points of $V_{\mathrm{CE\_ON}}$ at low current under the DC PC test [see Fig. 5(a)]. For junction temperature increase, high current is injected in the DC PC test by turning on a control switch. Then, the injection of high current is stopped in order to get the desired temperature swing and 100 mA is injected into this state for the temperature estimation. For $T_{j\max}$ estimation, $V_{\mathrm{CE\_ON}}$ is measured as soon as high current injection is stopped and only 100 mA current is injected. It is assumed that T_{j1}, just before stopping the high current injection, is almost the same with T_{j2}, just after the injection of 100 mA. The $V_{\mathrm{CE\_ON}}$ measurement for $T_{j\min}$ can be interpreted in a similar way. Consequently, T_{j_est} can be measured directly from $V_{\mathrm{CE\_ON}}$ at 100 mA as

$$T_{j\_\mathrm{est}} = K \cdot (V_{\mathrm{CE}\_M} - V_{\mathrm{CE}\_B}) + T_B. \tag{13}$$

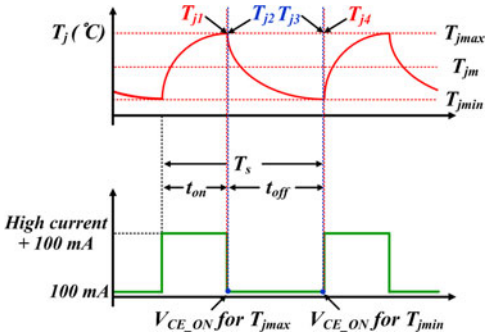

Fig. 33. Measurement points of $V_{\mathrm{CE\_ON}}$ at low current under the DC power cycling test [see Fig. 5(a)].

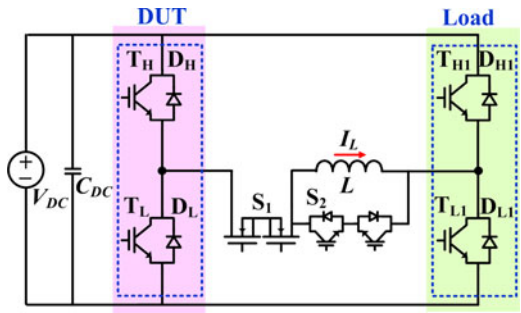

Fig. 34. AC power cycling test setup (see Fig. 15) with supplementary MOSFETs and IGBTs for junction temperature estimation [67].

where *K* is the *K*-factor, V_{CE_M} is the measured $V_{\mathrm{CE\_ON}}$ at 100 mA in real time, and V_{CE_B} is the base on-state V_{CE}. T_B is the base temperature corresponding to the base $V_{\mathrm{CE\_ON}}$.

In silicon devices, *K* has generally a negative temperature dependence of –2 mV/ °C. $V_{\mathrm{CE\_ON}}$ at low current can also be seen to depend highly on value of sensing current [79]. Therefore, the sensing current should be strictly controlled. Furthermore, the measurement of $V_{\mathrm{CE\_ON}}$ at low sensing current is impossible during normal load current commutation and thus this method is not proper for AC PC test. To apply this method for AC PC test, additional switches are included in order to interrupt the load current and isolate the DUT while the $V_{\mathrm{CE\_ON}}$ measurement at low sensing current is performed [67].

Fig. 34 shows the AC PC test setup [see Fig. 15(a)] where supplementary MOSFETs and IGBTs are placed in the load line. They can divert load current in 1 μs by turning off MOSFETs and turning on IGBTs. Then, the 100 mA sensing current is injected into desired IGBT and $V_{\mathrm{CE\_ON}}$ is used for T_j measurement. This procedure can be finished in a few hundreds of microseconds.

Fig. 35 shows a simulation of the interruption effect on the junction temperature based on the above-mentioned approach. In that case, all values are sampled in the same modulation period. A few degree variation of junction temperature can be observed during the $V_{\mathrm{CE\_ON}}$ measurement procedure but the estimated temperature agrees well with the measured temperature by the IR camera as shown in Fig. 36.

4) Junction Temperature Estimation Method by Internal Gate Resistance $(R_{G\mathrm{int}})$ *[73], [81], [82]:* This method is using

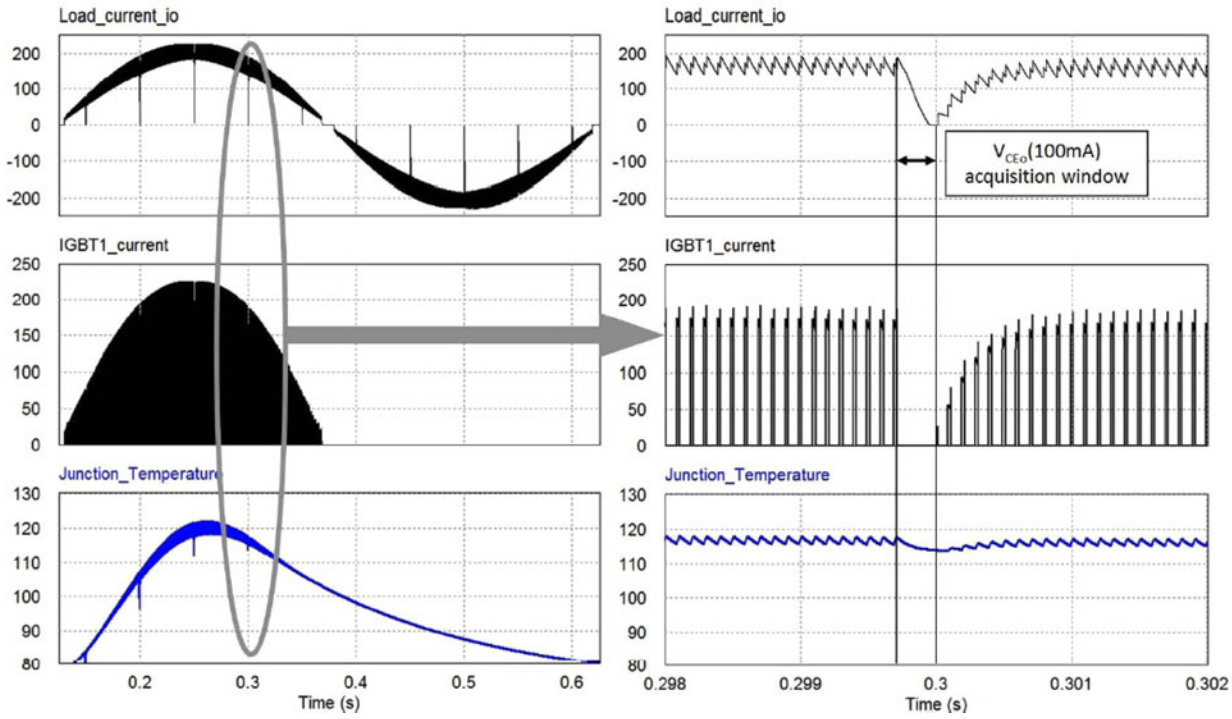

Fig. 35. Simulation result of the interruption effect on the junction temperature [67].

an internal gate resistance ($R_{G\mathrm{int}}$), which is located on the chip itself as a TSEP.

Fig. 37 shows $R_{G\mathrm{int}}$ of one IGBT inside an Infineon FS200R12PT4 module under different temperatures, measured by a Keysight E4990A impedance analyzer. A temperature sensitivity of 4.2 mΩ/ °C can be observed. The $R_{G\mathrm{int}}$ can be obtained from the peak gate current ($I_{G\mathrm{Peak}}$) and voltage swing of the gate driver. $I_{G\mathrm{Peak}}$ is measured during the normal charging cycle of the gate terminal during turn-on.

The gate circuit of IGBTs before the threshold voltage is reached (i.e., during turn-on delay) can be viewed as a step response of a second-order *RLC* circuit as shown in Fig. 38 including gate driver as a step voltage source, the parasitic gate inductance (L_G), both external ($R_{G\mathrm{ext}}$) and internal gate resistances ($R_{G\mathrm{int}}$), and gate capacitance (C_G). Under the assumption that L_G is kept low and the *RLC* circuit is sufficiently overdamped (i.e., $R^2 > 4L/C$), its behavior can be simplified as a first-order *RC* circuit where the initial charging current into the capacitor can be calculated as

$$I = \frac{V}{R} \cdot e^{-t/R_G C_G}$$
$$R_G \cdot C_G = (R_{G\mathrm{ext}} + R_{G\mathrm{int}}) \cdot [C_{\mathrm{GS}} + C_{\mathrm{GD}}(V_{\mathrm{DS}})]. \quad (14)$$

where $R_{G\mathrm{ext}}$ is the external gate resistance, $R_{G\mathrm{int}}$ is the internal gate resistance, C_{GS} is the gate–source capacitance (gate–emitter in IGBTs), C_{GD} is the gate–drain capacitance (gate–collector in IGBTs), and V_{DS} is the drain–source voltage (collector–emitter in IGBTs). From this, the peak gate current can be approximated by Ohm's law, $I \approx V/R$, where V is the voltage swing of the gate driver, and R is the total gate resistance. If it is assumed that the temperature dependence of

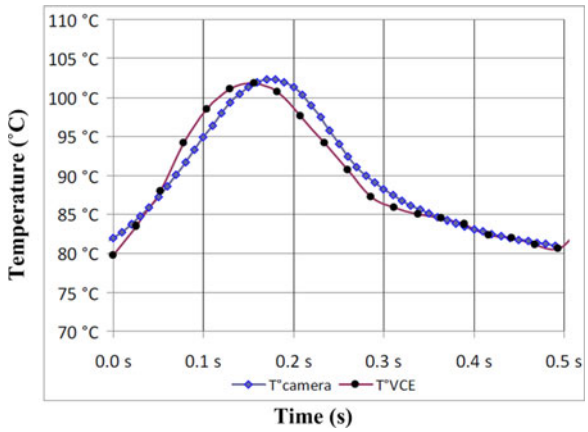

Fig. 36. Comparison of estimated junction temperature (T°V_{CE}) with measured temperature by the IR camera (T°camera) [67].

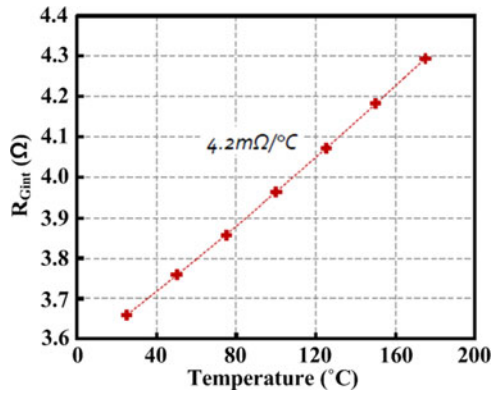

Fig. 37. $R_{G\mathrm{int}}$ of one IGBT inside an Infineon FS200R12PT4 module under different temperatures [81].

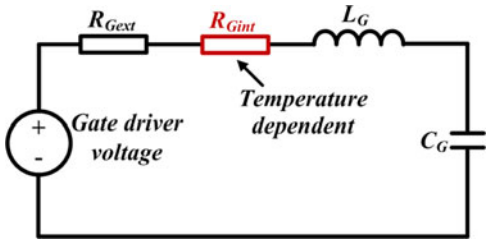

Fig. 38. Simplified gate circuit of IGBTs before the threshold voltage is reached.

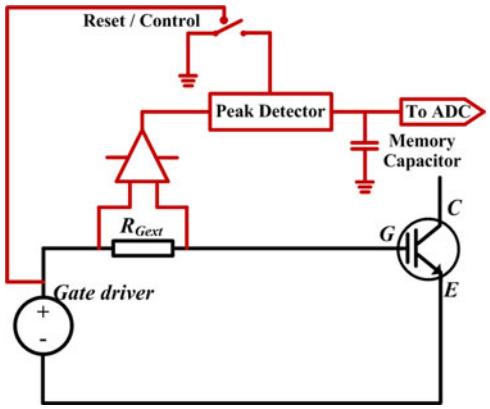

Fig. 39. $V_{RG\mathrm{ext}}$ peak detector schematic.

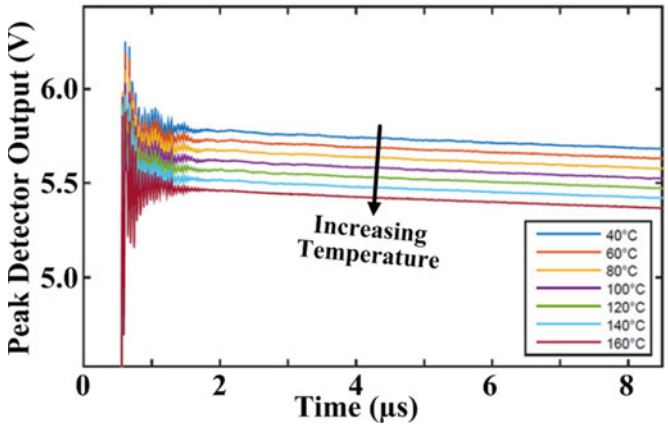

Fig. 40. Peak of $V_{RG\mathrm{ext}}$ by peak detector under different temperatures [81].

$R_{G\mathrm{ext}}$ is insignificant, C_G is stable until the gate voltage is reached to the threshold voltage and L_G has a negligible impact on the behavior of the circuit under overdamped condition. The variation of $R_{G\mathrm{int}}$ depending on temperature can be only cause of a peak gate current $(I_{G\mathrm{Peak}})$ change. $I_{G\mathrm{Peak}}$ can be monitored by measuring the voltage across $R_{G\mathrm{ext}}$ $(V_{RG\mathrm{ext}})$ as this voltage is directly proportional to $I_{G\mathrm{Peak}}$.

Fig. 39 shows the $V_{RG\mathrm{ext}}$ peak detector for obtaining $R_{G\mathrm{int}}$, which consists of a differential amplifier, a peak detector, a memory capacitor, and a reset switch, controlled by the gate voltage signal.

Fig. 40 shows the $V_{RG\mathrm{ext}}$ peak detector output on an Infineon FF200R12PT4 under different temperatures. From the peak of

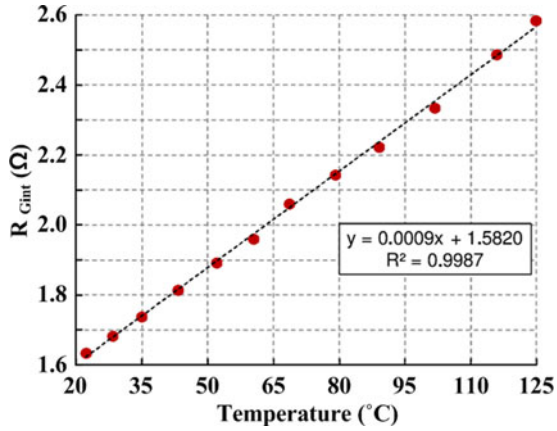

Fig. 41. Calculated $R_{G\mathrm{int}}$ of Infineon FF1000R17IE4 based on $V_{RG\mathrm{ext\_peak}}$ under different temperatures [81].

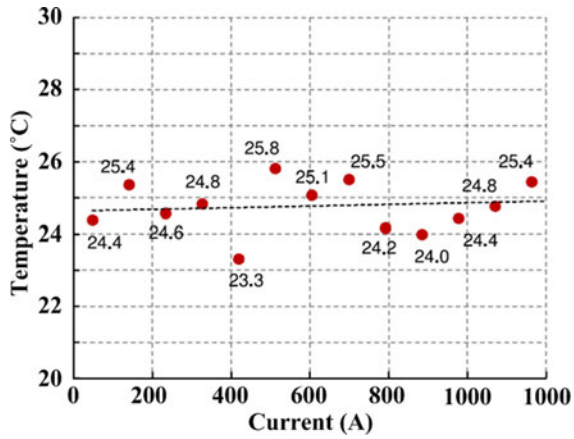

Fig. 42. Estimated temperature versus load current under room temperature, 24.5 °C [81].

$V_{RG\mathrm{ext}}$, $R_{G\mathrm{int}}$ can be calculated based on (14) and the assumptions mentioned above:

$$R_{G\mathrm{int}} = \frac{V_{G+} - V_{G-}}{(V_{RG\mathrm{ext\_peak}}/R_{G\mathrm{ext}})} - R_{G\mathrm{ext}}. \tag{15}$$

where V_{G+} is gate voltage for turning on, V_{G-} is the gate voltage for turning off, $V_{RG\mathrm{ext\_peak}}$ is peak voltage across $R_{G\mathrm{ext}}$, and $R_{G\mathrm{ext}}$ is the external gate resistance.

Fig. 41 shows the calculated $R_{G\mathrm{int}}$ of Infineon FF1000R17IE4 based on $V_{RG\mathrm{ext\_peak}}$ under different temperatures. From this, the relationship between $R_{G\mathrm{int}}$ and temperature is derived as

$$R_{G\mathrm{int}} = (0.917 \cdot 10^{-3}) \cdot T_j + 1.582. \tag{16}$$

Fig. 42 shows the estimated temperature versus load current under room temperature, 24.5 °C. It can be seen from the result that the load current does not alter the temperature measurement method by $R_{G\mathrm{int}}$ and the estimated temperatures agree well with real temperature. Furthermore, this method is not affected by partial bond-wire lift-off. Therefore, this method could be a good option for the PC test. However, this method requires an additional measurement circuit besides the $V_{\mathrm{CE\_ON}}$

TABLE IV
COMPARISON OF INTRODUCED INDIRECT JUNCTION TEMPERATURE ESTIMATION METHODS FOR POWER CYCLING TESTS

Method	Dependents	Linearity	Resolution of sensing parameter	Additional circuit (in addition to $V_{\mathrm{CE\_ON}}$ measurement circuit)	Remarks
$V_{\mathrm{CE\_ON}}(I_{\mathrm{high}})$ [51], [69], [74]–[76]	T, I, V_{GE}	Good linearity	± (2–3) mV/ °C	No	- Require accurate current sensor. - Large estimation error due to nonhomogeneous temperature distribution of internal resistance.
$V_{\mathrm{CE\_ON}}(I_{\mathrm{high}})$ with compensation [56], [77], [78]	T, I, V_{GE}	Good linearity	± (2–3) mV/ °C	No	- Requires efforts to find compensation factors for different kinds of power device modules
$V_{\mathrm{CE\_ON}}(I_{\mathrm{low}})$ [51], [63], [67], [79], [80]	T	Good linearity	2 mV/ °C in Silicon device	Yes	- Interrupt converter operation in AC power cycling test. - Very accurate small current injection is required.
Internal gate resistance ($R_{G\mathrm{int}}$) [73], [81], [82]	T, V_{GE}	Good linearity	(1–3) mΩ/ °C	Yes	- Accuracy is affected by internal gate pads positions of power device modules. - Five main criteria are required for designing a gate driver [69]. - Not applicable for IGBT modules which have gate drives inside of modules.
Gate threshold voltage (V_{TH}) [84]	T	Good linearity	–(2–10) mV/ °C	Yes	- Require disconnection of device from power circuit. - Require increased gate resistor. - May require measurement synchronization accuracy in nanoseconds
Saturation current (I_{sat}) [85]	T, V	Not Linear (Exponential)	Varies depending on temperature range	Yes	- Additional gate voltage is required. - The device is partially turned on with a low gate voltage during the off-state.
Short circuit current (I_{SC}) [86]	T, V	Good linearity	Depending on devices (0.17% of $I_{\mathrm{SC\,max}}$ / °C)	Yes	- Limitation in the measurement frequency
Switching time (rise time, turn-off time) [87]–[90]	T, I, V, V_{GE}	Good linearity	ns/ °C	Yes	- Measuring parameters are influenced by lots of electrical parameters and are too sensitive.

measurement circuit. Furthermore, this method can have a junction temperature estimation error depending on the gate pad position of various IGBTs. Therefore, it requires a good knowledge of the gate pad position.

5) Junction Temperature Estimation Method by Other TSEPs: The gate threshold voltage (V_{TH}) is also one of well-known TSEPs. Considering the *n*-channel MOSFET, the threshold voltage is given by [83]

$$V_{\mathrm{TH}} = \frac{2d}{\varepsilon_{\mathrm{ox}}}\sqrt{\varepsilon_s N_A kT \ln\left(\frac{N_A}{n_i}\right)} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right). \quad (17)$$

where ε_s is the semiconductor permittivity, $\varepsilon_{\mathrm{ox}}$ is the oxide permittivity, d is the oxide thickness, N_A is the acceptor doping density, n_i is the intrinsic carrier concentration, k is the Boltzmann constant, and q is the elementary charge.

The negative temperature dependence is observed mainly due to n_i increase as temperature increases. The sensitivity depends on semiconductors chips. It is generally –2 to –10 mV/ °C range [79].

In [84], the V_{TH} measurement circuit for junction temperature estimation of MOSFETs is proposed. The proposed circuit adds an additional gate resistor of several kΩ in order to measure the current and gate voltage properly by slowing down the turn-on transition when the V_{TH} measurement is required. Furthermore, the V_{TH} measurement is also performed under steady-state condition. For this measurement, an additional switch is required in order to disconnect the MOSFET under test from the main power circuit. Then, gate and drain are connected by additional components when V_{TH} is measured by injecting the small fixed drain current of several mA.

Another known TSEP for IGBTs and MOSFETs is the saturation current (I_{sat}) under a given gate–emitters (gate–source) and a given collector–emitter (drain–source) voltages [85]. I_{sat} of the IGBT can be represented by

$$I_{\mathrm{sat}} = \left(1 + \beta_{\mathrm{PNP}}\frac{\mu_{\mathrm{ns}} C_{\mathrm{ox}} Z_c}{2L_c}\right)\cdot (V_{\mathrm{GS}} - V_{\mathrm{TH}})^2. \quad (18)$$

where β_{PNP} is the current gain of the bipolar transistor in IGBT (for MOSFET, $\beta_{\mathrm{PNP}} = 0$), μ_{ns} is the surface mobility of electrons, C_{ox} is the oxide capacitance, Z_c is the channel width, L_c is the channel length, V_{GS} is the gate source voltage, and V_{TH} is the gate threshold voltage. In (18), μ_{ns} and V_{TH} are the parameters, which are varied depending on temperatures.

In [85], the parameter is used for the junction temperature measurement when the semiconductor is in the off-state by partially turning on the device for 2 μs with a gate voltage of about 6 V. This method interrupts the normal power converter operation as $V_{\mathrm{CE\_ON}}$ at low current. Therefore, an additional circuit

is required to be used for the AC PC test. Furthermore, $I_{\rm sat}$ has an exponential relationship with the temperature, which could cause difficulties in the calibration procedures.

In [86], the short-circuit current, which has a negative thermal coefficient is used as a TSEP for junction temperature estimation. In this method, a hard switching short fault is induced during converter operation by an additional switch for by passing short current, where peak short current is measured for the junction temperature estimation. This method does not disturb the converter operation and thus it can be used for both DC and AC PC tests. The main problem of this method is a very high thermal dissipation during the short circuit, which can cause a fast thermal runaway. Furthermore, the related repetitive short-circuit stress can accelerate the degradation of the DUT.

Besides the above-mentioned methods, the switching time such as rise time and turn-off time can be used for junction temperature estimation [87]–[90]. However, there is a difficulty in real implementation due to the too sensitive measuring parameter. Typically it is ns/ °C.

The introduced indirect junction temperature estimation methods which can be used for PC tests are summarized in Table IV.

VI. Conclusion

In this paper, representative PC test circuits, monitoring circuits of failure indicators, and monitoring strategies under different PC test methods are presented in order to give an insight of PC test design for the reliability assessment of power device modules by providing the current state of knowledge of the topic by organizing and evaluating the current literature.

In the first section of this paper, an overview of the major failure mechanisms and related failure indicators of a standard power IGBT module are given. Then, schematics and operating principles of representative PC test circuits, conventional DC PC circuits, DC PC test circuit with saturation mode of DUT, and AC PC circuits are presented and their features are summarized.

The $V_{\rm CE\_ON}$ and V_F measurement circuits for the condition monitoring of power device modules during PC tests are introduced by dividing into offline and online measurement methods. The offline methods are simple to implement, and have no dependence on PC test conditions. Furthermore, the measurement circuits are relatively simple. However, in the offline measurement methods, the PC test must be stopped for the monitoring of the failure indicators. On the other hand, online measurement methods can monitor the wear-out condition of power device modules under test in real time which gives a convenience to perform the PC test. However, typically, these measurements circuits are complex and more expensive.

Finally, direct and indirect junction temperature estimation methods are presented for the monitoring of solder joint fatigue and also in order to know the applied temperature stress in the PC test. Typically, in direct measurements methods, IR camera and optic fiber sensor are the most widely used methods. These methods are simple to perform but the related equipment are expensive and these methods require the modifications of power device modules. Indirect measurement methods by TSEPs are widely used because they do not need to modify the package of power device modules and less expensive ways. However, the junction temperature measurement in real converter operation such as AC PC test is still under study because a universal solution does not exist yet. The indirect junction temperature measurement methods by TSEPs are introduced and their features are also compared.

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